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Real time validation of adaptive virtual complex impedance-based droop control method for an islanded microgrids

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Nomenclature

f	Frequency
L_f	Filter Inductor
R_f	Filter Resistor
C_f	Filter Capacitor
RES	Renewable Energy Resources
AC	Alternating Current
DC	Direct Current
VSI	Voltage Source Inverter
DG	Distributed generation
MG	Micro-Grid
IMG	Islanded Micro-Grid
PCC	Point of Common Coupling
DER	Distributed Energy Resources
PI	Proportional Integral
DCM	Demand Side Management
HFAC	High Frequency Alternating Current
PC	Point of Connection
DS	Distributed Storage
PV	PhotoVoltaic
LPF	Low-Pass Filter

General Conclusions

This master's thesis aims to enhance the control performance of VSI-based distributed generation (DG) units in an islanded microgrid, focusing on power sharing, power decoupling, power oscillation reduction, and circulating current eliminations, all while utilizing a decentralized method. The virtual impedance concept-based droop control methods are a powerful way to improve the performance and power quality of IMGs. This is especially true when power decoupling, accurate power sharing, and circulating currant suppression are very important. However, these virtual impedance-based methods also have some limitations, including increased control complexity and potential stability issues due to improper design or tuning of the virtual impedance. In this context, we investigated an adaptive virtual complex impedance-based droop control method for three VSI-based DG units in an IMG, and we validated its results using Hardwar-In-the-Loop (HIL) real-time simulation and the OPAL RT OP5700 associated with the OP8660 HIL controller.

In the first chapter of this master's thesis, a brief overview of microgrids discussed in the literature was presented, and then attention was focused on an IMG, which shows many advantages compared to the others, including improved reliability and resilience, energy efficiency and reduced transmission losses, and economic benefits, as well as its utilisation for power requirements in remote and isolated communities, critical infrastructure and facilities (hospitals, data centres, military bases, and emergency services require a highly reliable and uninterrupted power supply), and campus environments (Universities, research parks, and large commercial or industrial complexes).

In the second chapter, we presented a comprehensive analysis of a three-phase voltage source inverter (VSI) with LC filter used as a DG unit in the IMG. We divided this chapter into two main parts. In the first part, we presented the mathematical model of a VSI-based DG module, including the dynamics of both VSI output current and capacitor voltages in different reference frames (*abc*, *αβ*, and *dq*). We use the model in the dq reference frame to develop the inner voltage and current controllers, employing PI controllers to manage the output active and reactive powers and regulate the capacitor voltages. In the second part, we simulate the three phase VSI-based DG unit using the designed controllers in MATLAB/Simulink environment. Simulation results demonstrate that the VSI-based DG unit responds effectively in terms of output currents, capacitor voltages, line currents, and active and reactive powers, as well as load power requirements under any change. These results form the foundation for constructing an IMG with three VSI-based DG units in the subsequent chapter, where an advanced control method is proposed to enhance power sharing, power decoupling, and the elimination of circulating currents within the IMG.

Two virtual impedance-based droop control methods in the dq reference frame have been developed in the third chapter to enhance the control performance of the IMG and their dynamic responses, including power sharing, power decoupling, reduction of power overshoot and oscillation, and elimination of circulating current. The first droop control method is based on the complex virtual impedance concept, and the second droop control method is based on the adaptive complex virtual impedance concept. Simulation results using

MATLAB/Simulink confirm that the virtual impedance-based droop control method is completely possible for controlling the three parallel VSI-based DG units of the IMG. The method enhances power sharing, eliminates power overshoot, and eliminates circulating current in situations where line impedances are mismatches. However, the results obtained from this method demonstrate that any change in the IMG's structure, such as a change in load, swiftly erases these performances. This method's main drawback stems from the selection of the resistive and inductive values of the complex virtual impedance method in the ideal IMG scenario, rendering it incapable of adapting to any changes in the system's structure. In order to address this issue and improve the performance of the IMG, an adaptive virtual complex impedance-based droop control method based on the output reactive power and voltage amplitude of each DG unit is applied. The method's results significantly enhance the control performances of the IMG. The system shares the active and reactive powers equally with few oscillations. It also gets rid of the three DG units' reactive power errors and stops the circulating currents completely. It can be concluded that this control method yields favorable performance and notable enhancements under line impedance mismatches and load changes when compared to both the traditional droop control and the virtual complex impedance-based droop control method.

To validate and examine the performance of the adaptive virtual complex impedance-based droop control method used for controlling the three VSI-based DG units of the IMG, HIL real-time simulations of the three control methods are performed in the fourth chapter using the OPAL RT OP5700 associated with the OP8660 HIL controller. The HIL simulation results show complete similarity to those previously obtained by simulations, further demonstrating the superiority of the proposed adaptive virtual complex impedance-based droop control method. It's interesting to note that the HIL real-time simulations done with the OPAL RT OP5700 and the OP8660 HIL controller pretty much match the real-time implementations. This result indicates that the proposed control method is ready for practical implementation.

This master's thesis is open to a variety of future research avenues. We have listed some of the important aspects of future research below.

- Practical implementation of the proposed control method;
- Applications of new control methods, such as secondary control, for power sharing, voltage, and frequency stabilization;
- Improvement of the IMG systems by using new power VSIs, such as multi-leg and multi-level VSIs.

Chapter 1

Microgrid Overview

1.1. Introduction

Electricity has become vital for modern society due to its important role in the operation of its many applications, such as lighting, heating, communication, and powering everyday devices, that have shaped the way we live and do things. Since the first electric power station PSES “Pearl Street Electric Station” opened for business in 1882, conventional electrical power systems have provided the energy needed for all of these devices [13]. Because of this and the fact that our modern civilization is becoming more and more dependent on energy, stability, resilience, security, and power quality are essential components of electrical power systems [14].

Power substations serve as the link between the three primary components of traditional power networks, which are distribution, transmission, and generating. Because the generation is often done at a distance from the point of consumption, a transformer is utilized to increase the voltage and lower the losses in the transmission system, which is connected to distribution systems to lower the voltage and provide residential, commercial, and industrial customers with electricity at the appropriate voltage levels [15]. Furthermore, ordinary electric power systems are regarded of as passive systems with unidirectional power flows since they employ minimal active components, such as static synchronous compensators and static var compensators.

This aspect raises questions about resilience and dependability because of unforeseen outages, major disruptions, or natural disasters [16].

As a result, in order to satisfy governmental incentives meant to lessen these issues, as well as to answer consumer desires and environmental concerns, traditional electric power networks are undergoing constant and quick modifications. These changes are transforming existing systems. By having additional active components, bidirectional power flows are created from unidirectional ones. In order to provide an intelligent electric network with increased sustainability and dependability, the concept of the "smart grid" has lately gained traction [17]. So, utilizing digital technology to regulate consumer loads to conserve energy and using the idea of microgrids as its foundation, power will be distributed from suppliers to consumers in a way that lowers costs and increases dependability. This idea was created to govern the growing adoption of renewable energy resources (RESs) and provide end users the capacity to produce, store, control, and manage a portion of their energy usage.

Distributed generation (DG), energy storage, electricity distribution lines, and local loads are connected by microgrids, which are small groups that may function both connected and separated from the main grid thanks to control technology. As a result, microgrids enable power to flow both ways with the main distribution network, activating the system as a whole. Additionally, the traditional power networks' transmission and distribution losses may be minimized by integrating distributed generation (DG), which is mostly reliant on RESs.

Grid-connected and island mode are the two primary operating modes for microgrids. The microgrid imports or exports power to and from the main grid in the first one. When there is a disturbance in the primary grid, the microgrid transitions to an island mode and provides electricity to the burdens according to importance. Furthermore, microgrids may be divided into two categories: distribution microgrids, which consist of medium voltage lines that can span several miles and are found in places like industrial parks, military bases, and residential areas. Conversely, low-voltage microgrids for facilities or smaller regions, such a single building, a house, or a collection of buildings next to one another, are covered by these systems [18].

An AC microgrid linked to the main power grid is shown in Fig. 1.1. The microgrid can be disconnected from the grid for island operation by using a circuit breaker at the point of common coupling (PCC). Given that microgrids provide efficient, renewable, and storage

A range of fuel and energy sources may be employed to make the system more adaptable and efficient while serving critical and non-critical loads in an emergency. This makes technologies more appealing when combined into a single energy system. The ac-dc converter is the primary power interface in distributed generation (DG) and a crucial component for dependable control of microgrid systems as power electronics interfaces are typically integrated between specific distributed energy resources (DERs) and the remainder of the microgrid [19].

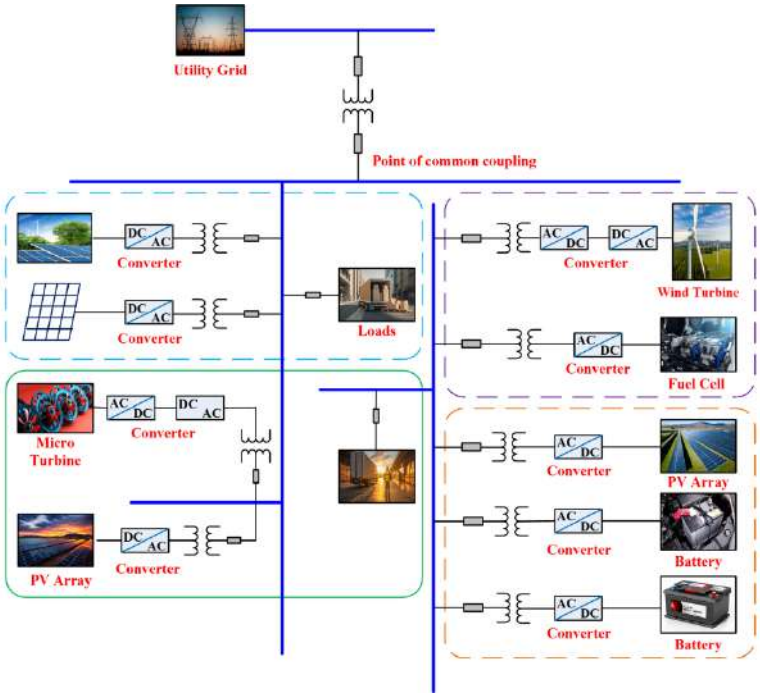


Fig. 1.1: Typical microgrid system architecture

1.2. Distributed Generation Technology

1.2.1. Definition

Distributed Generation Technologies mainly include new energy sources such as fuel cells, wind power and photovoltaic power generation, energy storage devices such as storage batteries, small internal combustion engine generators, and conventional fossil fuel generators [20]. Typically, the DG set is directly connected, via a modular and decentralized way, to the low- or medium-voltage distribution network where the load is placed. Its capacity ranges from several kilowatts to several tens of megawatts. According to [21], DG technology has the following benefits over traditional large-scale power generation technologies:

1. Green, clean, and renewable energy sources are used by DG technologies to produce power. There is no impact from the scarcity of conventional energy sources. It achieves the diversification of energy use, resulting in energy conservation and improved energy efficiency.
2. Decentralized, adaptable, and flexible in position to better utilize RESs while distributing decentralized resources and meeting electricity demands.
3. There is a reduction in the huge cost required for network loss and the upgrading of the transmission and distribution network because the construction period is short, the area is small, the investment is lower, and the electrical and physical distance between the electricity load and the power generation equipment is shortened. Distributed generation provides huge power systems with strong support and a powerful addition. According to [22], mutual backup for big power grids also increases power supply dependability. As a result, the DG system can enhance the flexibility and dependability of the power supply in addition to fully utilizing energy, reducing expenses, and resolving the issue of long-distance transmission while using electricity in remote places.

1.2.2. Literature review of voltage source inverter-based parallel DGs control technology

Early multi-voltage source inverter VSI-based parallel DGs technology research reveals that each parallel unit is classified into three categories: multi-agent method, signal interconnect line method, and

without signal interconnect line method [23]. Centralized control, master-slave control, and decentralized logic control are all included in the signal interconnect line approach [24]. The VSI-based DG module depends on interactive key information to support parallel operation; if this information interaction is disrupted, the parallel system will not be able to function reliably. As a result, the parallel DG units using these methods are unable to realize independent parallel operation. The VSI-based DG based on droop control can realize the autonomous parallel operation in the case that the VSI-based DG has no information interaction.

1.2.3. Parallel VSI-based DGs technology relying on information interaction

In order to achieve information interaction, the VSI-based DG with parallel technology must either add a signal interconnect line between the parallel DG units or employ common mode current, power line, or wireless communication technologies. Due to the heavy dependency on the interaction signals, this restricts the flexibility of the geographical distribution of the VSI-based DG and lowers the redundancy of the parallel system [24]. These techniques can, however, produce output voltage quality and higher current sharing. Currently, the parallel VSI-based DG systems with a shared AC bus are the norm for parallel DG technology with information exchange.

1.3. Essential Ideas and Importance of Microgrid

Micro-grids are one of the most important forms of distributed generation [25], and they are also the most effective form of integration into large power grids. A micro-grid is a small-scale system for producing and distributing power that consists of loads, distributed power supply, protective mechanisms, energy management systems, and monitoring systems. It can operate in isolation as well as be integrated with large-scale power grids to create relatively independent autonomous systems for management, protection, and self-control [26]. As stated by [27], the micro-grid is going to play a significant role in the smart grid. The following are the primary benefits of the microgrid described above [28]:

1) Boost power supply system dependability: Microgrids can guarantee power quality, lower power consumption, and boost local power supply dependability. Moreover, it is concluded that the big power grid's safety and stability may be significantly enhanced by the demand side management (DSM) function that the flexible parallel operating mode of the microgrid can perform [27].

2) Adaptable mode of operation There are two ways that microgrids can function: islanding and grid connectivity. Following grid connection, the microgrid must produce electricity in accordance with big power grid instructions, power dispatching, and the ability of the microgrid's load to receive power from either the large power grid or the microgrid. The micro-power grid can realize a large power grid solution quickly and smoothly, ensuring that the large power grid, load, and distributed power are not affected in the event of a disturbance caused by various faults or intermittent fluctuations of renewable energy from distributed generation [29]. A microgrid can match the local load power supply's dependability when it is run in islanding mode. The microgrid can function as a black-start device in the event that the grid fails, enhancing post-disaster emergency response capabilities and assisting the system in returning to regular operation [30].

3) Boost the effectiveness of energy use. The microgrid can logically improve resource allocation, boost resource utilization, decrease resource waste, and lessen environmental pollution by evaluating the

load's electrical consumption. In addition, distributed generation powered by renewable energy sources is located nearer to the load, resulting in shorter transmission distances, lower line losses, and lower maintenance expenses [31].

4) Encourage the growth of the electric power sector. The microgrid modifies the conventional one-way power transmission system by integrating dispersed power sources of different shapes and sizes into the same physical network. As a separate player in the power market, the microgrid takes part in the marketization process, which supports consistent energy scheduling [32]. Energy management will raise the power industry's service quality and efficiency while also fostering the stable growth of the electrical market. In addition, widespread microgrid deployment can maximize financial gains and lower electricity costs [33]. Businesses have the ability to save energy, cut consumption, electrify rural areas, and significantly enhance the quality of the power supply. The microgrid holds immense importance as a crucial component of the smart grid. In addition to fully realizing the advantages of distributed power supply for both users and power grids, micro-power networks also address the drawbacks of distributed power supply and increase its potential value. Micro-power networks are an efficient use of distributed power supply and an effective supplement to large power grids. Microgrids have drawn more attention and have tremendous development potential [34].

1.4. Microgrid Development Status

In recent years, with the continuing development of energy demand and environmental challenges, the United States, Europe, and Japan have represented the developed countries. The area has embraced proactive and successful initiatives and policies, as well as increased investment in distributed generation. In order to initially construct distributed energy sources, it has actively conducted research on microgrids in conjunction with real-life situations in many nations, based on the sustainable growth of the economy and practical issues of its own power system. In order to confirm that microgrid operation and protection have been resolved, the microgrid model and simulation analysis tools have independently developed control and protection strategies and communication protocols for domestic microgrid construction. They have also established laboratory tests and on-site demonstration projects. Microgrids' efficient integration, adaptability, and intelligent management of distributed power supply have drawn a lot of interest and recognition in the field of distributed energy grid-connected problem solutions [35].

1.5. Microgrid Classification

The microgrid is classified according to the network structure and functional characteristics and can be divided into AC microgrids [36], DC microgrids [37] and AC-DC hybrid microgrids [38].

1.5.1. AC micro-grid

The AC microgrid is currently the main form of microgrid [39]. Power electronic inverters are required to connect distributed power supply, energy storage devices, and other components of the AC microgrid to the AC bus, as seen in Fig. 1.3. The microgrid's grid-connected operation and islanding operation modes can be switched by adjusting the on-grid/off network switch at the common contact point PCC. In [40], a novel high frequency AC (HFAC) microgrid is proposed in addition to the standard AC bus microgrid. In this microgrid,

all distributed power DGs and energy storage devices are connected to high frequency bus, and then supply power to the user's load. HFAC microgrids have certain advantages in terms of miniaturization of equipment, reduction of harmonic influence, improvement of power quality and easy access to AC energy storage equipment due to their high frequency of operation.

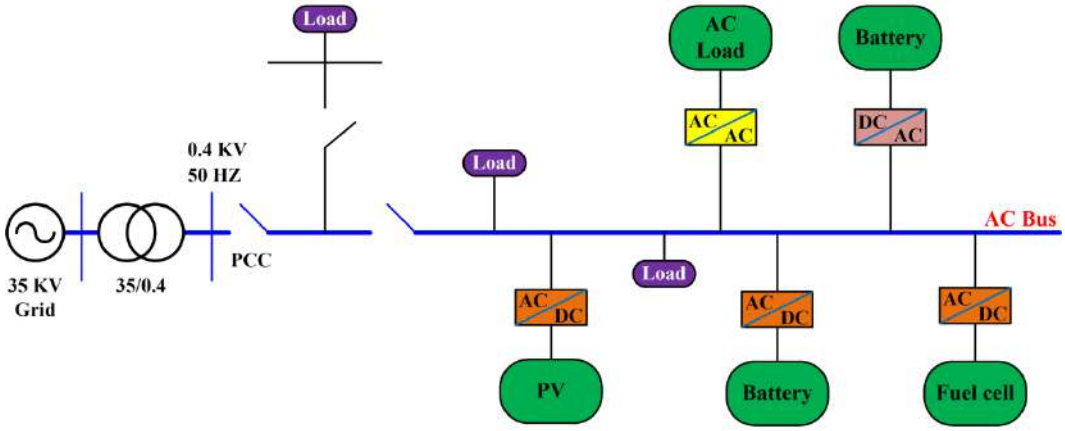


Fig. 1.2: AC microgrid structure

1.5.2. DC microgrid

The distributed power source, energy storage device, and load within the system are all connected to the DC bus, which is a feature of the DC microgrid [41]. As seen in Fig. 1.4, the power electronic inverter equipment connects the DC network to the external AC grid. Through power electronic converters, DC micropower grids can supply power to AC and DC loads at varying voltage levels. The energy storage device on the DC side can also moderate load variations [42]. Two or more DC micro-grids can constitute a dual or multiple circuit power supply mode, depending on the distributed power supply characteristics and the users' requirements for varying levels of power quality [43]. A DC feeder used to supply power to common load types is coupled to a distributed power source with very visible intermittent characteristics.

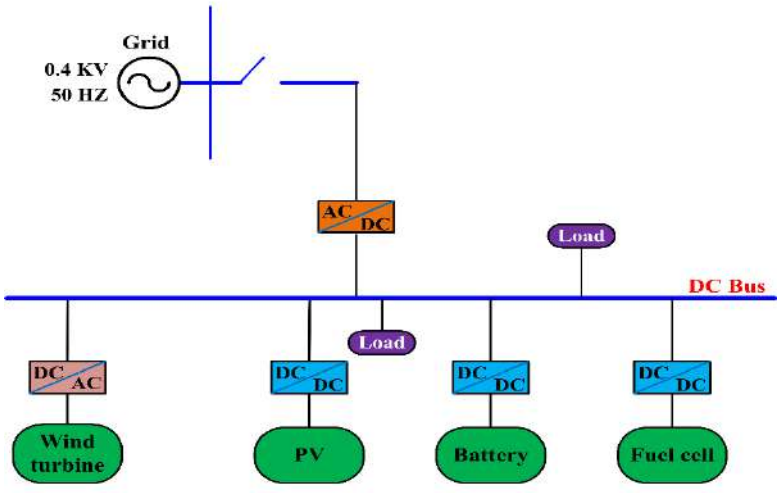


Fig. 1.3: DC microgrid structure

To supply power to loads with increasing demand, a DC feed line links dispersed power sources and energy storage devices with generally smooth operating characteristics. The DC microgrid features fewer levels of voltage conversion equipment between each distributed power source and the DC bus than the AC microgrid, which lowers system construction costs and facilitates control implementation. Suppressing the circulation between various distributed power sources is also more favorable because the synchronization issue between distributed power sources does not need to be taken into account.

1.5.3. AC-DC Hybrid Microgrid

The AC-DC hybrid microgrid structure is shown in Fig. 1.5. In this microgrid, it contains both AC bus and DC bus. It can supply DC to AC loads and can directly supply DC loads and for the hybrid AC/DC microgrid [44], but from the overall structural analysis, it can still be regarded as an AC microgrid and the DC microgrid can be regarded as a unique power source that is connected to the AC bus through the power electronic inverter [45].

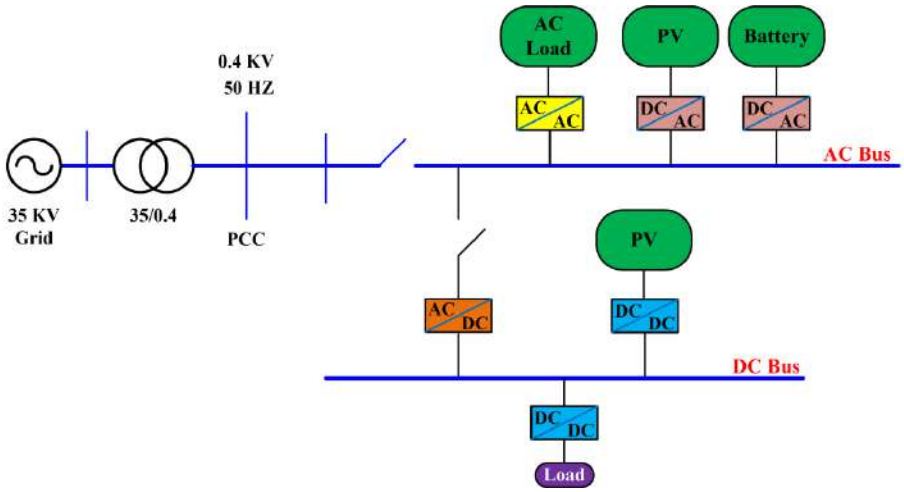


Fig. 1.4: AC and DC microgrid structure

1.6. Advantages and Disadvantages of micro-grid

a) Advantages

- Ability to disconnect from utility grid during disturbance and operate independently.
- It reduces demand on utility grid thus prevents grid failure.
- We can use both electricity and heat energy so that overall efficiency increases.

b) Disadvantages

- Voltage, frequency and power quality should be at acceptable limits.
- Requires battery tanks to store which requires space and maintenance.
- Resynchronization to utility grid is difficult.
- Protection is difficult.

1.7. AC Microgrid Operation Modes

There are two different operating modes: Grid-connected mode and Island mode. The main tasks of the central controller in the Grid-Connected operating mode are summarized as follows:

- Ensuring synchronized operation with the main grid;

- Monitoring system diagnostics by collecting information from the DG units and loads;
- Performing state estimation and security assessment evaluation, economic generation
- scheduling and active and reactive power control;

Moreover, the tasks of the central controller in the Islanded Microgrid (IMG) mode are as follows:

- Frequency and voltage regulation at all points of the microgrid by adjusting active and reactive power control of the DG units;
- Adapting load-shedding strategies using demand-side management with storage device support for maintaining power balance;
- Initiation of a local black start to ensure improved reliability and continuity of service;
- Switching the microgrid back to grid-connected mode after main grid supply is restored without hindering the stability of either grid;

Finally, it must be noted that the whole hierarchical microgrid structure can be implemented in a decentralized manner as done in [30].

1.7.1 Grid-Connected Control

In the grid-connected mode, the microgrid's primary functions are to accommodate :(1) the real or reactive power provided by the DER units and (2) the load demand. The voltage of the microgrid's point of common coupling (PCC) is primarily set by the host grid. At the appropriate point of connection (PC), reactive power injection from a DER unit can be utilized for (1) power factor correction, (2) reactive power supply, or (3) voltage control.

A robust utility network's voltage and/or frequency control cannot be essentially assisted by DER devices with modest power producing capability. In order to prevent interference with the grid's operation, the host utility may not allow the DER units to regulate or control the PCC voltage in the grid-connected mode. As a result, DER units that are close to the PCC (as indicated by the grid's SC_{MVA} and electrical distance) shouldn't actively use a voltage control method [46].

1.7.2. Hierarchical Microgrid Control

Microgrids can be very complex systems just as the main grid; hence, proper control and coordination of its components is required for stable and efficient operation. As a result, a microgrid is transformed into a single, regulated, aggregated system comprising several distributed generation units (DGs) that may communicate with the main grid. It also serves as a crucial part of the smart grid's implementation, guaranteeing energy production, security, dependability, and power quality [20]. The following duties need to be handled by the microgrid control structure [17]:

- Controlling frequency and voltage in both operational modes;
- Resynchronizing the microgrid with the main grid;
- Coordinating DERs for appropriate load-sharing strategies;
- Managing power flow between the microgrid and the main grid;
- Optimizing microgrid resources economically.

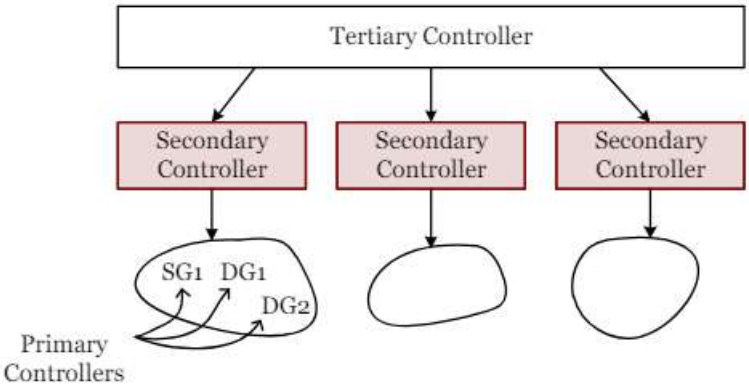


Fig. 1.5: Hierarchical control levels: primary control, secondary control, and tertiary control

1.7.3. Islanded Control

In the islanded mode, the microgrid operates as an independent entity and must provide voltage and frequency control as well as real and reactive power balance. For instance, the microgrid central controller should reduce the net generated power if the load demand is less than the total generation. The DER units are given new set points in order to do this. On the other hand, noncritical load shedding or the activation of storage units must be taken into consideration if the power generated inside the microgrid is insufficient to fulfill the load demand. Applying the hierarchy of control Fig. 1.2 to an islanded microgrid looks like this:

1.7.3.1. Primary Control

Primary control is the first level in the control hierarchy, and it has the fastest response. Primary control responds to the system's dynamics and ensures that its variables, such as voltage and frequency, follow their predetermined values. Primary control primarily operates on a local level, utilizing locally measured signals and conventional linear control methods [47].

1.7.3.2. Secondary control

Secondary control is the next level of control and is responsible for ensuring power quality and mitigating longer term voltage and frequency deviations by determining the set points for the primary control. Although an energy management strategy and a secondary controller share this responsibility [48], the latter does not leverage (1) communication between microgrid components or (2) potential distributed storage (DS) devices like spinning reserves.

Primary control handles the majority of the microgrid's initial transients, and the primary control loop reaches its steady state before the secondary controller updates the set point. This is because secondary control operates on a slower time frame than primary control, with a settling time of about a minute in a conventional grid. Given that the secondary control employs sampled measurements of the microgrid variables, this helps to (1) isolate secondary control from primary control [49] and (2) minimize the communication bandwidth.

1.7.3.3. Tertiary control

Tertiary control is the highest level of control and sets the long term set points depending on the requirements of an optimal power flow, e.g., based on the information received about the status of the DER units, market signals, and other system requirements.

Chapter 2

Modeling and inner voltage control of Single Three-phase Voltage Source Inverter-based Distributed Generation in an Islanded Microgrids

2.1. Introduction

Islanded Microgrid (IMG) is small to medium-scale power system, usually formed by connecting distributed generation (DG) units and local load [7]. The DGs are small sources of energy located remotely or at close proximity to the loads to be supplied. Typical DG technologies include wind power, photovoltaic (PV), fuel cells, microturbines, small hydro, biomass, biogas, geothermal power, and reciprocating internal combustion engines with generators. These systems may be driven by renewable energy sources or fossil fuels [1]. Certain types of DG provide their power through the recovering of the waste heat produced by sources such as the combined heat and power generators, which increases the efficiency and capacity of DGs [7]. DGs-based AC IMG are usually interfaced with voltage source inverter (VSI), which is the critical element for reliable AC IMG that able to control the voltage amplitude and frequency of the AC IMG busbar by using local measurements of its output currents and voltages. So, this chapter reviews the fundamental circuit model of the VSI-based DG unit and its well-established voltage/frequency control.

The block diagram of the VSI-based DG is shown in Fig. 2.1, which consists of a constant DC power source, three phase VSI connected to the load via LC filter and coupling line impedance, and a voltage controller. The last one ensures control of the capacitor voltage amplitude frequency to the load. Frequency is maintained through the capacitor voltage phase angle that is used for each transformation between *abc* frame and synchronous rotating reference frame (*dq*-frame). Whereas, capacitor voltage amplitude control is carried out by combining outer voltage and inner current control loops in order to control both voltage magnitude and transient currents. The two control loops can be implemented by using the well-established proportional and integral controllers (PI-controllers) controllers in dq frame as developed below.

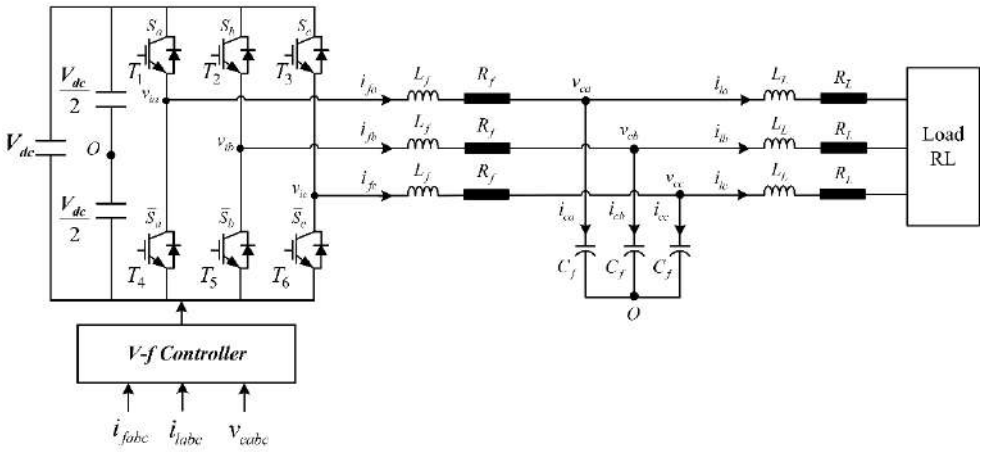


Fig. 2.1: The basic topology of three-phase VSI based DG an islanded MG

In this figure, V_{dc} is the DC input voltage, L_f is the filter inductor, R_f is the filter resistance and C_f is the filter capacitor. a, b, and c three-phase inverter arms from left to right. The three-phase output voltages of the inverter are v_{ia}, v_{ib}, v_{ic}. The three-phase filter capacitor at the output is star-connected and (o) is the midpoint of the filter capacitor. The output voltages of the inverter are the capacitor voltages v_{ao}, v_{bo}, v_{co}. The three-phase inductor or VSI output currents are i_{fabc}.The three-phase output capacitor voltages are v_{cabc}.The three-phase output currents of the load are i_{labc}. The establishment of a mathematical model of a three-phase VSI is the basis for its theoretical analysis and is a prerequisite for the design of reasonable control parameters.

2.2. Modeling of Three-phase Voltage Source Inverter (VSI)

The modeling and local control of the three-phase VSI-based DG unit are critical for the reliable and efficient operation of AC IMGs. By developing accurate models and effective control strategies, we can enhance the performance, stability, and resilience of microgrids, paving the way for sustainable and autonomous energy systems.

2.2.1. Voltage Source Inverter (VSI)

VSI uses semiconducting switches to convert DC voltage to AC voltage. Because the DG units rely on DC sources, the VSIs are essential to the functioning of the IMG that is being studied. Each VSI's control system is also used to manage the IMG locally. Fig. 2.2 shows a three-phase VSI with an output voltage v_i and an input dc-voltage V_{dc}. Together with the input DC voltage at the inverter, the VSI's switching determines the output voltage v_i [50]. The next part will cover pulse-width modulation, which is a common method of controlling the semiconducting switches in the three phase VSI. This control circuit is independent from the rest of the system.

2.2.2. Averaged VSI Model [51]

Since the operation of the VSI is based on the discrete states that arise from the switching of its IGBTs, obtaining a more simplified, comparable model is helpful for control design purposes. Decoupling the DC and AC components of the VSI allows for the derivation of a simpler VSI averaged model, which is a non-harmonic model, as shown in Fig. 2.2. The power balance between the input (DC side) and output (AC-side) of the VSI is the foundation of the model. Three controlled voltage sources with an instantaneous magnitude from the

modulator and a current source on the DC side equal to the current needed to reach the active power injected for a measured voltage characterize this model [52, 53].

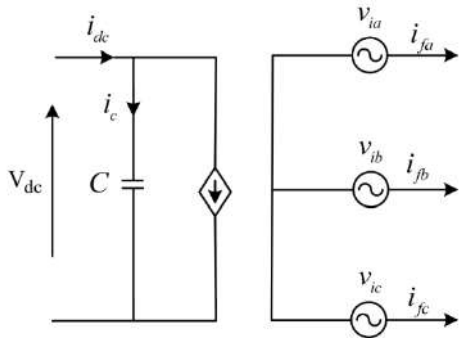


Fig. 2.2: Averaged VSI model circuit

Equation (2.1) represents the active power on the input of the VSI, while equation (2.2) represents the instantaneous active power on the output of the VSI.

$$P_{dcinv} = v_{dc} i_{dc} \tag{2.1}$$

$$P_{acinv} = v_{ia} i_{fa} + v_{ib} i_{fb} + v_{ic} i_{fc} \tag{2.2}$$

The DC input power P_{dcinv} is equal to the AC output inverter power P_{acinv} if both the inverter power losses and commutation power losses are ignored.

2.2.3. Switched Model of the VSI-based DG

The VSI depicted in Fig. 2.1 functions by turning the switching elements ON or OFF in response to the status of the control signals (S_a, S_b, and S_c) generated by the PWM approach. Regardless of i_{fx} polarity, the waveform of the VSI output voltage v_{ix} is exclusively governed by the switching functions given by:

$$S_x = \begin{cases} 1 \text{ if } T_x \text{ is close and } T_{x+3} \text{ is open} \\ 0 \text{ if } T_x \text{ is open and } T_{x+3} \text{ is close} \end{cases} \qquad x = a,b,c \tag{2.3}$$

As shown in Fig. 2.2, the three input voltages of the VSI (v_{ao}, v_{bo}, and v_{co}) called also the potentials of the nodes *a*, *b*, and *c* of the VSI with respect to the imaginary midpoint (*o*) are expressed as a function of the switching states and DC voltage by:

$$\begin{cases} v_{ao} = \dfrac{V_{dc}}{2}(2S_a - 1) \\ v_{bo} = \dfrac{V_{dc}}{2}(2S_b - 1) \\ v_{co} = \dfrac{V_{dc}}{2}(2S_c - 1) \end{cases} \tag{2.4}$$

Using this equation, the VSI line-to-line output voltages are represented as follows:

$$\begin{cases} v_{ab} = v_{ao} - v_{bo} = v_{dc}(S_a - S_b) \\ v_{bc} = v_{bo} - v_{co} = v_{dc}(S_b - S_c) \\ v_{ca} = v_{co} - v_{ao} = v_{dc}(S_c - S_a) \end{cases} \tag{2.5}$$

These line-to-line output voltages are also expressed as a function of the line-to-neutral voltages by:

$$\begin{cases} v_{ab} = v_{an} - v_{bn} \\ v_{bc} = v_{bn} - v_{cn} \\ v_{ca} = v_{cn} - v_{an} \end{cases} \tag{2.6}$$

This gives:

$$\begin{cases} v_{ab} - v_{ca} = v_{an} - (v_{bn} + v_{cn}) + v_{an} \\ v_{bc} - v_{ab} = v_{bn} - (v_{cn} + v_{an}) + v_{bn} \\ v_{ca} - v_{bc} = v_{cn} - (v_{an} + v_{bn}) + v_{cn} \end{cases} \tag{2.7}$$

Since the sum of the voltages in a balanced three-phase system is:

$$v_{an} + v_{bn} + v_{cn} = 0 \tag{2.8}$$

From equations (2.7) and (2.8), we can write:

$$\begin{cases} v_{an} = -(v_{bn} + v_{cn}) \\ v_{bn} = -(v_{an} + v_{cn}) \\ v_{cn} = -(v_{an} + v_{bn}) \end{cases} \tag{2.9}$$

According to equations (2.7) and (2.9), the output line-to-neutral voltages of the VSI are expressed as follows:

$$\begin{cases} v_{an} = \dfrac{v_{ab} - v_{ca}}{3} \\ v_{bn} = \dfrac{v_{bc} - v_{ab}}{3} \\ v_{cn} = \dfrac{v_{ca} - v_{bc}}{3} \end{cases} \tag{2.10}$$

According to equations (2.5) and (2.10), the output line-to-neutral voltages of the VSI are expressed as a function of the DC voltage and switching states (S_a, S_b, S_c) by the following equation:

$$\begin{Bmatrix} v_{ia} \\ v_{ib} \\ v_{ic} \end{Bmatrix} = \frac{V_{dc}}{3} \begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix} \begin{pmatrix} S_a \\ S_b \\ S_c \end{pmatrix} \tag{2.11}$$

From this equation, the output line-to-neutral voltages of the VSI within its eight different switching states are given in the abc and $\alpha\beta$ stationery reference frames as in the Tab. 2.1:

S_c	S_b	S_a	v_{ia}	v_{ib}	v_{ic}	v_α	v_β	$\vec{v}_i$
0	0	0	0	0	0	0	0	$\vec{v}_0$
0	0	1	$-\frac{V_{dc}}{3}$	$-\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$-\frac{V_{dc}}{\sqrt{6}}$	$-\frac{V_{dc}}{\sqrt{2}}$	$\vec{v}_1$
0	1	0	$-\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$-\frac{V_{dc}}{3}$	$-\frac{V_{dc}}{\sqrt{6}}$	$\frac{V_{dc}}{\sqrt{2}}$	$\vec{v}_2$
0	1	1	$-\frac{2V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$-\sqrt{\frac{2}{3}}V_{dc}$	0	$\vec{v}_3$
1	0	0	$\frac{2V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\sqrt{\frac{2}{3}}V_{dc}$	0	$\vec{v}_4$
1	0	1	$\frac{V_{dc}}{3}$	$-\frac{2V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{\sqrt{6}}$	$-\frac{V_{dc}}{\sqrt{2}}$	$\vec{v}_5$
1	1	0	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$-\frac{2V_{dc}}{3}$	$\frac{V_{dc}}{\sqrt{6}}$	$\frac{V_{dc}}{\sqrt{2}}$	$\vec{v}_6$
1	1	1	0	0	0	0	0	$\vec{v}_7$

Tab. 2.1: Possible voltage vectors of the VSI in abc and αβ stationery reference frames

Using the eight vector states and their correspondent output voltages in the Tab. 2.1, we provide the switching polygon of the VSI as shown in Fig 2.3 [51].

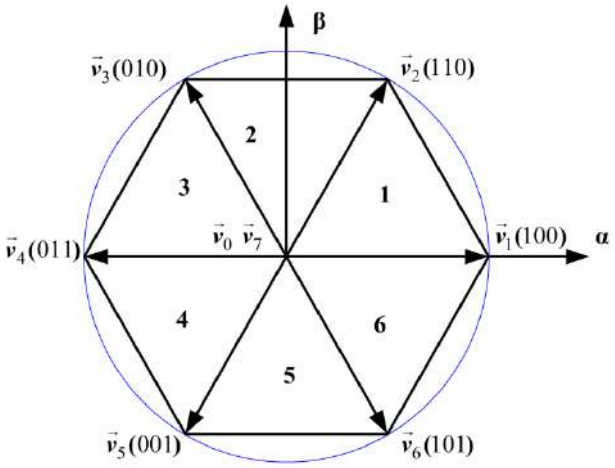


Fig. 2.3: Representation of the switching polygon of the VSI

The matrix form of (2.11) yields the following equation, which defines the VSI conversion matrix:

$$\begin{bmatrix} v_{ia} \\ v_{ib} \\ v_{ic} \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \tag{2.12}$$

On the DC side, the output current is determined by:

$$I_{dc} = \begin{bmatrix} S_a & S_b & S_c \end{bmatrix} \begin{bmatrix} i_{fa} \\ i_{fb} \\ i_{fc} \end{bmatrix} \tag{2.13}$$

2.3. Dynamic model of the three phase VSI

2.3.1. Model of the three phase VSI in the *abc* reference frame

Using Kirchhoff's theorem in the Fig. 2.1, the VSI output current and capacitor voltages dynamics may be expressed as follows:

$$\begin{cases} C_f \dfrac{dv_{ca}}{dt} = i_{ca} = i_{fa} - i_{La} \\ C_f \dfrac{dv_{cb}}{dt} = i_{cb} = i_{fb} - i_{Lb} \\ C_f \dfrac{dv_{cc}}{dt} = i_{cc} = i_{fc} - i_{Lc} \end{cases} \tag{2.15}$$

$$\begin{cases} L_f \dfrac{di_{fa}}{dt} = v_{ia} - R_f i_{fa} - v_{ca} \\ L_f \dfrac{di_{fb}}{dt} = v_{ib} - R_f i_{fb} - v_{cb} \\ L_f \dfrac{di_{fc}}{dt} = v_{ic} - R_f i_{fc} - v_{cc} \end{cases} \tag{2.16}$$

2.3.2. Model of the three phase VSI in the $\alpha\beta$ reference frame

Using the Park transformation with power conservation named the Concordia transformation, the VSI output voltages in the $\alpha\beta$-reference frame by:

$$\begin{bmatrix} v_{i\alpha} \\ v_{i\beta} \end{bmatrix} = T_{3,2} \begin{bmatrix} v_{ia} \\ v_{ib} \\ v_{ic} \end{bmatrix} \tag{2.17}$$

where:

$$T_{3,2} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\dfrac{1}{2} & -\dfrac{1}{2} \\ 0 & \dfrac{\sqrt{3}}{2} & -\dfrac{\sqrt{3}}{2} \end{bmatrix} \tag{2.18}$$

Similarly, the capacitor voltages are expressed in the $\alpha\beta$-reference frame are given by:

$$\begin{bmatrix} v_{c\alpha} \\ v_{c\beta} \end{bmatrix} = T_{3,2} \begin{bmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \end{bmatrix} \tag{2.19}$$

Also, the output currents of the VSI in the *αβ*-reference frame are represented as follows:

$$\begin{bmatrix} i_{f\alpha} \\ i_{f\beta} \end{bmatrix} = T_{3,2} \begin{bmatrix} i_{fa} \\ i_{fb} \\ i_{fc} \end{bmatrix} \tag{2.20}$$

It is advised to convert the three-phase system into a virtual two-phase system in order to simplify the prior VSI model. This results in:

After converting the dynamics of the capacitor voltages and VSI output currents in equations (2.15) and (2.16) from the *abc*-reference frame into *αβ*-reference frame, we obtained:

$$\begin{cases} C_f \dfrac{dv_{c\alpha}}{dt} = i_{c\alpha} = i_{f\alpha} - i_{L\alpha} \\ C_f \dfrac{dv_{c\beta}}{dt} = i_{c\beta} = i_{f\beta} - i_{L\beta} \end{cases} \tag{2.21}$$

$$\begin{cases} L_f \dfrac{di_{f\alpha}}{dt} = v_{i\alpha} - R_f i_{f\beta} - v_{c\alpha} \\ L_f \dfrac{di_{f\beta}}{dt} = v_{i\beta} - R_f i_{f\beta} - v_{c\beta} \end{cases} \tag{2.22}$$

The input DC current of the VSI in equation (2.13) is given as function of the switching states and output current in the *αβ*-reference frame as follows;

$$I_{dc} = S_\alpha i_{f\alpha} + S_\beta i_{f\beta} \tag{2.23}$$

where:

$$\begin{bmatrix} S_\alpha & S_\beta \end{bmatrix} = T_{3,2} \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \tag{2.24}$$

2.3.3. Model of the three phase VSI in the *dq* reference frame

By applying the direct Park transformation on the VSI output voltages in equation (2.17), we obtained these voltages in the dq reference frame as follows

$$\begin{bmatrix} v_{id} \\ v_{iq} \end{bmatrix} = T_{Park} \begin{bmatrix} v_{i\alpha} \\ v_{i\beta} \end{bmatrix} \tag{2.25}$$

where:

$$T_{Park} = \begin{bmatrix} \cos\omega t & \sin\omega t \\ -\sin\omega t & \cos\omega t \end{bmatrix} \tag{2.26}$$

Also, using this transformation, we convert the capacitor voltages from the $\alpha\beta$-reference frame into the dq reference frame as follows:

$$\begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix} = T_{Park} \begin{bmatrix} v_{c\alpha} \\ v_{c\beta} \end{bmatrix} \tag{2.27}$$

Similarly, we obtained the output currents of the VSI in the *dq*-reference frame as follows:

$$\begin{bmatrix} i_{fd} \\ i_{fq} \end{bmatrix} = T_{Park} \begin{bmatrix} i_{f\alpha} \\ i_{f\beta} \end{bmatrix} \tag{2.29}$$

After converting the dynamics of the capacitor voltages and VSI output currents in equations (2.21) and (2.22) from the $\alpha\beta$-reference frame into dq reference frame, we obtained:

$$\begin{cases} C_f \dfrac{dv_{cd}}{dt} = i_{cd} + \omega C_f v_{cq} \\ C_f \dfrac{dv_{cq}}{dt} = i_{cq} - \omega C_f v_{cd} \end{cases} \tag{2.30}$$

$$\begin{cases} L_f \dfrac{di_{fd}}{dt} = v_{id} - R_f i_{fd} + \omega L_f i_{fq} - v_{cd} \\ L_f \dfrac{di_{fq}}{dt} = v_{iq} - R_f i_{fq} - \omega L_f i_{fd} - v_{cq} \end{cases} \tag{2.31}$$

The input DC current of the VSI in equation (2.13) is given as function of the switching states and output current in the *dq*-reference frame as follows:

$$I_{dc} = S_d i_{fd} + S_q i_{fq} \tag{2.32}$$

2.4. Instantaneous active and rective powers in *abc* frame

2.4.1. Instantaneous active power (*P*)

In a three-phase VSI in Fig. 2.1, the instantaneous active power is provided by:

$$P = v_{ca} i_{la} + v_{cb} i_{lb} + v_{cc} i_{lc} \tag{2.33}$$

2.4.2. Instantaneous rective power (*Q*)

The instantaneous reactive power in a three-phase system can be defined in terms of the cross-products of the capacitor voltages and VSI output currents. One common definition uses Clarke transformation to transform the abc-frame quantities to the $\alpha\beta$-frame and then compute the reactive power. However, in the abc-frame, an alternative approach involves defining a power that represents the energy exchanged between phases, which does not contribute to the net energy transfer to the load. This definition is less straightforward but can be understood as:

$$Q = \frac{1}{\sqrt{3}}[(v_{ca} - v_{cb})i_{lc} + (v_{cb} - v_{cc})i_{la} + (v_{ca} - v_{cc})i_{lb}] \tag{2.34}$$

2.4.3. Instantaneous active and rective powers in $\alpha\beta$ -frame

By taking into account balanced three-phase systems and defining capacitor voltage and VSI output current phases as $\bar{V}_{c\alpha\beta} = V_{c\alpha} + jV_{c\beta}$ and $\bar{I}_{l\alpha\beta} = I_{l\alpha} - jI_{\beta}$, respectively, the apparent complex power in $\alpha\beta$-frame may be written as follows [54]:

$$\bar{S} = P + jQ = \bar{V}_{c\alpha\beta}\bar{I}_{l\alpha\beta_{ref}} = \left(V_{c\alpha} + jV_{c\beta}\right)\left(I_{l\alpha} - jI_{l\beta}\right) \tag{2.35}$$

The active and reactive powers as functions of capacitor voltages and VSI output currents in the $\alpha\beta$-frame can be expressed by rearranging equation (2.35) as follows:

$$\begin{cases} P = V_{c\alpha}I_{l\alpha} + V_{c\beta}I_{l\beta} \\ Q = V_{c\alpha}I_{l\beta} - V_{c\beta}I_{l\alpha} \end{cases} \tag{2.36}$$

2.4.4. Instantaneous active and rective powers in the *dq*-frame

Similar to this, the apparent complex power in the *dq*-frame may be found by using $\bar{V}_{cdq} = v_{cd} + jv_{cq}$ and $\bar{I}_{ldq} = i_{ld} - ji_{lq}$ as the capacitor voltage and VSI output current phases, respectively [54]:

$$\bar{S} = P + jQ = \bar{V}_{cdq}\bar{I}_{ldq_{ref}} = \left(V_{cd} + jV_{cq}\right)\left(I_{ld} - jI_{lq}\right) \tag{2.37}$$

The active and reactive powers as functions of capacitor voltages and VSI output currents in the dq reference frame can be expressed by rearranging equation (2.37) as follows:

$$\begin{cases} P = V_{cd}I_{ld} + V_{cq}I_{lq} \\ Q = V_{cd}I_{lq} - V_{cq}I_{ld} \end{cases} \tag{2.38}$$

2.5. Low-Pass Filter (LPF)

The three phase VSI output filter circuits are essential components in power converter systems, particularly in applications where the quality of the output waveform is crucial, which has an important influence on the dynamic and static performance of the VSI output voltage and current control. These filters help to reduce harmonic distortion, mitigate high-frequency noise, and shape the output voltage waveform to meet specific requirements. There are three common types of output filter circuits: L, LC, and LCL filters.

2.5.1. Inductive Filter (L Filter)

A single inductor filter, also known as an L filter, is a basic type of output filter commonly used in power electronic systems, including VSIs. It consists of a single inductor L connected in series with the output load. This configuration forms a low-pass filter that attenuates high-frequency harmonics while allowing the fundamental frequency component (desired output frequency) to pass through with minimal attenuation.this filter is shown in Fig. 2.4:

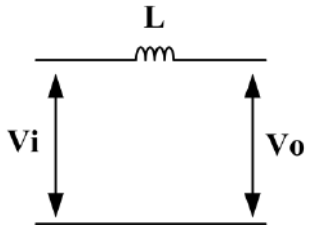


Fig. 2.4: L Filter

2.5.2. Inductive-capacitive Filter (LC Filter)

The LC filter is typically used to removing the higher-order harmonics from the outputs of the VSIs. The cut-off frequency (f_c) of this filter is a trade-off between VSI control bandwidth and harmonic attenuation effect. Decreasing the cut-off frequency increases the harmonic attenuations; but can limits the VSI control bandwidth.

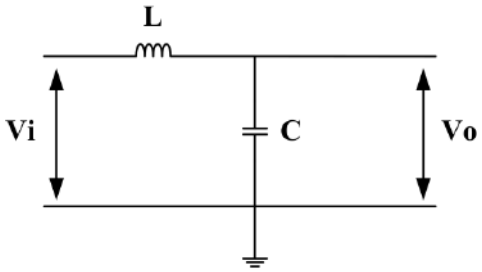


Fig. 2.5: LC Filter

Advantages:

- Simple and economical.
- Provides basic filtering for reducing harmonic distortion.

Disadvantages:

- Limited effectiveness in attenuating high-order harmonics.
- Can introduce resonances if not properly designed.

2.5.3. Inductive-capacitive-inductive Filter (LCL Filter)

The LCL filter is an advanced version of the LC filter, incorporating two inductors (L_{f1} and L_{f2}) and a capacitor (C_f). It provides better harmonic attenuation and improved filtering performance compared to the LC filter. The additional inductor (L_{f2}) helps to mitigate resonances and provides additional filtering of higher-order harmonics. this filter is shown in Fig. 2.6:

Advantages:

- Better harmonic attenuation compared to LC filters.
- Helps to suppress resonances and improve stability.

Disadvantages:

- More complex and expensive compared to LC filters.
- Requires careful design to prevent resonance and ensure stability

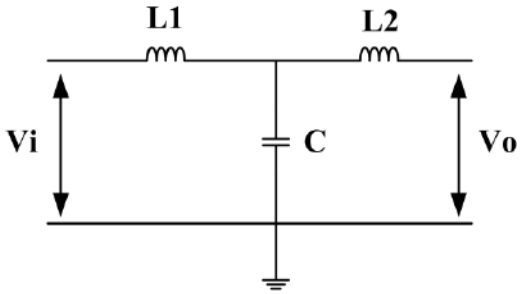


Fig. 2.6: LCL filter

In this theses we are speak to LC Low-Pass filter that show in Fig. 2.5:

2.5.4. Parameters tuning of LC Filter

Usually, the cut-off frequency is maintained between and three times the fundamental frequency and one-five of the switching frequency as [7]:

$$3f_0 < f_c < (1/5) f_{sw} \tag{2.39}$$

The inductance of the LC filter (L_f) is chosen such that its voltage drop remains within 3% of the VSI output voltage as follows [7], [55]:

$$I_{f\max} \times (2\pi f L_f) < 0.03 V_{inv} \tag{2.40}$$

where:

$I_{f\max}$ is the max of the inverter output current.

According to equation (2.40), the inductance of the filter is expressed by:

$$L_f < (0.03 V_{inv}) / (I_{fmax} \times (2\pi f)) \tag{2.41}$$

The cut-off frequency of the LC filter is expressed as a function of the inductance and capacitor by:

$$f_c = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{2.42}$$

According to this equation, the filter capacitance can be calculated as follows:

$$C_f = \frac{1}{(2\pi f_c)^2 L_f} \tag{2.43}$$

According to the system parameters in Tables A.1 and A.2 for I_{fmax} = 15 A and f_c = 150 Hz, we obtained:

L_f = 2 mH and C_f = 150 uF.

2.6. Transmission Lines (feeders)

Usually, in IMGs, feeders are critical components that distribute power from DGs to various load points within the IMG. Feeders can be classified based on the voltage level of the IMGs into three types, which has

resistive feeder (Low Voltage IMG), inductive feeder (High Voltage IMG) or resistive- inductive feeder (Medium Voltage IMG) as shown in Tab. 2.2 [56].

Type of Line	R [Ω/km]	X [Ω/km]	Ratio, R/X
Low Voltage	0.642	0.083	7.7
Medium Voltage	0.161	0.190	0.85
High Voltage	0.06	0.191	0.31

Tab. 2.2: Typical feeder parameters for differnt IMG voltage levels.

2.7. Load

As shown in Fig. 2.1, a resistive-inductive linear load was selected in our thesis to study the characteristic of the DG outputs (active and reactive powers, DG output currents and voltages, and line currents) of the investigated microgrid system, which has chosen to model a residential load, as given in the benchmark microgrid [57]. This load is modelled as a constant impedance ($Z_0=R_0+jX_0$) and it adjusted to provide the nominal active, reactive, and apparent powers at the nominal voltage of the IMG as follows:

$$\begin{cases} S_0 = \dfrac{V_{PCC}^2}{Z_0} \\ P_0 = \dfrac{V_{PCC}^2}{R_0} \\ Q_0 = \dfrac{V_{PCC}^2}{X_0} \end{cases} \tag{2.44}$$

2.8. Design of inner voltage and current controllers in the *dq*-frame

As shown in the general control schema of the three phase VSI-based IMG shown in Fig. 2.7, both capacitor voltages and VSI output currents are controlled using the Vector Oriented Control (*VOC*) concept, which consists of two control loops: the outer capacitor voltage control loop and the inner output current control loop. The basic principle of this method is to convert the three-phase capacitor voltage and output current quantities from the abc reference frame to the *dq*-frame and control them as constant vectors in the steady state with the goal of eliminating the static errors of both vectors by using PI controllers. The transformation of the three-phase capacitor voltage and output current quantities into the *dq*-frame is achieved using the Park transformation with power conservation named the Concordia transformation, in which the phase angle is provided using the phase locked loop (PLL). The details of different parts of the general control schema are described in the next subsections.

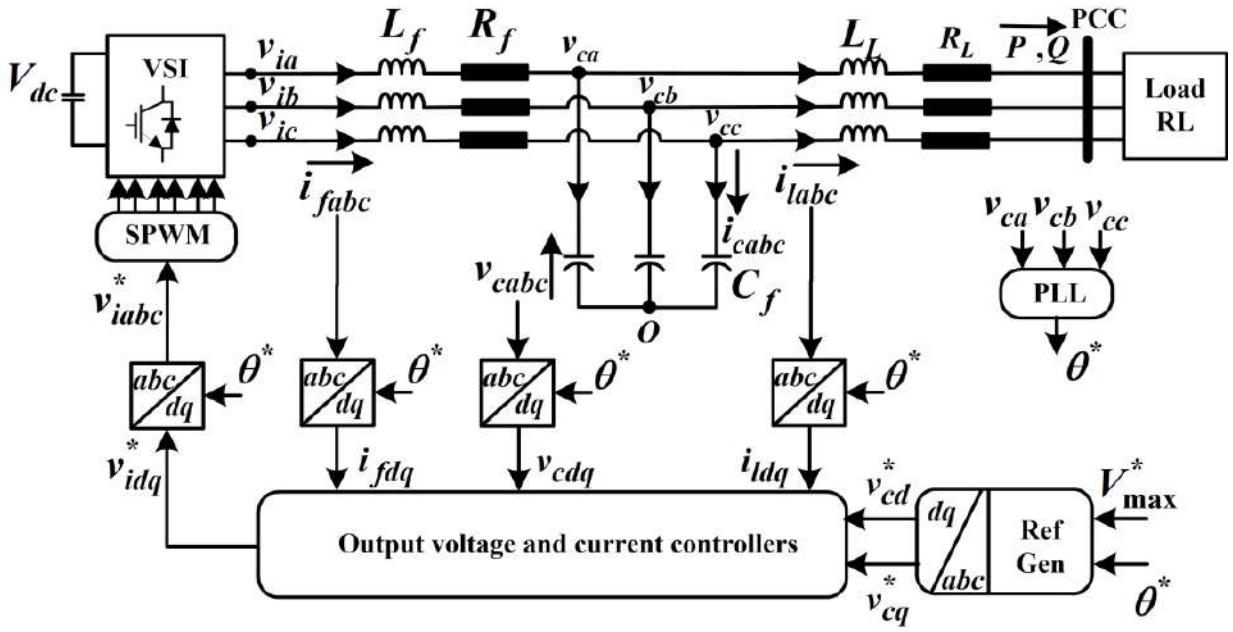


Fig. 2.7: Block diagram of single three-phase VSI based DG of an Islanded Microgrid with control.

2.8.1. Output currents and capacitor voltages dual classed loop controllers in the *dq* reference frame

The main goals of controlling the capacitor voltages are to maintain them pure sinusoidal and balanced under linear and nonlinear; balanced and unbalanced loads, as well as to provide the suitable reference of the inner output current control loop. This latter is used to control the output current for the objectives of controlling the active and reactive powers, decoupling the d-axis and q-axis, i.e., decoupling the active and reactive powers, protecting the VSI circuit against the overcurrent, and to provide the proper VSI output voltage references used in the PWM stage for the generation of PWM switching-states of the VSI to generate good output voltages. In this work both outer voltage control and inner output current control loops are achieved using the PI controllers as shown in Fig. 2.5.

According to the capacitor voltage dynamics in equation (2.27), we obtained the capacitor currents in the dq reference frame as follows:

$$\begin{cases} i_{cd} = C_f \dfrac{dv_{cd}}{dt} - \omega C_f v_{cq} \\ i_{cq} = C_f \dfrac{dv_{cq}}{dt} + \omega C_f v_{cd} \end{cases} \tag{2.45}$$

The terms $C_f \dfrac{dv_{cd}}{dt}$ and $C_f \dfrac{dv_{cq}}{dt}$ are obtained with the opposite of coupling terms from the regulation of the capacitor voltages in the dq frame using *PI*-controllers as follows:

$$\begin{cases} C_f \dfrac{dv_{cd}}{dt} + \omega C_f v_{cq} = i_{cd} = (k_{pv} + \dfrac{k_{iv}}{s})(v^*_{cd} - v_{cd}) \\ C_f \dfrac{dv_{cq}}{dt} - \omega C_f v_{cd} = i_{cq} = (k_{pv} + \dfrac{k_{iv}}{s})(v^*_{cq} - v_{cq}) \end{cases} \tag{2.46}$$

The opposite of the coupling's terms is determined by the *PI*-regulators to compensate the coupling between *d-axis* and *q-axis* of the capacitor voltages.

$$\begin{cases} i_{fd}^{*} = i_{cd}^{*} + i_{Ld} = (k_{pv} + \dfrac{k_{iv}}{s})(v_{cd}^{*} - v_{cd}) - \omega C_f v_{cq} + i_{Ld} \\ i_{fq}^{*} = i_{cq}^{*} + i_{Lq} = (k_{pv} + \dfrac{k_{iv}}{s})(v_{cq}^{*} - v_{cq}) + \omega C_f v_{cd} + i_{Lq} \end{cases} \tag{2.47}$$

According to the VSI output current dynamics in equation (2.47), we obtained the VSI output voltages in the dq reference frame as follows:

$$\begin{cases} v_{id} = L_f \dfrac{di_{fd}}{dt} + R_f i_{fd} - \omega L_f i_{fq} + v_{cd} \\ v_{iq} = L_f \dfrac{di_{fq}}{dt} + R_f i_{fq} + \omega L_f i_{fd} + v_{cq} \end{cases} \tag{2.48}$$

The terms $L_f \dfrac{di_{fd}}{dt} + R_f i_{fd}$ and $L_f \dfrac{di_{fq}}{dt} + R_f i_{fq}$ represent the inductance drop voltages, which are obtained with the opposite of coupling terms from the regulation of the VSI output currents with their references obtained from the regulation of the capacitor voltages in equation (2.47) using PI controllers as follows:

$$\begin{cases} L_f \dfrac{di_{fd}}{dt} + R_f i_{fd} + \omega L_f i_{fq} = u_{ld}^{*} = (k_{pi} + \dfrac{k_{ii}}{s})(i_{fd}^{*} - i_{fd}) \\ L_f \dfrac{di_{fq}}{dt} + R_f i_{fq} - \omega L_f i_{fd} = u_{lq}^{*} = (k_{pi} + \dfrac{k_{ii}}{s})(i_{fq}^{*} - i_{fq}) \end{cases} \tag{2.49}$$

Subtracting equation (2.49) into equation (2.48), we obtain the VSI output voltage references as follows:

$$\begin{cases} v_{id}^{*} = u_{ld}^{*} + v_{cd} = (k_{pi} + \dfrac{k_{ii}}{s})(i_{fd}^{*} - i_{fd}) - \omega L_f i_{fq} + v_{cd} \\ v_{iq}^{*} = u_{lq}^{*} + v_{cq} = (k_{pi} + \dfrac{k_{ii}}{s})(i_{fq}^{*} - i_{fq}) + \omega L_f i_{fd} + v_{cq} \end{cases} \tag{2.50}$$

Also, in this control loop, the opposite of the coupling's terms is determined by the *PI*-regulators to compensate the coupling between d-axis and q-axis of the VSI output currents.

According to the two equations (2.47) and (2.50), the bloc diagram of both control loops is given in the Fig. 2.8:

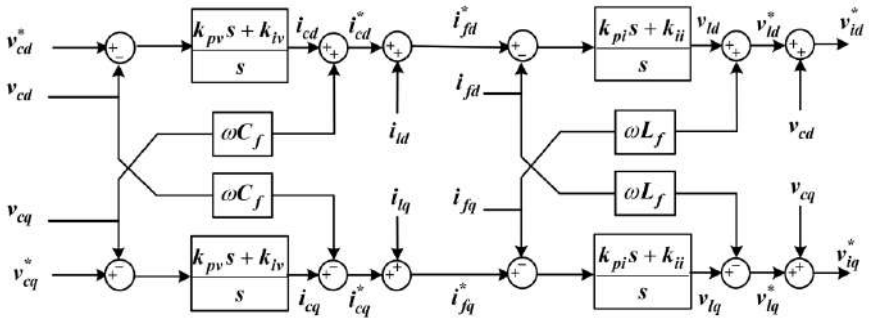
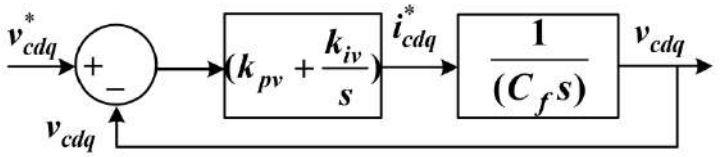


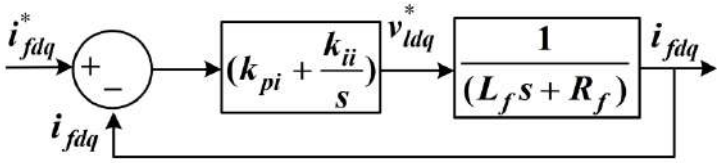
Fig. 2.8: Block diagram of dual loop voltage and current regulations in the dq reference frame

2.8.2. Parameter tuning of PI controllers

In steady state, when considering that the coupling terms of both control loops are compensated, the outer capacitor voltage close loop control and inner output current close loop control output current are given, respectively, in Figs. 2.9 (a and b).



(a)



(b)

Fig. 2.9: Outer capacitor voltage and inner current close loop PI controllers. (**a**) Outer capacitor voltage close loop PI_v control, (**b**) Inner output current close loop PI_i control

According to Fig. 2.9.a, the closed loop transfer function $F_v(s)$ of the capacitor voltage controller is given by:

$$F_v(s) = \frac{v_{cdq}}{v^*_{cdq}} = \frac{\frac{1}{C_f}\left(k_{pv}s + k_{iv}\right)}{s^2 + \frac{k_{pv}}{C_f}s + \frac{k_{iv}}{C_f s}} \quad \textbf{(}2.51\text{)}$$

By identifying this transfer function with the closed loop transfer function of the second order system $F(x)$ given by equation (2.52), we obtain the gains of the PI_v as in equation (2.53):

$$F(s) = \frac{k\omega_c^2}{s^2 + 2\xi\omega_c s + \omega_c^2} \quad (2.52)$$

$$\begin{cases} \frac{k_{pv}}{C_f} = 2\xi\omega_{cv} \\ \frac{k_{iv}}{C_f} = \omega_{cv}^2 \end{cases} \Rightarrow \begin{cases} k_{pv} = 2\xi\omega_{cv}C_f \\ k_{iv} = \omega_{cv}^2 C_f \end{cases} \quad (2.53)$$

Similarly, we calculate the gains of the PI_i controller according to Fig. 2.9.b as follows:

The closed loop transfer function $F_i(s)$ of the output current controller is given by:

$$F_i(s) = \frac{i_{fdq}}{i^*_{fdq}} = \frac{\frac{1}{L_f}\left(k_{pi}s + k_{ii}\right)}{s^2 + \frac{\left(R_f + k_{pi}\right)}{L_f}s + \frac{k_{ii}}{L_f}} \quad (2.54)$$

By identifying this transfer function with the closed loop transfer function of the second order system *F(x)* given by equation (2.55), we obtain the gains of the PI_v as in equation (2.56):

$$F(s) = \frac{k\omega_c^2}{s^2 + 2\xi\omega_c s + \omega_c^2} \tag{2.55}$$

$$\begin{cases} \dfrac{R_f + k_{pi}}{L_f} = 2\xi\omega_{ci} \\ \dfrac{k_{ii}}{L_f} = \omega_{ci}^2 \end{cases} \Rightarrow \begin{cases} k_{pi} = 2\xi\omega_{ci}L_f - R_f \\ k_{ii} = \omega_{ci}^2 L_f \end{cases} \tag{2.56}$$

where :

ξ_v and ξ_i are respectively the damping factor of the PI_v and PI_i controllers. ω_{cv} and ω_{ci} are respectively the cut-off frequency of the PI_v and PI_i controllers.

To achieve well-damped oscillations and a slight overshoot, the voltage and current controllers have chosen a damping coefficient, ξ_v and ξ_i of 0.707. To obtain the correct response, it is therefore possible to determine the natural frequency, ω_{cv} and ω_{ci} for each controller. The condition of choosing ω_{cv} and ω_{ci} is knowing that the cut-off frequency of the voltage control loop is too low comparing to the cut-off frequency of the current control loop $\omega_{ci} \geq 10\omega_{cv}$ [51]. The outer voltage loop's lower cut-off frequency ensures stability and robustness by making the system less sensitive to high-frequency noise, disturbances, and unmolded dynamics, while the inner current loop's higher cut-off frequency provides fast response, better disturbance rejection, and decoupling. Both factors contribute to the system's robustness and stability.

2.9. Simulation results and discussions

To verify the characteristics of the three phase VSI-based DG unit, the system with its inner voltage and current in Fig. 2.3 is simulated under the change of load in both cases balanced and unbalance load using MATLAB/Simulink. The parameters of system and simulation are given in the Appendix A. The results of both cases are presented in the Following subsections:

2.9.1. Characteristics of the VSI-based DG unit under balanced loads

The simulation results of this test when the DG is feeding the three loads are shown in Figs. 2.10 to 2.16. Figs. 2.10 to 2.13 show the steady and transient waveforms of DG output currents and voltages in the abc reference frame, as well as their dq components. These results demonstrate that the DG with its inner voltage and current controller, can track the change in load and provide good output voltage and current waveforms, as well as can perfectly reject the disturbance of load. Both output voltages and currents are sinusoidal and can track their references with a steady state tracking error near zero and with very fast dynamic responses under the change of three phase load. Also, we can observe that the DG can increase its output current to track the change in load and meet its active and reactive power requirements as shown in Figs. 2.15 and 2.16.

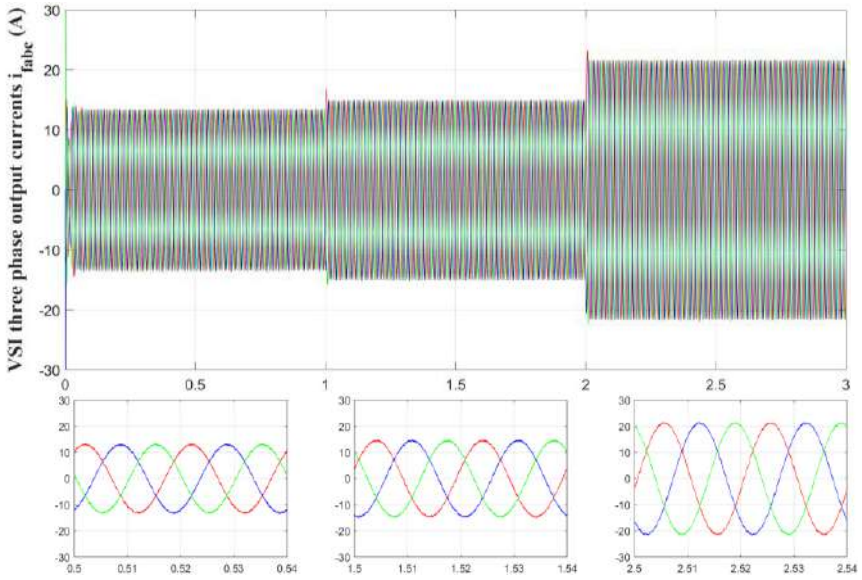


Fig. 2.10: Three phase VSI-based DG output currents.

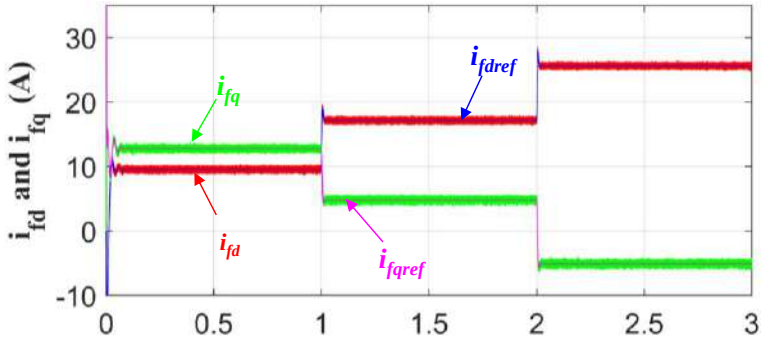


Fig. 2.11: VSI-based DG output currents in the dq reference frame**.**

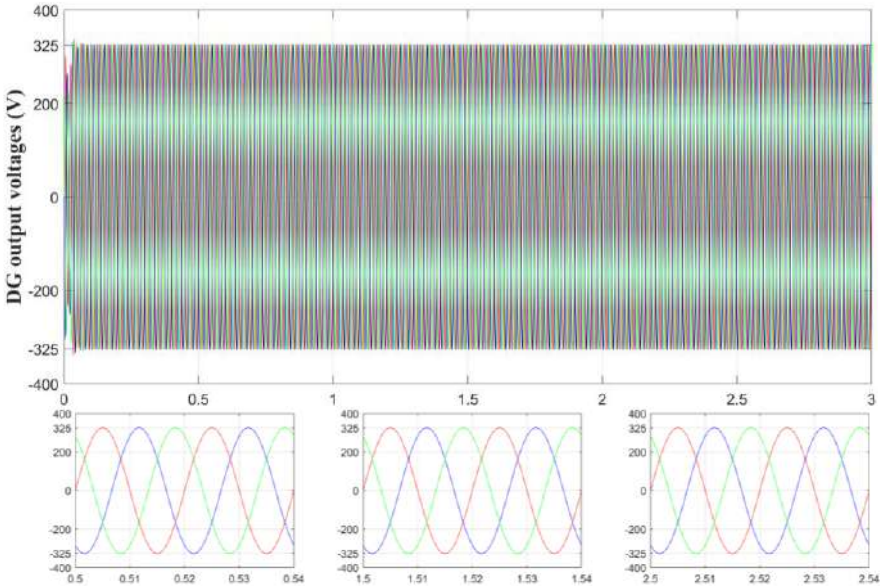


Fig. 2.12: Three phase DG output voltages (capacitor voltages)

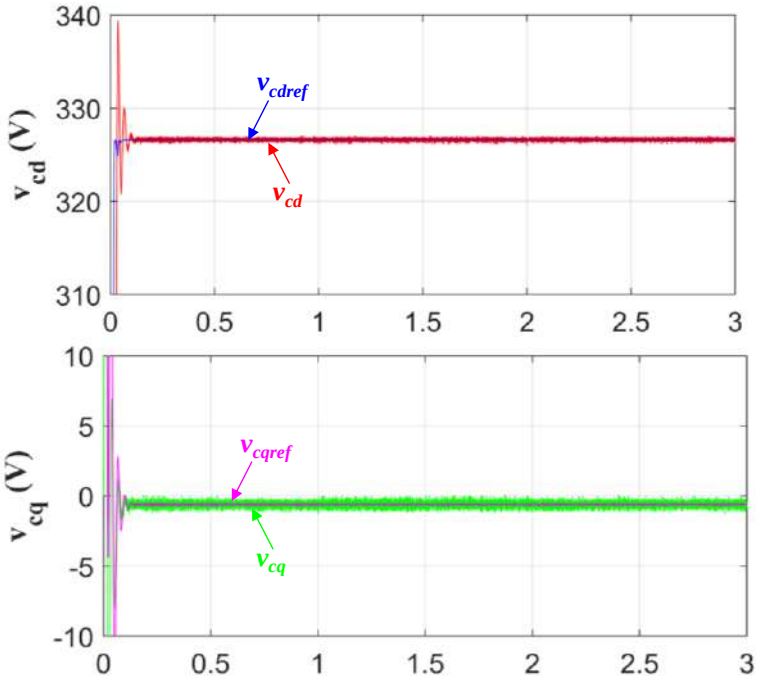


Fig .2.13: DG output voltages in the dq reference frame

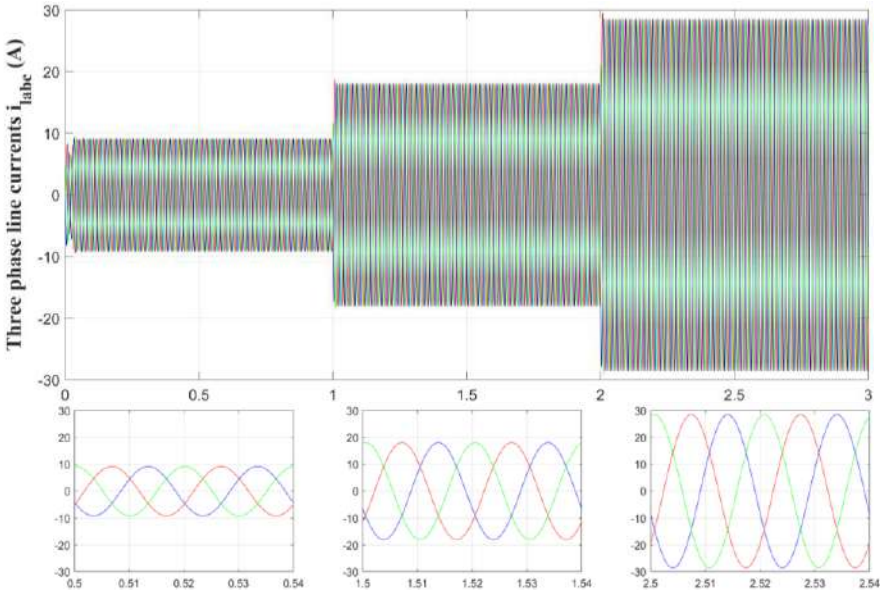


Fig .2.14: Three phase line currents.

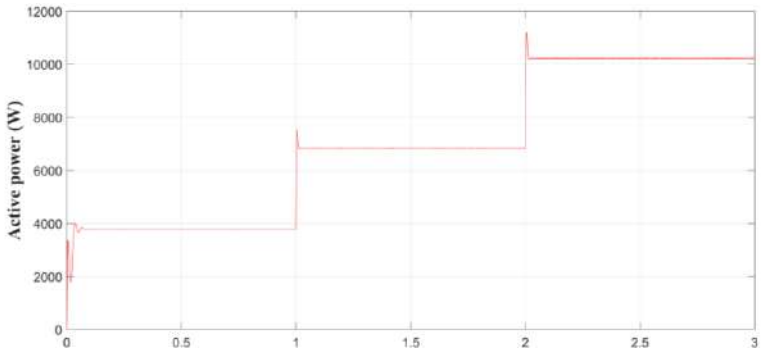


Fig .2.15: DG output active power

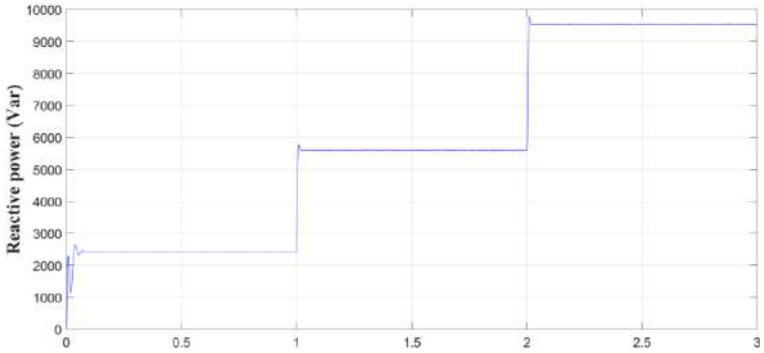


Fig .2.16: DG output reactive power

Figs. 2.17 and 2.18 show the three phase IMG voltages and its RMS value, respectively. Both figures demonstrated that the three phase IMG voltages are sinusoidal under the three loads, with a decrease in its RMS voltage value under any change in load due to the increase in MG impedance drop voltage.

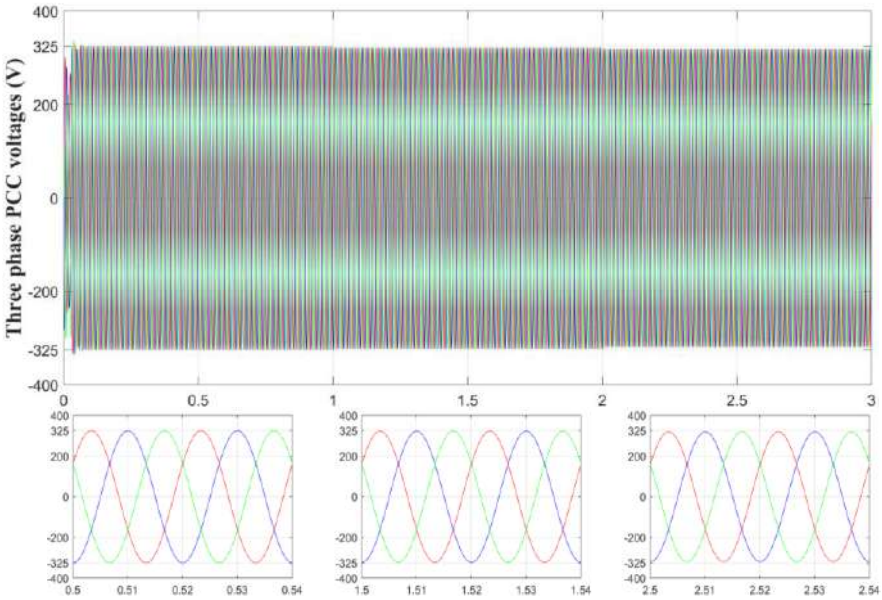


Fig .2.17: Three phase IMG voltages

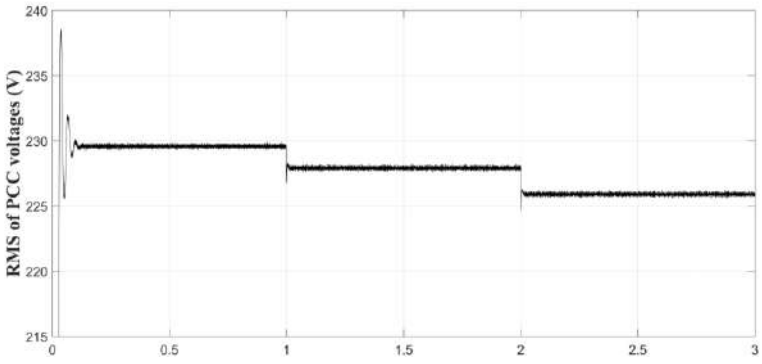


Fig .2.18. RMS voltage of IMG

2.10. Conclusions

In this chapter, a three-phase voltage source inverter with LC filter used as distributed generation unit in an IMG is studied. In the first part of this chapter, the mathematical model of a VSI based DG unit including the dynamics of both VSI output current and capacitor voltages are presented in the three well knowing frames. The obtained dynamic models of the VSI output currents and capacitor voltages in the dq reference frame is

used to develop the inner voltage and current controllers in the dq reference frame to control the output active and reactive powers and regulate the capacitor voltages of the VSI-based DG unit. For both the VSI output current control loop and the capacitor voltage control loop, PI controllers are used. In the second part of this chapter, the characteristics of the three phase VSI-based DG unit are tested and analyzed using the controllers that are designed before. The obtained simulation results show the good responses of the VSI-based DG unit in terms of output currents, capacitor voltages, line currents, active and reactive powers. Based on these, an IMG with three VSI-based DG units is constructed in the next chapter, in which an adaptive virtual complex impedance-based droop control method combined with the inner voltage and current control loop is proposed in the control of the IMG to improve the power sharing among the three DG, the power decoupling, and the circulating current eliminations.

Chapter 3

Adaptive virtual impedance-based droop control of an islanded microgrids

3.1. Introduction

As described in the previous chapter, IMGs have become a practically effective system to fully utilize distributed renewable energy sources, including wind power, photovoltaic (PV), fuel cells, microturbines, small hydro, biomass, biogas, geothermal power, and reciprocating internal combustion engines with generators [1]. DG units should regulate the voltage and frequency on the islanded microgrid (IMG) and supply loads according to their respective capacities. The traditional droop control method with inner voltage/current controllers, which can automatically achieve adequate power sharing between DG units without the help of communications, has been widely used [4]. However, unlike active power, the sharing accuracy of reactive power tends to be barely satisfactory due to mismatched line impedances. Also, under extreme situations, poor reactive power sharing may result in severe circulating currents among the DG units and even cause system instability, which poses a great challenge to the parallel operation of DG units in IMGs [60], [68]. In the literature, one of the most widely used methods to address these problems is the adaptive virtual-impedance-based control method. This method can be used according to the type of line impedance, which has adaptive virtual resistive impedance for IMG with pure resistive line impedances, adaptive virtual inductive impedance for IMG with pure inductive line impedances, and adaptive virtual complex impedance for IMG with complex line impedances. Our work focuses on IMG control with complex line impedances. In this regard, this chapter will present a detailed study of the adaptive virtual complex impedance-based droop control method of three parallel VSIs operating as part of an IMG with complex line impedances. To verify the performance of this control method, a comparison between this method and both the fixed virtual complex impedance-based droop control method and the traditional droop control method is performed under the change of load using MATLAB/Simulink.

3.2. System description

The synoptic structure of the investigated IMG in our thesis is illustrates in Fig. 3.1. It is composed of three DG units connected in parallel via three identical LC-filters to powering three phase loads via three different feeders, in which every DG unit provides a part of the needed power. In each DG, the dc power supply is connected to the PCC through a three-phase VSI.

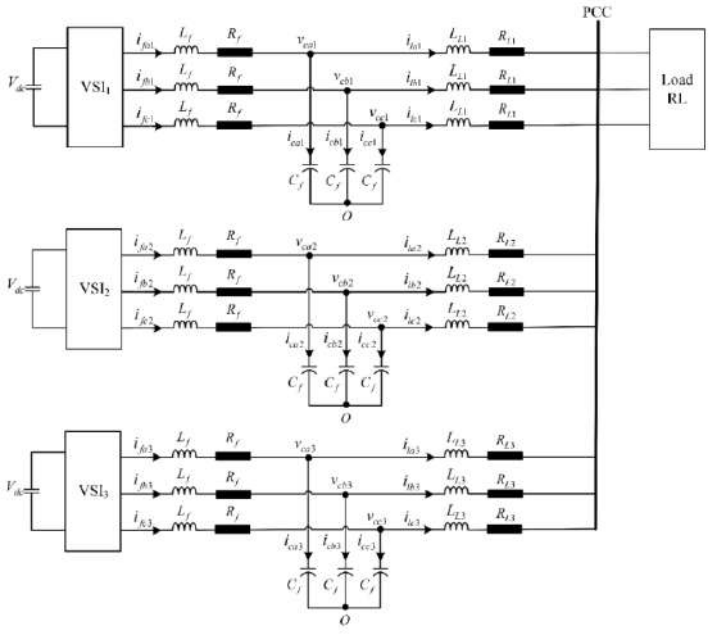


Fig. 3.1: The basic topology of three parallel three-phase VSI based DG an IMG

3.3. Basic principle of traditional droop control and power sharing analysis

The traditional droop control technique has been successfully used in IMGs, which has the "plug-and-play" feature without communication [58, 59]. Due to the random integration locations of DG units, the transmission line impedances of the three DG units are usually different. The local droop controller is used to control the active power and reactive power of each DG unit, as well as the output voltage and frequency.

The droop control technique is developed from the operation of an alternator (i.e. when there is a large demand for active power, the alternator speed increases resulting in drooping the frequency). Similarly, when the reactive load on the alternator is increased, its voltage droops slightly. This principle has been generalized in controlling the three DG-based IMG. The equivalent circuit of multiple DGs in an IMG is shown in Fig. 3.2.

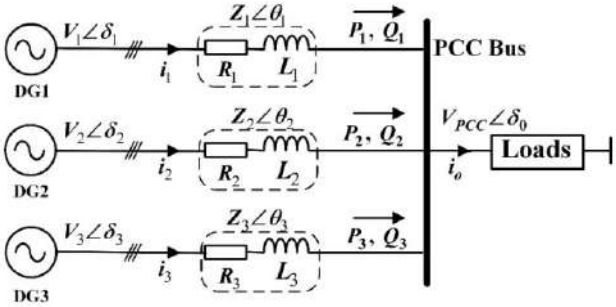


Fig. 3.2: Simplified equivalent circuit of a typical IMG based on three DG units

where $Z_i\angle\delta_i$ (i=1, 2, and 3) is the equivalent impedance of the IMG, which consists of the VSI output impedance and line impedance that can be expressed by:

$$Z_i\angle\delta_i = R_i + jX_i = R_{invi} + jX_{invi} + R_{Li} + jX_{Li} \tag{3.1}$$

The load equivalent impedance is given by:

$$Z_o\angle\theta_o = R_o + jX_o \tag{3.2}$$

where R_{invi} and X_{invi} are respectively the output resistance and output reactance of each VSI-based DG i. Where R_{Li} and X_{Li} are respectively the line resistance and line reactance of each VSI-based DG i. $V_{PCC}\angle\theta_i$ is the ac bus voltage amplitude. V_i are the VSI-based DG output voltages; θ_i is the VSI-based DG output voltage phase angles; δ_i is the total impedance angles of VSI-based DGs; i_i is the output currents of VSI-based DGs; i_o is the load current.

The equivalent circuit impedances Z_i are:

$$Z_i = R_i + jX_i \tag{3.3}$$

The output current of each VSI-based DG unit is given by:

$$i_i = \frac{V_i\angle\theta_i - V_{PCC}\angle\theta_o}{Z_i\angle\delta_i} \tag{3.4}$$

The output power of each VSI-based DG is given by:

$$S_i = P_i + jQ_i = V_i\angle\theta_i.i_i^* \tag{3.5}$$

where i_i^* is the conjugate of the output current of each DG. P_i and Q_i are the outputs active power and reactive power of the VSI-based DG, which are expressed according to Fig. 3.2. as follows [60]:

$$P_i = \frac{\left(V_iV_{PCC}\cos\theta_i - {V_{PCC}}^2\right)\cos\delta_1 + V_iV_{PCC}\sin\theta_i\sin\delta_i}{Z_i} \tag{3.6}$$

$$Q_i = \frac{\left(V_iV_{PCC}\cos\theta_i - {V_{PCC}}^2\right)\sin\delta_1 - V_iV_{PCC}\sin\theta_i\sin\delta_i}{Z_i} \tag{3.7}$$

Normally, the line impedance ratio R/X is small enough in high- or medium-voltage microgrids, and isolated transformers or coupling inductances are usually introduced at the output terminals of VSIs, so the line impedances are assumed to be dominantly inductive [61]. Thus, $Z_i \approx X_i$, $\delta_i \approx 90°$. Usually, the value of δ_i is assumed to be very small, and $\sin\theta_i \approx \theta_i$, $\cos\theta_i \approx 1$. Therefore, equations (3.6) and (3.7) can be simplified as:

$$P_i = \frac{V_iV_{PCC}}{X_i}\theta_i \tag{3.8}$$

$$Q_i = \frac{V_{PCC}}{X_i}\left(V_i - V_{PCC}\right) \tag{3.9}$$

As can be seen from these two equations, reactive power is only related to the voltage amplitude difference, whereas the active power output by the distributed unit is only related to the phase angle. Consequently, by

varying the system's active and reactive power output, the interface VSI's power angle and voltage amplitude can be adjusted. In real-world scenarios, the phase angle difference is acquired through frequency integration, and it is simpler to achieve the adjustment frequency than the phase angle difference through direct adjustment. The relationship of phase-shift angle δ_i and the angular frequency ω_i of each DG unit is derived as $\omega_i = d\delta i/dt$. Consequently, the frequency is controlled by adjusting the DG output active power, and the voltage amplitude is controlled by adjusting its output reactive power. The traditional droop control equation can be obtained as [62]:

$$\omega_i^* = \omega_o - m_p P_i' \tag{3.10}$$

$$V_i^* = V_o - n_Q Q_i' \tag{3.11}$$

ω_o and V_o are the rated frequency and voltage of the IMG, m_p is the P-ω droop coefficient and n_Q is the Q-V droop coefficient, ω_i and V_{ci} are the nominal frequency and output voltage of each DG unit, P' and Q' are the filtered active and reactive powers of each DG unit obtained from the filtering of the measured DG active (P_i) and reactive (Q_i) powers using 2nd order low-pass filter (LPF) which can be represented as:

$$P_i' = \frac{\omega_c^2}{s^2 + 2\xi\omega_c s + \omega_c^2} P_i \tag{3.12}$$

$$Q_i' = \frac{\omega_c^2}{s^2 + 2\xi\omega_c s + \omega_c^2} Q_i \tag{3.13}$$

where ξ *and* ω_c are respectively the damping factor and cut-off frequency of the 2nd order LPF.

The second order low-pass filter is used in our work to filtering the output powers due to its significant advantages such as better attenuation, settling time, flexibility, dynamic performance, and overshoot reduction.

Conventional droop control adjusts the frequency and voltage amplitude of each DG output by comparing the output active power and reactive power to their rated power values. The drooping characteristics of Conventional (P-f and Q-V) droop control are shown in Fig. 3.3 (a and b) [63]:

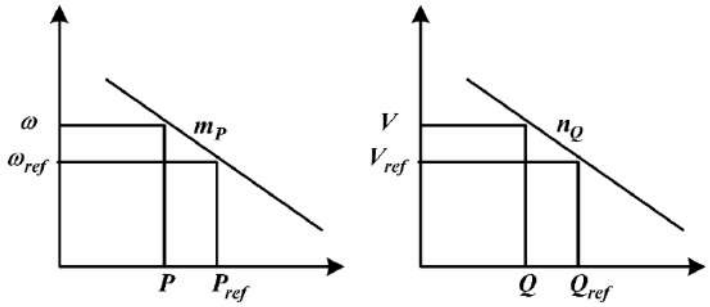


Fig. 3.3: Conventional droop characteristics

P_{ref} and Q_{ref} are respectively the maximum output active and reactive powers of each VSI-based DG unit. ω_{ref} is the system's permitted minimum operating frequency. V_{ref} is the system's permitted minimum output voltage amplitude.

3.4. Control of IMG using conventional (*P-ω*/*Q-V*) droop control method

The schematic diagram of the traditional droop control method-based IMG is shown in Fig. 3.4. Due to similar structure and control strategy of the three parallel DG-based IMG, we present only one DG with its controller to avoid the redundancy. The considered IMG is maintained and operated using two control loops. The outer-loop control which is the traditional droop control used for power sharing among the DGs while the inner-loop output voltage and VSI current control, which is designed in the dq reference frame is responsible of proper turning on/off of the IGBTs of VSI-based DG units in order to generate the desired output voltage. The output voltage and frequency references obtained from the droop loop are used to build the output voltage references in the abc reference frame, which they then transform into the dq reference frame to provide the output voltage references that used in the output voltage controllers. The outputs of these controllers are added to the line current feedforward to provide the VSI output current references used in the VSI output current controllers. The inner-loop control of the VSI-based DG units is discussed in detail in section (2.8.1) of chapter-2 and it will not be repeated here.

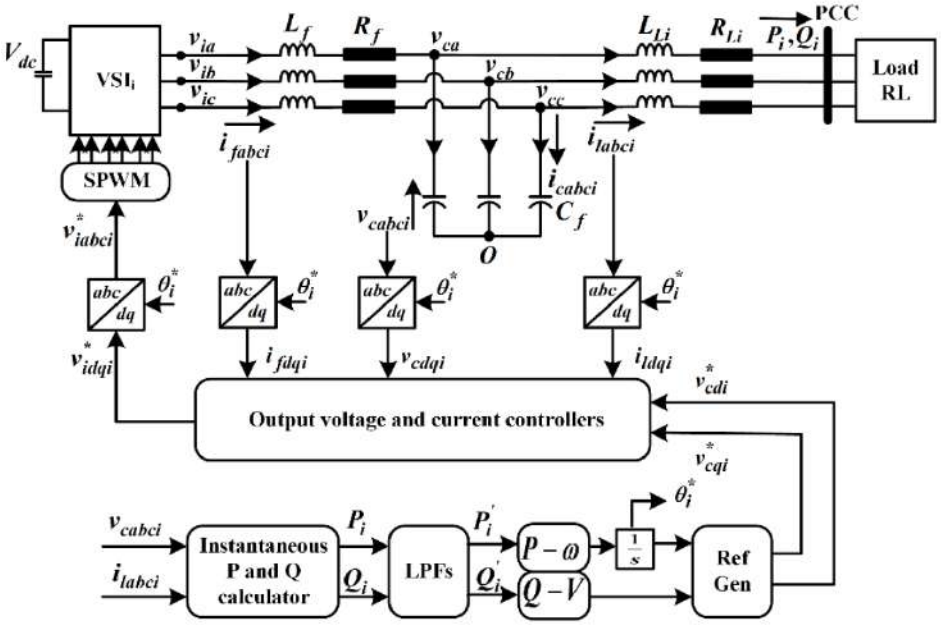


Fig. 3.4: Block diagram of three-phase VSI-based DG of an IMG with traditional droop control method

The output voltage references in the abc reference frame are given by:

$$\begin{cases} v_{cai}^{*} = \sqrt{\frac{2}{3}} V_i^{*} \cos(\theta_i^{*}) \\ v_{cbi}^{*} = \sqrt{\frac{2}{3}} V_i^{*} \cos(\theta_i^{*} - \frac{2\pi}{3}) \\ v_{cci}^{*} = \sqrt{\frac{2}{3}} V_i^{*} \cos(\theta_i^{*} + \frac{2\pi}{3}) \end{cases} \tag{3.14}$$

These voltage references are transformed into the dq reference frame using Concordia transformation, which yields:

$$\begin{bmatrix} v_{cdi}^{*} \\ v_{cqi}^{*} \end{bmatrix} = T_{park} T_{3,2} \begin{bmatrix} v_{cai}^{*} \\ v_{cbi}^{*} \\ v_{cci}^{*} \end{bmatrix} \tag{3.15}$$

3.5. Simulation results

To verify the performance of the traditional droop control method-based IMG in terms of power sharing and circulating current elimination under mismatched line impedances (see Tables A.1 and A.2 in Appendix A), the IMG with three DG units is built in a MATLAB\Simulink based on the block diagram shown in Fig. 3.4. The performances of the traditional droop control method-based IMG are evaluated under four stages of simulation according to load changing and DG turning off. These stages are:

- 1st stage: t=0-1s: 3 DGs ON, load 1 connected,
- 2nd stage: t=1-2s: 3 DGs ON, loads 1 and 2 connected,
- 3rd stage: t=2-3s: 3 DGs ON, loads 1, 2 and 3 connected,
- 4th stage: t=3-4s: *2 DGs* ON (third DG is disconnected), loads 1, 2 and 3 connected.

The main parameters of the target system and their values are given in Tables A.1 and A.2. The simulation results of the traditional droop control method-based IMG are shown in Fig. 3.5 to Fig. 3.11.

Figs. 3.5 and 3.6 show the three DG units output active and reactive power sharing performance. In stage 1, the IMG operates with the three DG units between t = 0 and 1 s, feeding only the first load. At t = 1 and 2 s, the IMG rests with the three DG units, and connects to both loads, 2 and 3, respectively. This not only triggers a step change in the load but also modifies the IMG structure. The IMG rest feeds the three loads before t = 3 s, at which point the third DG unit (DG3) disconnects. It can be seen from these figures that the traditional droop control method can provide good steady-state active power sharing with poor dynamics under the change of load in the four stages, as shown in Fig. 3.5, whereas reactive power sharing exhibits poor steady state performance in the four stages due to the mismatched in line impedance, as shown in Fig. 3.6.

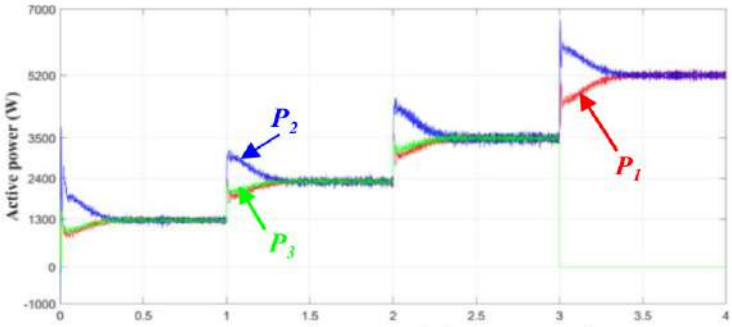


Fig. 3.5: Output active power of the three DG units

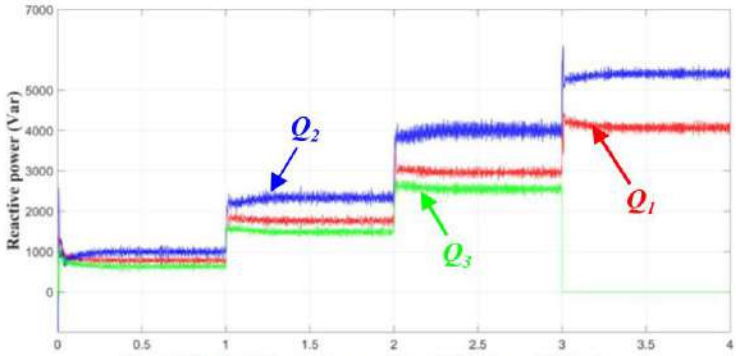


Fig. 3.6: Output reactive power of the three DG units

Fig. 3.7 shows the absolute value of the reactive-power sharing errors $\varepsilon_{qi}(\%)$ of the three DG units. This figure demonstrates that the traditional droop control method can lead to larger reactive-power sharing errors, which can escalate as the load power demand increases. Table 3.1 lists the absolute values of these errors during the four stages.

The reactive-power sharing errors of the three DG are calculated as follows:

$$\varepsilon_{qi}(\%) = 3\left|\frac{\sum_{i=1}^{3} Q_i \Big/ 3 - Q_i}{\sum_{i=1}^{3} Q_i}\right| \tag{3.15}$$

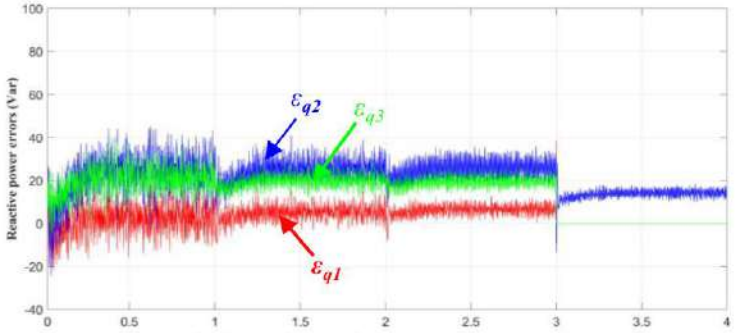


Fig. 3.7: Absolute value of the reactive-power sharing errors

Reactive-power sharing errors	Stage 1	Stage 2	Stage 3	Stage 4
$\varepsilon_{q1}(\%)$	2.5	5	5.5	15
$\varepsilon_{q2}(\%)$	24	25	26	15
$\varepsilon_{q3}(\%)$	23	20	20	/

Table. 3.1: Absolute values of these errors

Figs. 3.8 and 3.9, respectively, show the first phase line currents with their zooms in the four stages, as well as the circulating currents of the three DG units. These figures show that the mismatch in line impedance prevents the traditional droop control method from achieving line current equalization between the three DG units, which can offer larger peak circulating current values between the three DG units in the four stages. The peak values of the circulating currents escalate as the load power demand increases. Table 3.2 lists the peak values of the circulating currents during the four stages.

The circulating currents between the first phases of the three DG are calculated as follows:

$$\begin{cases} I_{CC1} = i_{la1} - i_{la2} \\ I_{CC2} = i_{la2} - i_{la3} \\ I_{CC3} = i_{la3} - i_{la1} \end{cases} \quad (3.16)$$

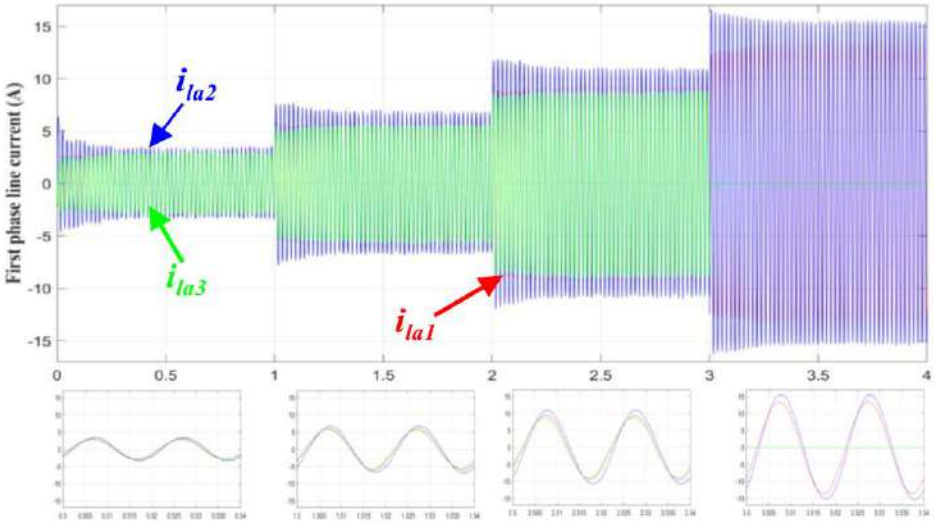


Fig. 3.8: First phase line currents with their zooms in the four stages

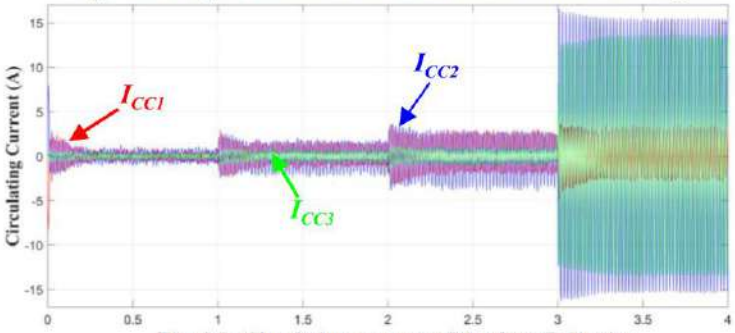


Fig. 3.9: Circulating currents of the three DG units

Peak values of the circulating currents	Stage 1	Stage 2	Stage 3	Stage 4
I_{cc1}(A)	1.4	3	5	6
$I_{cc\ 2}$(A)	2	4	7	/
$I_{cc\ 3}$(A)	1	1.5	2	/

Table. 3.2: Peak values of the circulating currents

Figs. 3.10 and 3.11, respectively, display the RMS voltage values of the IMG and the output of the three DGs. These figures show that both voltages follow the same profile, with the IMG voltage having a lower value due to the voltage drop across the line impedance. The IEEE 1547 Standard, IEEE 2030.7 Standard, and IEC 62257-4 Standard also confirm that the maximal IMG voltage drop does not surpass the system regulations.

- *The IEEE 1547 Standard serves as a framework for interconnecting distributed resources with electric power systems. This standard provides requirements for the interconnection of distributed energy resources (DERs) with electric power systems, including microgrids. It includes voltage regulation requirements and specifies that the voltage deviation should not exceed ±5% of the nominal voltage at the PCC* [64].
- *The IEEE 2030.7 Standard provides a specification for microgrid controllers. This standard defines the functions and features of microgrid controllers, including voltage regulation. It recommends that the voltage deviation not exceed ±5% of the nominal voltage at the load terminals* [65].

- *IEC 62257 Series of Standards for Renewable Energy and Hybrid Systems for Rural Electrification: These standards cover the design, installation, and operation of microgrids, particularly in rural areas. The IEC 62257-4 standard specifies that the voltage drop in distribution lines should not exceed 5% of the nominal voltage at the load terminals* [66].

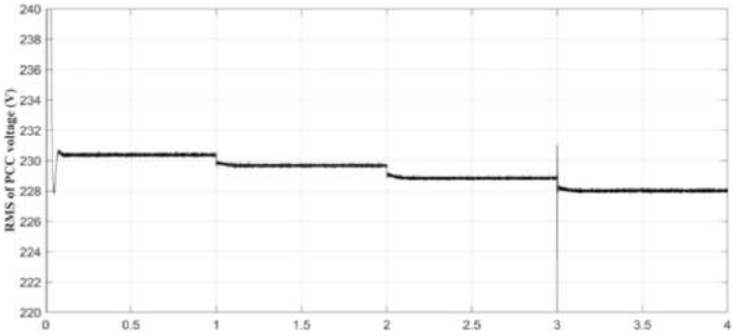


Fig. 3.10: RMS voltage of the IMG

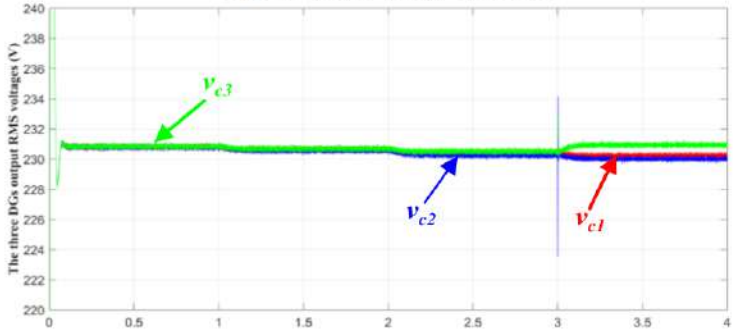


Fig. 3.11: Output RMS voltage of the three DGs

The results of this test demonstrate that the mismatched line impedance in an IMG can significantly affect the performance of both power sharing and circulating current suppression, and the traditional droop control strategy makes it difficult to evenly share the reactive power and restrain the circulating current among multiple parallel VSI-based DG units in an IMG. The next subsection of this chapter investigates a complex virtual impedance-based droop control method to address the issues with the traditional droop control strategy, enhancing the accuracy of active and reactive power sharing, power decoupling, and circulating current suppression.

3.6. Virtual complex impedance-based droop control method

Multiple parallel VSI-based DG units widely use the concept of a fixed virtual impedance-based droop control method to overcome the challenges of the traditional droop control strategy and enhance the accuracy of active and reactive power sharing, power decoupling, and circulating current suppressions. In this method, a virtual impedance loop is introduced in parallel with the traditional droop control loop to provide the output voltage references of the output voltage controllers. This virtual impedance loop emulates the behavior of physical impedances, such as resistors or inductors, in the microgrid system. The key aspects of the virtual-impedance-based control method are as follows:

1. Virtual impedance loop: In this loop, a virtual impedance is introduced between the output of each VSI-based DG unit and the PCC in the IMG. This virtual impedance can be resistive, inductive, or a combination of both.

2. Power decoupling and sharing: The virtual impedance loop helps to decouple the active and reactive power flows in the IMG, allowing for more accurate power sharing and circulating currant suppressions among the VSI-based DG units even under mismatched line impedance and unbalanced load conditions. This is achieved by introducing a phase shift between the voltage and current at the output of each DG.
3. Voltage regulation and stability: The voltage compensation provided by the virtual impedance loop helps to maintain tight voltage regulation at the PCC, improving the overall power quality and stability of the IMG.

You can use this method based on the type of line impedance, such as virtual resistive impedance for IMG with pure resistive line impedances [67], virtual inductive impedance for IMG with pure inductive line impedances [68], and virtual complex impedance for IMG with complex line impedances (medium-voltage microgrid) [69]. This study looks at an IMG that has a complex line impedance of the inductive-resistive type. To control it, we will use the fixed virtual inductive-resistive impedance-based droop control method.

3.6.1. Concept of the fixed virtual complex impedance-based droop control method

Fig. 3.12 depicts the equivalent circuit schematic of the investigated IMG with virtual complex impedance. The virtual complex impedance is included at the output of each DG units to adjust the equivalent output impedance of each DG.

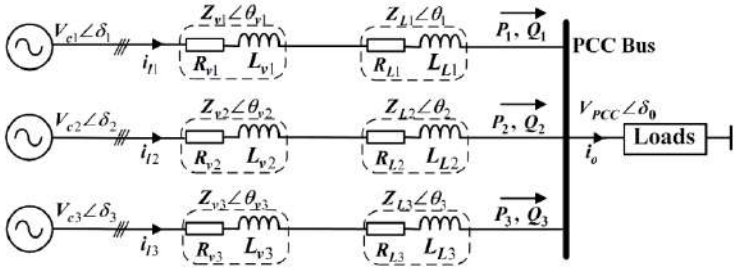


Fig. 3.12: Equivalent circuit of a typical IMG including virtual complex impedance

where $Z_{Li}\angle\theta_i$ is the line impedance of the IMG, $Z_{vi}\angle\theta_{vi}$ is the virtual impedance of the IMG, after using the virtual impedance, the equivalent circuit impedances Z_i in equation (3.3) is becomes:

$$Z_i = Z_{vi}\angle\theta_{vi} + Z_{Li}\angle\theta_i = R_{vi} + jX_{vi} + R_{Li} + jX_{Li} \tag{3.17}$$

where R_{Li} and X_{Li} are respectively the line resistance and line reactance of each VSI-based DG i. R_v and X_v are respectively the virtual resistance and virtual reactance of each VSI-based DG i.

The virtual complex impedance is given by:

$$Z_{vi} = R_{vi} + X_{vi} \tag{3.19}$$

The VSI-based DGs output current in equation (3.4) is becomes:

$$i_i = \frac{V_i\angle\delta_i - V_o\angle\delta_o}{Z_{vi}\angle\theta_{vi} + Z_{Li}\angle\theta_i} \tag{3.20}$$

3.6.2. Reactive Power Sharing Errors Analysis

According to [68], [70] and when we assume that the inner capacitor voltage control loop can force the DG output voltages to perfectly track their references in each DG unit, so we have $V_i^* = V_i$ and $\omega_i^* = \omega_i$, and when considering that the output voltage phase angle δ_i is very small [71, 72]. Thus, the voltage drop across the line impedance can be approximated as:

$$\Delta V \approx \frac{PR + XQ}{V_o} \tag{3.21}$$

where R and X represent the equivalent IMG resistance and reactance between each DG output and the PCC after adding the virtual impedance, P and Q represent the active power and reactive power flowing through the transmission line impedance, respectively. Based on the simplified equivalent circuit of the three DG units in Fig. 3.12, the voltage and current phasor diagram of DG_1 is obtained in Fig. 3.13, and its output voltage (V_{c1}) is expressed as in equation (3.22) [71]:

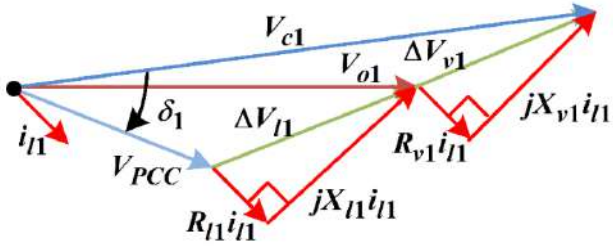


Fig. 3.13: Voltage phasor diagram of the first DG with the virtual complex impedance

$$V_{c1} = V_{PCC} + \Delta V_{l1} + \Delta V_{v1} \tag{3.22}$$

where: ΔV_{l1} is the voltage drop across the line impedance and ΔV_{v1} is the virtual voltage drop across the virtual impedance.

Using the voltage drop across the line impedance approximation in equation (3.21), the DG output voltage (V_{c1}) in equation (3.22) becomes:

$$V_{c1} \approx V_{PCC} + \frac{P_1 R_{L1} + X_{L1} Q_1}{V_o} + \frac{P_1 R_{v1} + X_{v1} Q_1}{V_o} \tag{3.23}$$

Similarly, the output voltages of the DG_2 and DG_3 are expressed as follows:

$$V_{c2} \approx V_{PCC} + \frac{P_2 R_{L2} + X_{L2} Q_2}{V_o} + \frac{P_2 R_{v2} + X_{v2} Q_2}{V_o} \tag{3.24}$$

$$V_{c3} \approx V_{PCC} + \frac{P_3 R_{L3} + X_3 Q_{L3}}{V_o} + \frac{P_3 R_{v3} + X_{v3} Q_3}{V_o} \tag{3.25}$$

Because the active power sharing is always accurate in the steady state [62], so $P_1 = P_2$. When we Assume that DG_1 and DG_2 have the same droop coefficients ($m_{P1} = m_{P2}$, $n_{Q1} = n_{Q2} = n_Q$) to simplify analysis. By solving

the equations (3.11), (3.21), (3.23) and (3.24), the error of the reactive power sharing between the first and second DG units can be expressed as follows:

$$\Delta Q = \frac{Q_1\left(\Delta X_{L1,L2} + X_{v2} - X_{v1}\right) + P_1\left(\Delta R_{L1,L2} + R_{v2} - R_{v1}\right)}{n_Q V_o} \tag{3.26}$$

where $\Delta X_{L1,L2} = X_{L2} - X_{L1}$, $\Delta R_{L1,L2} = R_{L2} - R_{L1}$.

Equation (3.26) indicates that both virtual resistance and inductance (R_{vi} and X_{vi}) should be simultaneously adjusted to compensate the mismatched line impedance among DGs in order to eliminate the reactive power sharing error in equation (3.26). As a result, reactive power sharing is accurately achieved, and its dynamic performance is guaranteed even if the load changes. In addition, the circulating current is suppressed due to the balanced voltage drop between the DG and PCC.

The drop voltages across the virtual impedance in each DG are expressed in the abc reference frame by:

$$v_{vabci} = R_{vi} i_{labci} + L_{vi} \frac{di_{labci}}{dt} \tag{3.27}$$

These drop voltages are given in the dq reference frame as follows:

$$\begin{cases} v_{vdi} = R_{viri} i_{ldi} + L_{vi} \dfrac{di_{ldi}}{dt} - \omega L_{vi} i_{lqi} \\ v_{vqi} = R_{vi} i_{lqi} + L_{vi} \dfrac{di_{lqi}}{dt} + \omega L_{vi} i_{ldi} \end{cases} \tag{3.28}$$

The drop voltages across the virtual impedance in each DG are implemented in the dq reference frame as shown in Fig. 3.14.

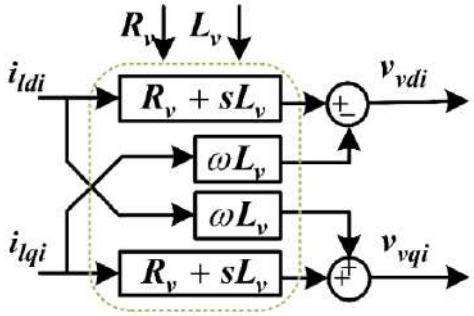


Fig. 3.14: Block diagram of the drop voltages across the virtual impedance in the *dq* reference frame

The new voltage references are obtained by subtracting the drop voltage across the virtual impedance from the output voltage references obtained from the droop control loop in equation (3.15) as follows:

$$\begin{cases} v_{crefdi} = v^*_{cdi} - R_{vi} i_{ldi} - L_{vi} \dfrac{di_{ldi}}{dt} + \omega L_{vi} i_{lqi} \\ v_{crefqi} = v^*_{cqi} - R_{vi} i_{lqi} - L_{vi} \dfrac{di_{lqi}}{dt} - \omega L_{vi} i_{ldi} \end{cases} \tag{3.29}$$

The schematic diagram of the fixed virtual complex impedance-based droop control method-based IMG is shown in Fig. 3.15. The considered IMG is nearly similar to the one utilized in the previously section except

that in this section a virtual complex impedance has been added to eliminate the lines mismatch through adjusting the obtained voltage references from the droop which leads to accuracy reactive power sharing and circulating current elimination.

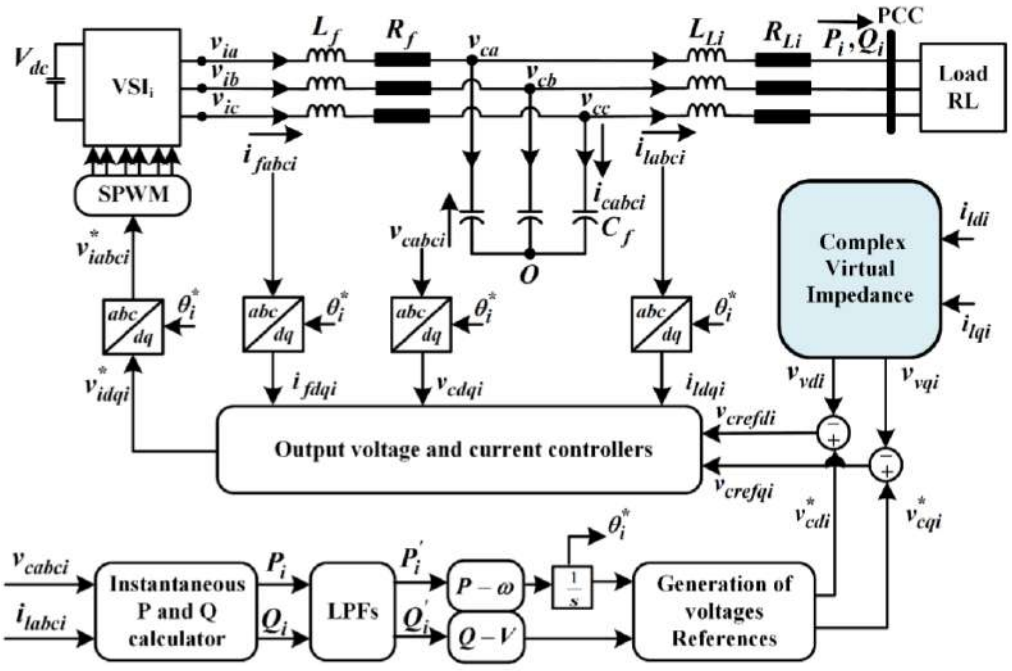


Fig. 3.15: Block diagram of three-phase VSI based DG of an IMG with fixed virtual complex impedance-based droop control method

3.7. Simulation results

To verify the performance of the virtual complex impedance-based droop control method for the IMG, a simulation test was performed using MATLAB/Simulink based on the block diagram shown in Fig. 3.15 with the same parameters and loads that adopted in previous section (see Tables A.1 and A.2 in Appendix A). The obtained simulation results are shown in Fig. 3.16 to Fig. 3.22.

Figs. 3.16 and 3.17 show the three DG units output active and reactive power sharing performance in the four stages. These figures demonstrate that the virtual complex impedance-based droop control method for the IMC can effectively meet the increases in load power demand. It ensures accurate sharing of both active and reactive powers, minimizing overshoot during load changes and DG unit disconnection. Furthermore, Fig. 3.18 shows a significant reduction in reactive power sharing errors compared to the traditional droop control method. However, as shown in these figures, these results cannot meet the required power sharing performance. The power oscillations and reactive power sharing errors have not been completely eliminated. Table 3.3 lists the absolute values of the reactive power sharing errors during the four stages.

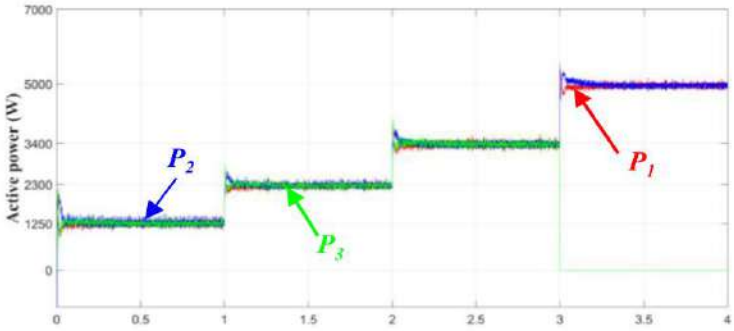


Fig. 3.16: Output active power of the three DG units

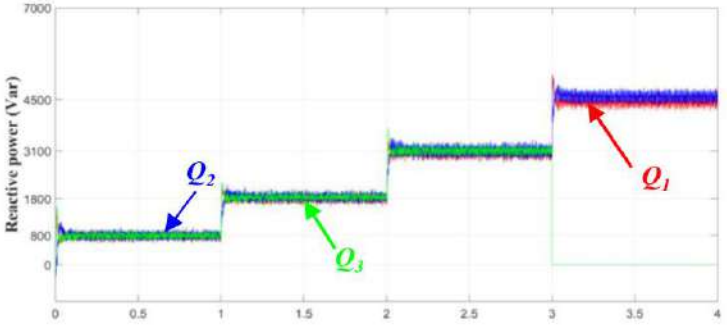


Fig. 3.17: Output reactive power of the three DG units

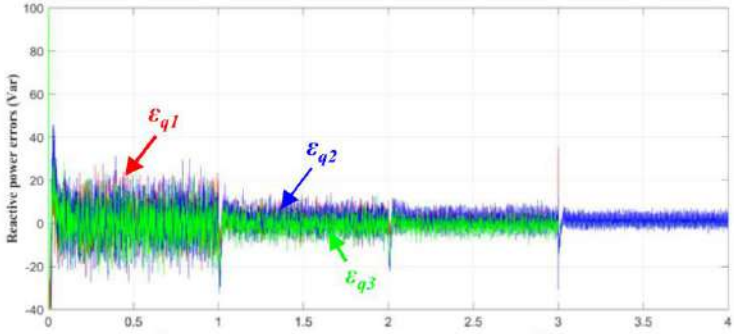


Fig. 3.18: Absolute value of the reactive-power sharing errors

Reactive-power sharing errors	Stage 1	Stage 2	Stage 3	Stage 4
ε_{q1}(%)	4	3	2	2
ε_{q2}(%)	3	3	2	2
ε_{q3}(%)	1.5	0.5	0	/

Table. 3.3: Absolute values of the reactive power sharing errors

Figs. 3.19 and 3.20, respectively, show the first phase line currents with their zooms in the four stages, as well as the circulating currents of the three DG units. These figures demonstrate how the virtual impedance-based droop control method mitigates the impact of line impedance mismatch, enabling the overall control of the IMG to achieve line current equalization between the three DG units. This, in turn, reduces the peak values of the circulating current between the three DG units in the four stages. The peak values of the circulating currents escalate imperceptibly as the load power demand increases.

Table 3.4 lists the peak values of the circulating currents during the four stages. However, examining these circulating current peak values reveals that the virtual impedance-based droop control method fails to deliver satisfactory circulating current performance, especially after the first stage.

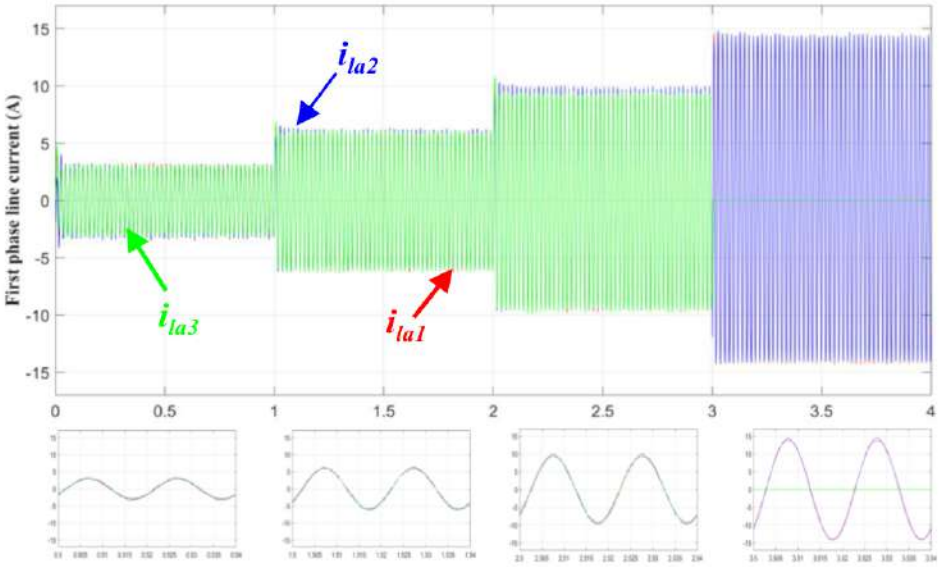


Fig. 3.19: First-phase line current of the three DG units and their zooms in the four stages

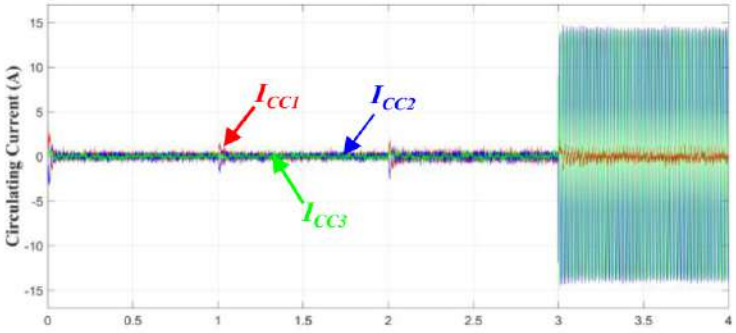


Fig. 3.20: Circulating currents

Peak values of the circulating currents	Stage 1	Stage 2	Stage 3	Stage 4
I_{cc1}(A)	1	1.2	1.4	2
$I_{cc\ 2}$(A)	1	0.9	1	/
$I_{cc\ 3}$(A)	0.6	0.6	0.8	/

Table. 3.4: Peak values of the circulating currents

Figs. 3.21 and 3.22, respectively, display the RMS voltage values of the IMG and the output of the three DGs. These figures show that both voltages follow the same profile, with a maximal IMG voltage drop that does not surpass the system regulations.

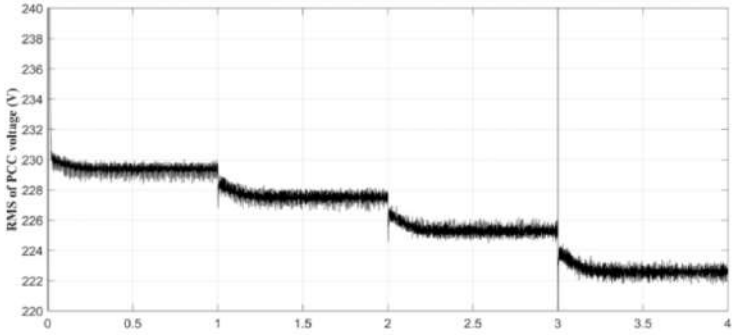


Fig. 3.21: RMS voltage of IMG

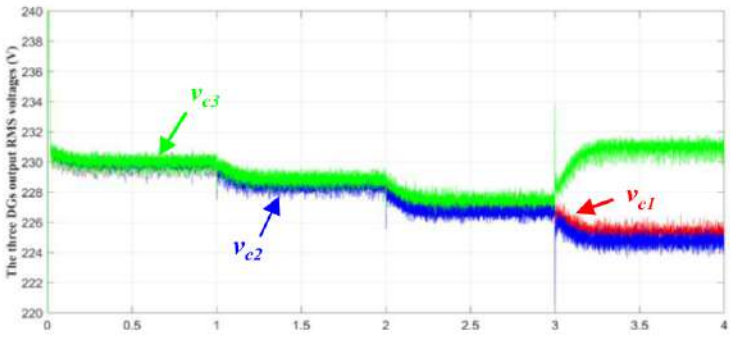


Fig. 3.22: Output RMS voltage of the three DGs

The test results indicate that the fixed virtual complex impedance-based droop control method improves power sharing, suppresses circulating current, and reduces reactive power sharing errors when compared to the traditional droop control method. However, it fails to deliver satisfactory performance during load changes because the virtual resistance and inductance values are not suitable in this case, which are challenging to calculate in such cases.

In order to address the difficulties posed by the virtual complex impedance-based droop control method that relies on its fixed parameters, and to further enhance reactive power sharing accuracy, circulating currant elimination, and reduction of power oscillations, the following subsection introduces an adaptive virtual complex impedance-based droop control method.

3.8. Proposed adaptive virtual complex impedance-based droop control method

One of the primary objectives of using virtual impedance is to ensure accurate reactive power sharing among DG units. However, without an adaptive term, the system cannot adjust for real-time variations in reactive power output and voltage conditions. This rigidity leads to persistent errors in reactive power sharing, which not only affects the efficiency of the IMG but also its ability to maintain balanced power flows.

Adaptive virtual impedance is an advanced control technique crucial for modern microgrid operation [72]. It addresses the limitations of traditional impedance matching methods by dynamically adjusting the virtual impedance of DG units to improve reactive power sharing accuracy and voltage stability. This is achieved by incorporating real-time local measurements of each DG unit's output reactive power and voltage amplitude into a formula with an adaptive coefficient. The calculated adaptive virtual impedance effectively modifies the equivalent line impedance seen by each unit, compensating for mismatches that can negatively impact power sharing and IMG stability. By enhancing reactive power sharing and mitigating line impedance mismatches without requiring communication infrastructure, this locally implemented approach enables more reliable, efficient and optimized IMG control compared to other methods. Adaptive virtual impedance control thus represents a critical strategy for addressing impedance mismatch challenges in the pursuit of stable and high-performance IMG operation. This method can dynamically adjust the virtual impedance based on real-time local measurements of the DG output reactive power (Q_i) and voltage amplitude (V_{cmaxi}). The adaptive term of the virtual impedance is given by:

$$\Delta Z_{viri} = \Delta R_{viri} + j\omega \Delta L_{viri} \tag{3.30}$$

According to this equation, the adaptive virtual impedance can be expressed as:

$$Z_{viri} = (R_{vi} - \Delta R_{viri}) + j\omega(L_{vi} + \Delta L_{viri}) \tag{3.31}$$

In order to eliminate the reactive power sharing error, the virtual resistive and inductive terms (ΔL_{vir} and ΔR_{vir}) are adaptively tuned as a function of the DG output reactive power and voltage amplitude as in the following equations:

$$\Delta L_{viri} = k_{vL} \frac{Q_i}{V_{c\max i}} \tag{3.32}$$

$$\Delta R_{viri} = k_{vR} \frac{Q_i}{V_{c\max i}} \tag{3.33}$$

The coefficients k_{vL} and k_{vR} represent the adaptive virtual resistive and inductive terms' coefficients, respectively. ΔR_{vir} is oppositely tuned against the reactive power sharing error due to the counter impact between P and Q in the IMG with complex line impedance. The virtual resistive term can adjust the damping resistance to ensures accurate active power sharing during the transient and the steady state, as well as reducing the power oscillations by damping the resonant frequency caused by the LC filter and system resonances [73].

The drop voltages across the adaptive virtual impedance in each DG are given in the dq reference frame as follows:

$$\begin{cases} v_{virdi} = (R_{vi} - \Delta R_{vir}) i_{ldi} + (L_{vi} + \Delta L_{vir}) \dfrac{di_{ldi}}{dt} - \omega(L_{vi} + \Delta L_{vir}) i_{lqi} \\ v_{virqi} = (R_{vi} - \Delta R_{vir}) i_{lqi} + L_{viri} \dfrac{di_{lqi}}{dt} + \omega(L_{vi} + \Delta L_{vir}) i_{ldi} \end{cases} \tag{3.34}$$

The adaptive virtual complex impedance with their drop voltages in each DG are implemented in the dq reference frame as shown in Fig. 3.23.

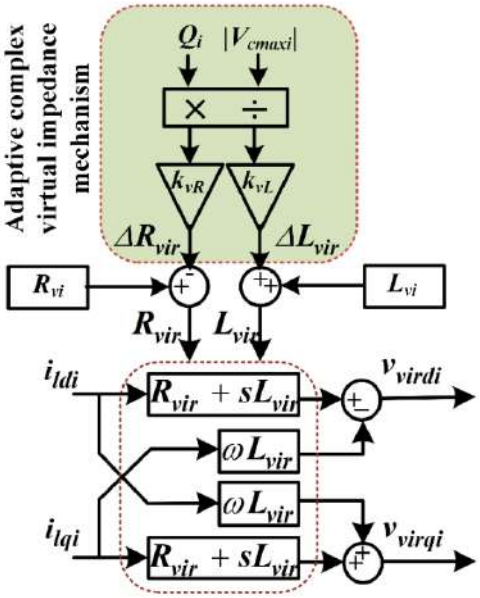


Fig. 3.23: Block diagram of the drop voltages across the adaptive virtual complex impedance in the dq reference frame

The new voltage references are obtained by subtracting the drop voltage across the virtual impedance from the output voltage references obtained from the droop control loop in equation (3.15) as follows:

$$\begin{cases} v_{crefdi} = v^{*}_{cdi} - R_{viri} i_{ldi} - L_{viri} \dfrac{di_{ldi}}{dt} + \omega L_{viri} i_{lqi} \\ v_{crefqi} = v^{*}_{cqi} - R_{viri} i_{lqi} - L_{viri} \dfrac{di_{lqi}}{dt} - \omega L_{viri} i_{ldi} \end{cases} \tag{3.35}$$

The schematic diagram of the adaptive CVI-based droop control method-based IMG is shown in Fig. 3.24.

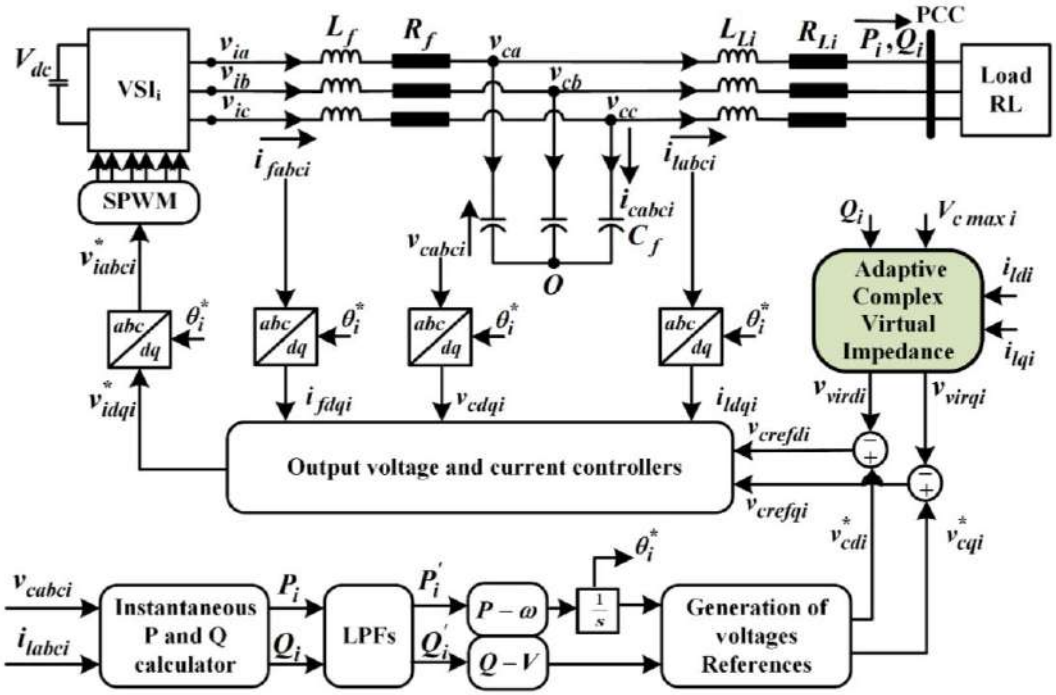


Fig. 3.24: Block diagram of three three-phase VSI based DG of an IMG with adaptive virtual complex impedance-based droop control method

3.9. Simulation results of the proposed adaptive virtual complex impedance-based droop control method

To verify the performance of the proposed adaptive virtual complex impedance-based droop control method for the IMG, a simulation test was performed using MATLAB/Simulink based on the block diagram shown in Fig. 3.24 with the same parameters and loads that adopted in previous sections (see Tables A.1 and A.2 in Appendix A). The obtained simulation results are shown in Fig. 3.25 to Fig. 3.31.

Figs. 3.25 and 3.26 show that the adaptive virtual complex impedance-based droop control method focuses primarily on improving reactive power sharing, but its benefits extend to active power sharing as well. The proposed method improves reactive power sharing by dynamically adjusting the resistive and reactive terms of the virtual impedance based on real-time local measurements, ensuring accurate and balanced power sharing in the four stages, as well as can perfectly reduce the power oscillations, as shown in Figs. 3.25 and 3.26. Also, these figures demonstrate that the proposed method increases system robustness and flexibility, allowing effective response to varying operational conditions and minimizing power losses and inefficiencies. Overall,

it fosters a more reliable, flexible, and efficient IMG operation, improving both the stability of the IMG and quality of the power supply.

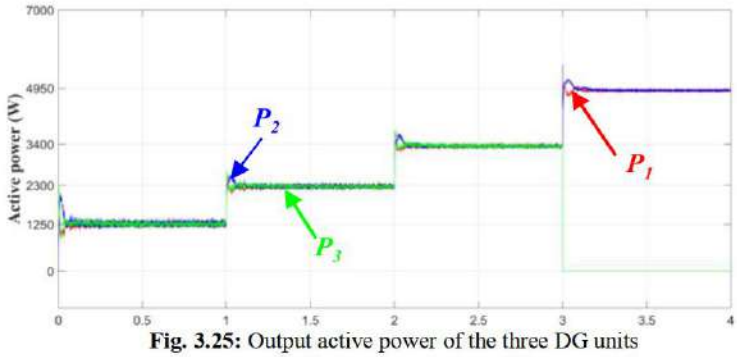


Fig. 3.25: Output active power of the three DG units

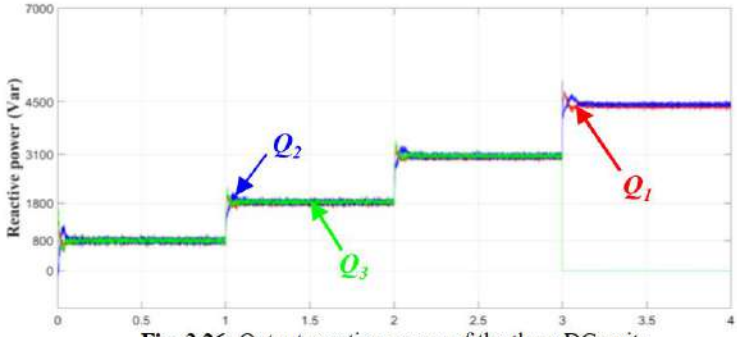


Fig. 3.26: Output reactive power of the three DG units

Fig. 3.27 shows a significant reduction in reactive power sharing errors because of the adaptive nature of the proposed method, which addresses the inaccuracies observed with fixed virtual complex impedance-based droop control method. By continuously tuning the virtual impedance to match real-time conditions, the system minimizes reactive power sharing errors during the four stages, as shown in Table 3.3.

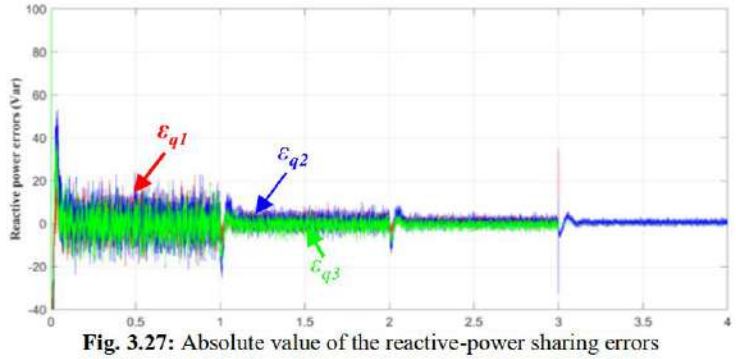


Fig. 3.27: Absolute value of the reactive-power sharing errors

Reactive-power sharing errors	Stage 1	Stage 2	Stage 3	Stage 4
ε_{q1}(%)	0	0	0	0
ε_{q2}(%)	0	0	0	0
ε_{q3}(%)	0	0	0	/

Table. 3.5: Absolute values of the reactive power sharing errors

Figs. 3.28 and 3.29, respectively, show the first phase line currents with their zooms in the four stages, as well as the circulating currents of the three DG units. The figures show how the adaptive virtual complex impedance-based droop control method makes the flow of current more stable and efficient. Additionally, it

reduces the impact of line impedance mismatch, enabling more effective control of the IMG and equalizing the line currents among the three DG units (Fig. 3.28). This, in turn, minimizes the differences that cause circulating currents, which reduce the peak values of the circulating current between the three DG units in the four stages as shown in Table 3.4.

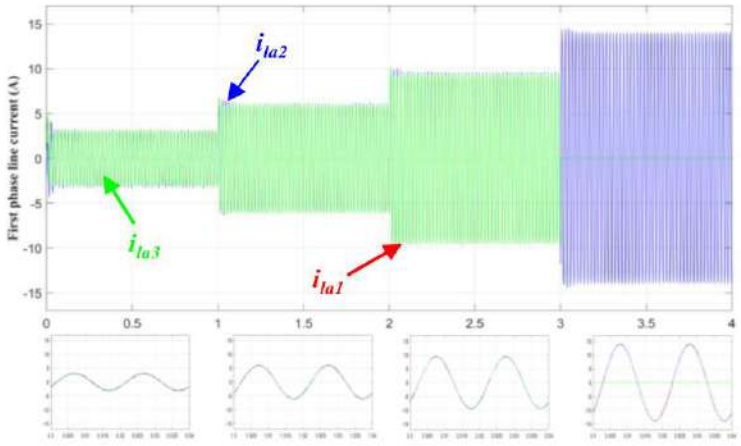


Fig. 3.28: First-phase line current of the three DG units and their zooms in the four stages

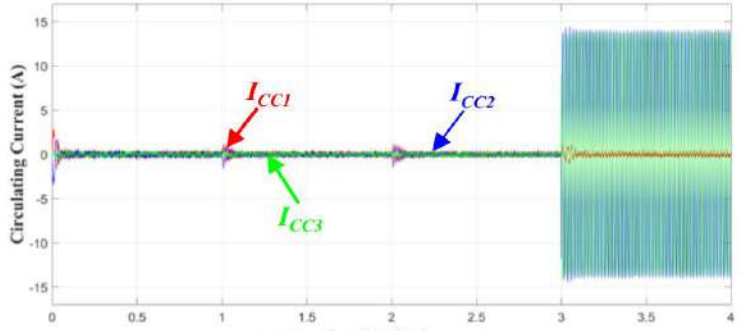


Fig. 3.29: The circulating currents

Peak values of the circulating currents	Stage 1	Stage 2	Stage 3	Stage 4
I_{cc1}(A)	0.7	0.7	0.8	1
$I_{cc\ 2}$(A)	0.6	0.6	0.7	/
$I_{cc\ 3}$(A)	0.3	0.4	0.4	/

Table. 3.6: Peak values of the circulating currents

Figs. 3.21 and 3.22, respectively, display the RMS voltage values of the IMG and the output of the three DGs. These figures show that both voltages follow the same profile, with a maximal IMG voltage drop that does not surpass the system regulations. This shows that the proposed adaptive impedance-based droop control method has a very small effect on the IMG voltage and does not cause any deviation.

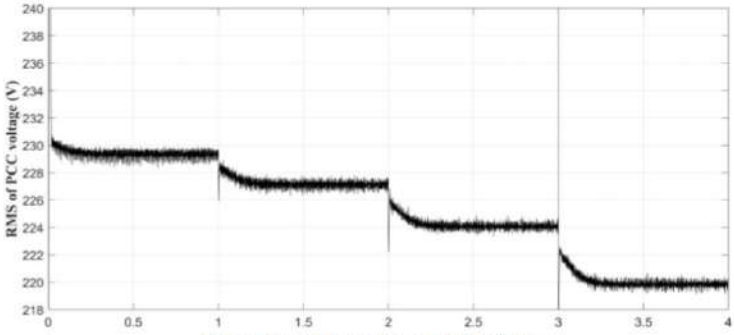


Fig. 3.30: RMS voltage of the IMG

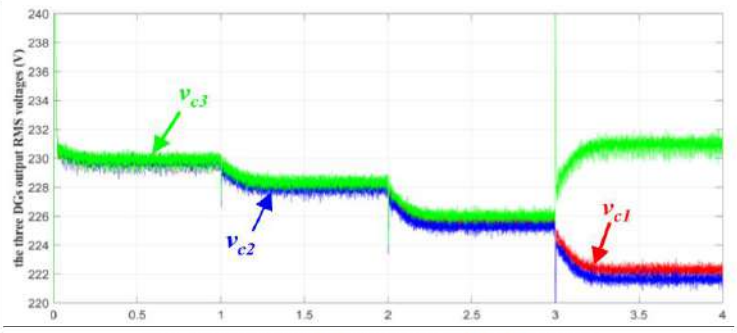


Fig. 3.31: Output RMS voltage of the three DGs

3.10. Conclusion

This chapter reports the IMG control methods based on the concepts of the traditional droop control method, the virtual complex impedance-based droop control method, and an adaptive virtual complex impedance-based droop control method. The power model of the IMG is established, the reactive power sharing errors are analyzed, and the concepts of the three control methods in the dq reference frame are also established. After a brief introduction to the IMG, the first part of this chapter focuses on the IMG system description and the design of the traditional droop control method.

The second part of this chapter talks about how to use the virtual complex impedance-based droop control method to get rid of problems like inaccurate power sharing, power coupling, power overshoot, power oscillations, and circulating currents that happen with the traditional droop control method. Simulation results using MATLAB/Simulink confirm that the virtual impedance-based droop control method is completely possible for controlling the three parallel VSI-based DG units of the IMG. The method enhances power sharing, eliminates power overshoot, and eliminates circulating current in situations where line impedances are mismatched. However, the results obtained from this method demonstrate that any change in the IMG's structure, such as a change in load, swiftly erases these performances. There is one problem with this method: it can only use the resistive and inductive values that were chosen for the ideal IMG scenario. This means that it can't adapt to any changes in the structure of the system.

In order to address this issue and improve the performance of the IMG, an adaptive virtual complex impedance-based droop control method based on the output reactive power and voltage amplitude of each DG unit is applied in the third part of this chapter. The method's results significantly enhance the control

performances of the IMG. The system shares the active and reactive powers equally with few oscillations. It also gets rid of the three DG units' reactive power errors and stops the circulating currents completely.

Chapter 4

Validation of the proposed control method via Hardware-In-the-Loop (HIL) real-time simulations using OPAL RT OP5700

4.1. Introduction:

Hardware-in-the-Loop (HIL) real-time simulation is a powerful technique that has gained significant importance in the development and validation of complex systems, particularly in the field of power systems and microgrids. It provides a versatile and cost-effective approach to testing and refining control algorithms, software components, and system models before deploying them on actual hardware or in real-world environments [02].

In the context of microgrids, HIL real-time simulation plays a crucial role in the design, evaluation, and optimization of various control strategies, energy management algorithms, and protection schemes. It allows researchers and engineers to simulate the behavior of the entire microgrid system, including distributed energy resources, energy storage systems, power electronic converters, and loads, in a virtual environment that accurately replicates real-time dynamics [74, 75].

The HIL real time simulation setup typically consists of a real-time digital simulator (RTDS) or a powerful computing platform capable of executing complex microgrid models and control algorithms in real-time. Within this simulation environment, the control software or algorithm under development is integrated and tested against the simulated microgrid model, enabling comprehensive evaluation and refinement of the software's performance under various operating conditions and fault scenarios.

By leveraging HIL real-time simulation, researchers and engineers can:

1. Develop and test advanced control strategies for microgrids, such as energy management systems, power flow control, and protection schemes, in a safe and controlled virtual environment.
2. Evaluate the performance and robustness of control algorithms under various scenarios, including renewable energy fluctuations, load changes, and different microgrid configurations.
3. Optimize control parameters and fine-tune algorithms based on simulation results, reducing the need for costly hardware prototyping and field trials.
4. Investigate the impact of communication delays, data losses, and other real-time constraints on the performance of control algorithms, enabling the development of more robust and resilient solutions.
5. Facilitate the integration and testing of multiple software components, such as energy management systems, protection relays, and data acquisition systems, within a unified simulation environment.

HIL real-time simulation is particularly valuable for the development and validation of microgrid control systems, as it allows for extensive testing and refinement of software components before deploying them on actual hardware platforms or in real-world microgrids. This approach reduces the risk of failures, ensures reliable operation, and accelerates the development cycle, ultimately contributing to the widespread adoption of resilient and sustainable microgrid solutions.

4.2. Devices-based SIL real-time simulations

In SIL real-time simulation for power systems and microgrids, various devices and components are typically used to create the simulation environment. The key devices involved in SIL real-time simulation include [76]-[78]:

4.2.1. Real-Time Digital Simulator (RTDS)

- RTDS is a powerful and widely used real-time simulation platform specifically designed for power systems and microgrids.
- It consists of modular hardware components, such as processor cards, input/output (I/O) cards, and communication interfaces, that work together to execute complex power system models in real-time.
- RTDS provides a high-fidelity simulation environment capable of modeling various components like generators, motors, power electronic converters, and control systems.

4.2.2. Industrial-grade Computing Platforms

- In some cases, instead of dedicated RTDS hardware, industrial-grade computing platforms with high computational power and real-time operating systems (RTOS) are used for SIL simulations.
- Examples include PC-based systems with multi-core processors, field-programmable gate arrays (FPGAs), or specialized real-time computers from vendors like National Instruments (NI) or dSPACE.
- These platforms run real-time simulation software, such as MATLAB/Simulink Real-Time or LabVIEW Real-Time, to execute the microgrid models and control algorithms.

4.2.3. Simulation Software

- Various simulation software tools are used to model and simulate the microgrid components, control algorithms, and power system dynamics.
- Examples include MATLAB/Simulink, PSCAD, PSLF, DigSILENT PowerFactory, and RTDS Software.
- These software tools provide libraries of pre-built component models, as well as the ability to create custom models using programming languages or graphical block diagrams.

4.2.4. Human-Machine Interface (HMI)

- HMIs, such as touchscreen displays, control panels, or dedicated software interfaces, are used to interact with the SIL simulation environment.
- They allow researchers and engineers to monitor and control the simulation parameters, visualize system outputs, and introduce disturbances or faults for testing purposes.

4.2.5. Data Acquisition and Communication Interfaces

- Data acquisition devices, such as analog-to-digital converters (ADCs) and digital input/output (I/O) modules, are used to interface the simulation environment with external hardware or control systems.
- Communication interfaces, such as Ethernet, serial ports, or fieldbus protocols (e.g., Modbus, CAN), enable the exchange of data between the simulation platform and external devices or control systems.

4.2.6. Signal Conditioning and Amplification Devices

In some cases, signal conditioning and amplification devices may be required to interface the simulation platform with external hardware or control systems operating at different voltage or current levels.

These devices and components work together to create a comprehensive SIL real-time simulation environment, enabling researchers and engineers to develop, test, and validate control algorithms, energy management strategies, and protection schemes for microgrids before deploying them in real-world systems.

4.3. Types of Real-Time Digital Simulators

RTDSs are specialized hardware platforms designed specifically for real-time simulation of power systems and related applications. Several vendors offer RTDS solutions, each with their own unique features and capabilities. Here are some of the main types of RTDS available on the market [77, 78]:

4.3.1. RTDS Technologies

RTDS Technologies is a leading provider of real-time power system simulation solutions. Their flagship product, the RTDS Simulator that comprises modular hardware like processor cards, I/O cards, and communication interfaces. Widely used in academia, research, and industry, the RTDS simulator enables microgrid simulation, hardware-in-the-loop (HIL) testing, and power system studies. With its high-fidelity simulation capabilities, it allows accurate modeling, control strategy testing, and performance validation of complex power systems under realistic conditions.

4.3.2. OPAL-RT Technologies

OPAL-RT Technologies provides real-time simulation solutions for motor control and power system applications, including microgrid simulations, such as the OP4510 and OP5707 RTDS platforms. Their solutions are often used with MATLAB/Simulink for model development and real-time execution. This integration allows for comprehensive testing, validation, and optimization of microgrid control strategies and system integration before practical deployment.

4.3.3. Typhoon HIL

Typhoon HIL is a company specializing in HIL testing solutions for power electronics and power systems. Typhoon HIL designs their RTDS products, such as the HIL402 and HIL604, for power converter testing, microgrid simulations, and other power system applications. They are known for their high-fidelity simulations and ability to work with a wide range of software tools. Typhoon HIL solutions let you test power electronic parts, control algorithms, and system integration in a simulated environment before practical deployment.

4.3.4. Triphase

Triphase provides real-time simulation solutions for power systems, including microgrids, and renewable energy applications. Triphase designs their RTDS platforms, such as the PM1000 and PM4000, for hardware-in-the-loop testing, controller validation, and power system studies. Research and development projects related to microgrid control and grid integration widely utilize Triphase solutions, which facilitate high-fidelity simulations, control algorithm testing, and system validation prior to practical deployment.

4.3.5. dSPACE

dSPACE is a renowned company specializing in real-time simulation solutions for power electronics and power systems. Power system applications commonly use dSPACE's RTDS platforms, like the DS1007 and DS1006, for HIL testing, rapid control prototyping, and model-based design. Before real-world deployment, dSPACE's solutions enable high-fidelity simulations, validate control algorithms, and conduct system integration testing.

These are just a few examples of the various RTDS vendors and platforms available on the market. The choice of RTDS solution often depends on factors such as the specific application requirements, budget, integration with existing software tools, and the desired level of fidelity and flexibility in the simulations. In this chapter we use the OP5700 RTDS platform to validate the performance of the proposed adaptive complex virtual impedance-based droop control for IMG. It is the entry level simulator from OPAL-RT, it is a FPGA and Intel based simulator [79].

4.4. OPAL-RT OP5700 real-time simulator

To validate the results obtained as part of this master thesis, we used the OP5700 real-time simulator. Even without a physical prototype, digital real-time simulation (DRTS) is more rigorous and representative of actual behavior. This simulator offers several advantages; the ability to

simulate MATLAB/Simulink models is one of its key strengths. You can easily convert and compile a Simulink model without rewriting code by making some modifications and adding new blocks. We have developed several Simulink blocks to facilitate interfacing with the most commonly used I/O cards. The simulator heavily relies on existing communication technologies such as TCP/IP, UDP, and FireWire, which are known and reliable technologies, ensuring system flexibility. The simulator's substantial computing power allows for the simulation of complex models in small time steps.

There are two components to the OPAL-RT OP5700 simulator, as shown in **Fig. 4.1**. The software-containing Host Station (Modeling environment) component enables you to manage the simulation, communicate with the simulated system, and observe the results. The second component, known as the target station (real-time simulator), comprises a supercomputer with up to 64 cores, modulated by digital, analogy, and I/O cards, along with FPGA and analogy-digital converter modules. The model to be simulated will be in this second section will contain the simulated model, which can be linked to a real prototype. Real-time operating systems, such as RedHat or QNX, power target computer stations [80].

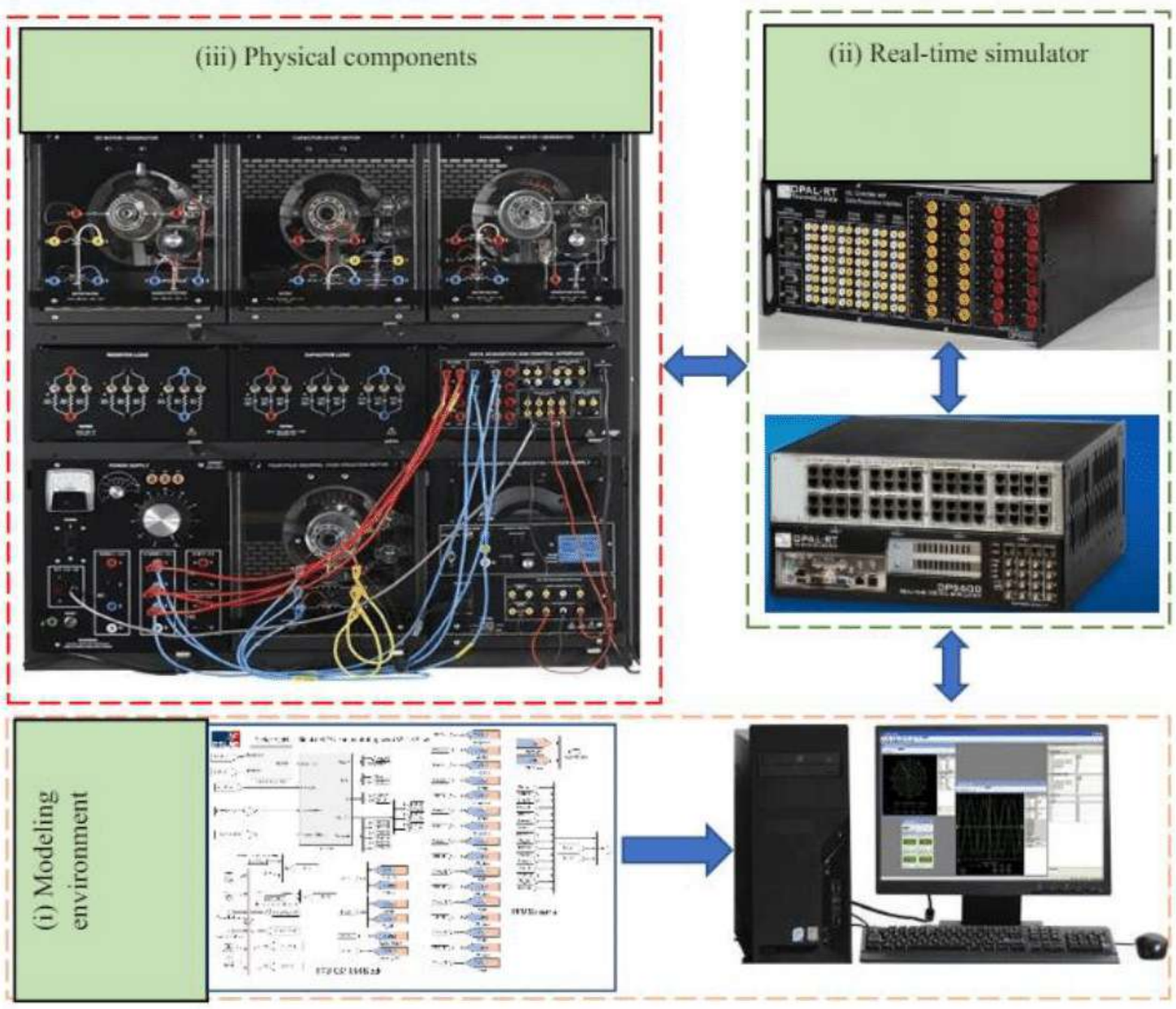


Fig. 4.1: Communication protocol of the interfaces

4.4.1. OPAL-RT properties with RT-LAB OP5700 and HIL controller OP8660

4.4.1.1. Overview of OP5700

The OP5700 is a versatile, powerful system designed to meet complex simulation needs. It integrates seamlessly with OPAL-RT's RT-LAB software to enable real-time simulation of various engineering systems, providing an essential tool for researchers and engineers.

Fig. 4.2: Picture of OPAL-RT OP5700

4.4.1.2. Architecture of the OP5700 [81]

The OP5700 is a complete simulation system. It contains a powerful target computer, a high-end reconfigurable FPGA, signal conditioning for up to 256 I/O lines and 16 high-speed fiber-optic SFP ports. The design makes it easy to use with standard connectors (DB37, RJ45 and mini-BNC) without the need for input/output adaptors and allows quick connections for monitoring I/O signals. It is designed to be used either as a desktop, shelf top, or mounted in a standard 19'' rack.

The front of the chassis allows for access to monitoring interfaces, connections, and SFP sockets. Conversely, the rear of the chassis allows for access to the standard connectors, I/O connectors, power cable, and main power switch of the target computer.

Inside, the main housing is divided into two portions, as shown in Fig. 4.3, each with a specific purpose:

The bottom portion of the chassis houses the target computer, which can be integrated into a network of simulators or operated independently. This target computer, utilized for executing simulations created with OPAL-RT's RT-LAB or HYPERSIM software, features an ATX motherboard, a Linux-based real-time operating system, an Intel Xeon E5 CPU with 4, 8, 16 and 32 processor cores up to 3.2GHz, 10MB Cache Memory per 4 cores, up to 32GB of DRAM, a 512GB SSD disk, and 6 PCIe slots used to connect the internal FPGA board and PCIe or PCI third party I/O and communication cards.

The top portion of the chassis houses the FPGA and the I/O conditioning modules. It features a Xilinx Virtex 7 FPGA programmable from the target computer via PCIe, which is used to execute models designed with the OPAL-RT RT-XSG tool, manage the I/O lines, and execute embedded FPGA-based simulations by exchanging data with the real-time simulations running on the target computer CPUs via the PCIe link. It also includes a flat carrier board capable of connecting any combination of up to 8 digital and analog conditioning modules, with each module controlling 16 or 32 lines for a total of up to 256 I/O lines, as well as 16 SFP ports for high-speed communication with other FPGA-based systems or with external devices.

The standard communication protocols available with the OP5707 are based on Xilinx® Aurora (1 to 5 Gbps). Other protocols, such as the Gigabit Ethernet, can also be implemented.

These SFP ports can be used to expand the simulator's I/O capability using OPAL-RT's Multi-System Expansion link (MUSE)2: each port can be connected to one OPAL-RT remote I/O unit (OP4520, OP5607 or OP4200), effectively increasing the simulator I/O capability to a maximum of 4096 channels. SFP ports not used for MUSE remain compatible with the legacy Generic Aurora link. The MUSE link is compatible with OPAL-RT boards I/O management architecture.

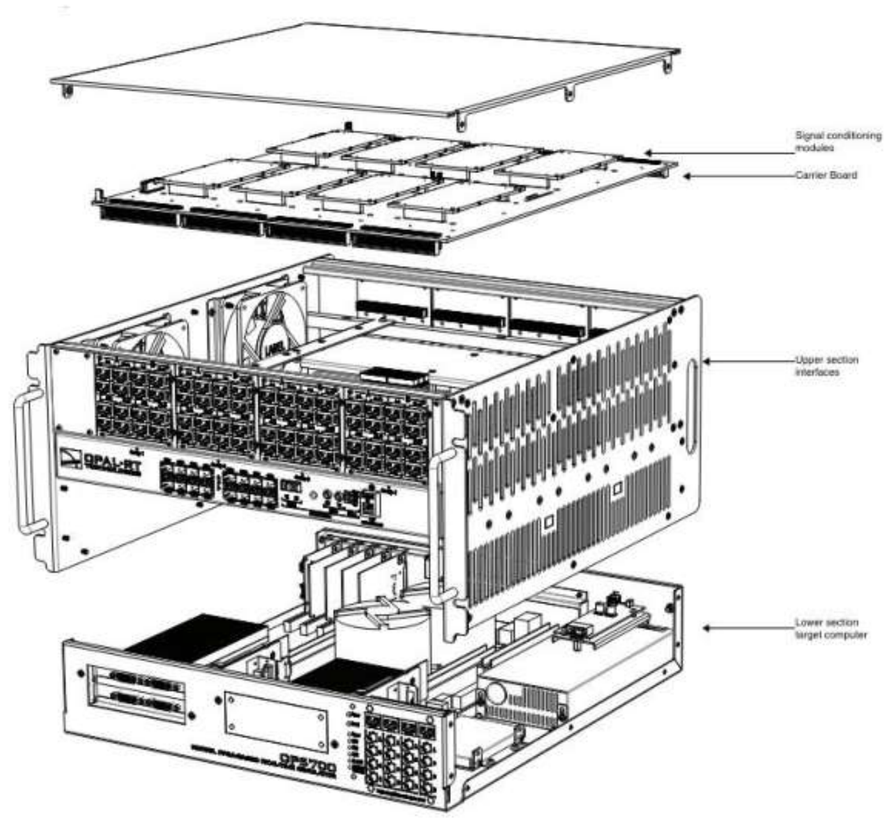


Fig. 4.3: Architecture of the OP5700 simulator

The OP5700 real-time simulator is designed with a comprehensive array of front and rear connectors to ensure robust connectivity and ease of use. These connectors facilitate interaction with various external devices, ensuring that the OP5700 can be effectively integrated into a wide range of simulation and testing environments.

4.4.1.2.1. Front Connectors of OP5700

The OP5700 system's front panel structure is shown in Fig. 4.4.

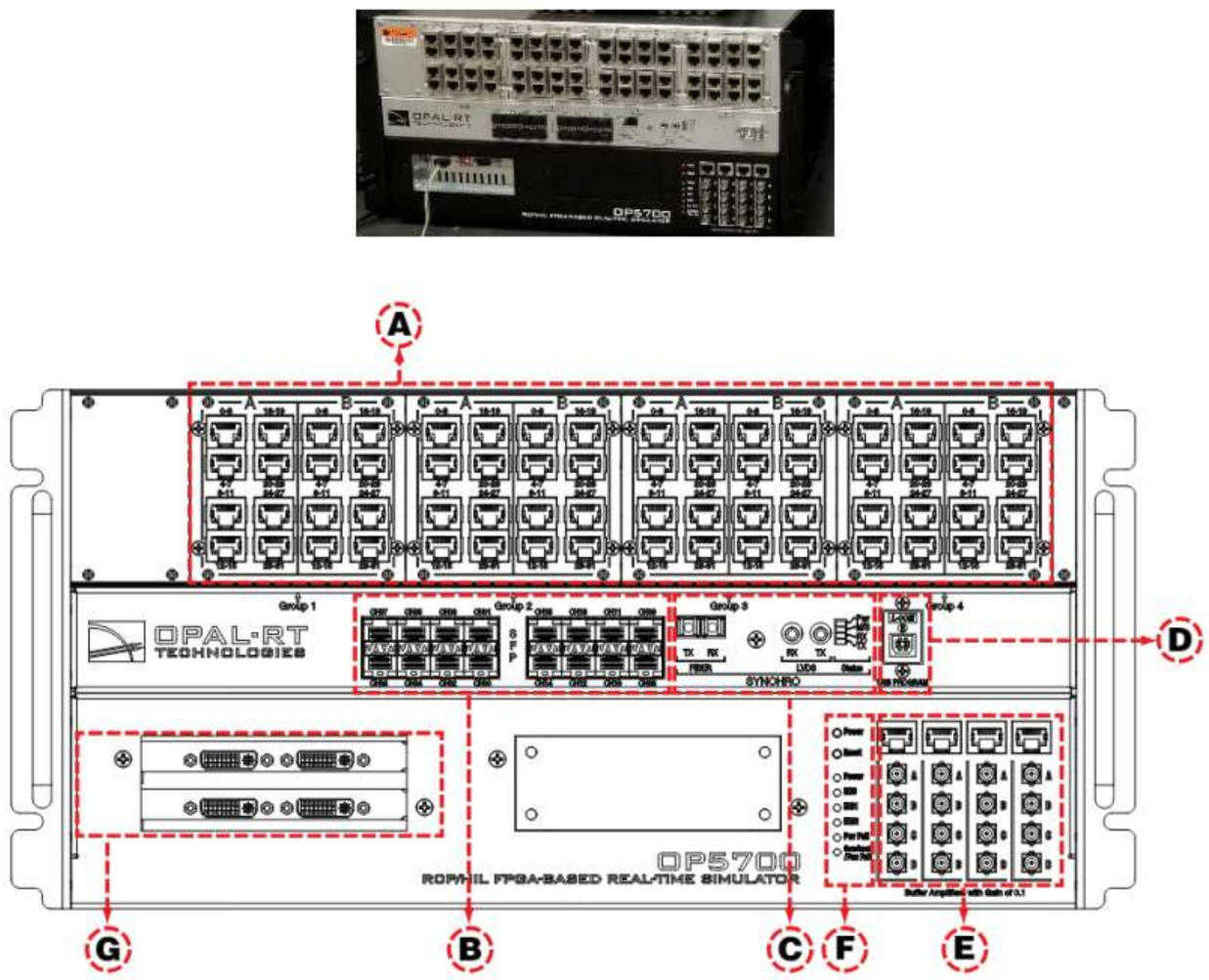


Fig. 4.4: Front panel structure of OP5700 simulator

The OP5700 simulator's front panel is equipped with various connectors designed to facilitate high-speed communication, monitoring, and synchronization. These connectors include:

A. RJ45 Connector Panels: These provide connections for monitoring signals from mezzanine I/O boards. Each RJ45 connector is linked to the front and back mezzanines on the carrier board. For analog mezzanines, channels 0-15 use the first column of connectors, while digital mezzanines

utilize both columns, covering channels 0-15 in the first column and channels 16-31 in the second column.

B. 16 SFP Ports: These small form-factor pluggable ports are controlled by the FPGA, enabling high-speed communication with other simulator FPGAs or third-party devices. Each SFP socket controls one communication link. The SFP transceivers and optical fiber cables should be selected based on the type and speed of the communication protocol implemented in the FPGA. For MUSE link, specific SFP and cable types are required.

C. Synchronization Connectors (SYNCHRO): This includes fiber optic and audio synchronization connectors, along with a series of four LEDs on the front panel to display the device status. These LEDs indicate the status of synchronization transmission (Tx), reception (Rx), master/slave mode (M/S), and power (PWR).

D. USB Connector for JTAG Programming: This USB port is used for JTAG programming in the event of lost or damaged FPGA configuration, providing an essential interface for maintenance and updates.

E. Monitoring RJ45 Connectors with Mini-BNC Terminals: These connectors allow for quick connections to monitoring devices like oscilloscopes. RJ45 cables connect from a channel on the RJ45 panel to one of four RJ45 monitoring connectors. Mini-BNC connectors enable fast and easy connections to monitoring equipment.

F. Target Computer Monitoring Interface: This interface includes two push buttons for power and reset functions of the target computer, along with six LED indicators. These LEDs provide information on power status, hard disk drive activity, network port usage, power faults, and overheat/fan failure conditions.

G. LED Indicators: The LEDs associated with the SFP channels light up to indicate channel activity. Green LEDs indicate the presence and activity of SFP transceivers, while red LEDs signal transmission faults or reception loss. This comprehensive array of front panel connectors and indicators ensures that the OP5700 system can be effectively monitored and maintained, facilitating robust and high-performance simulation operations.

4.4.1.2.2. The rear Connectors of OP5700

The OP5700 system's rear panel structure is shown in Fig. 4.5.

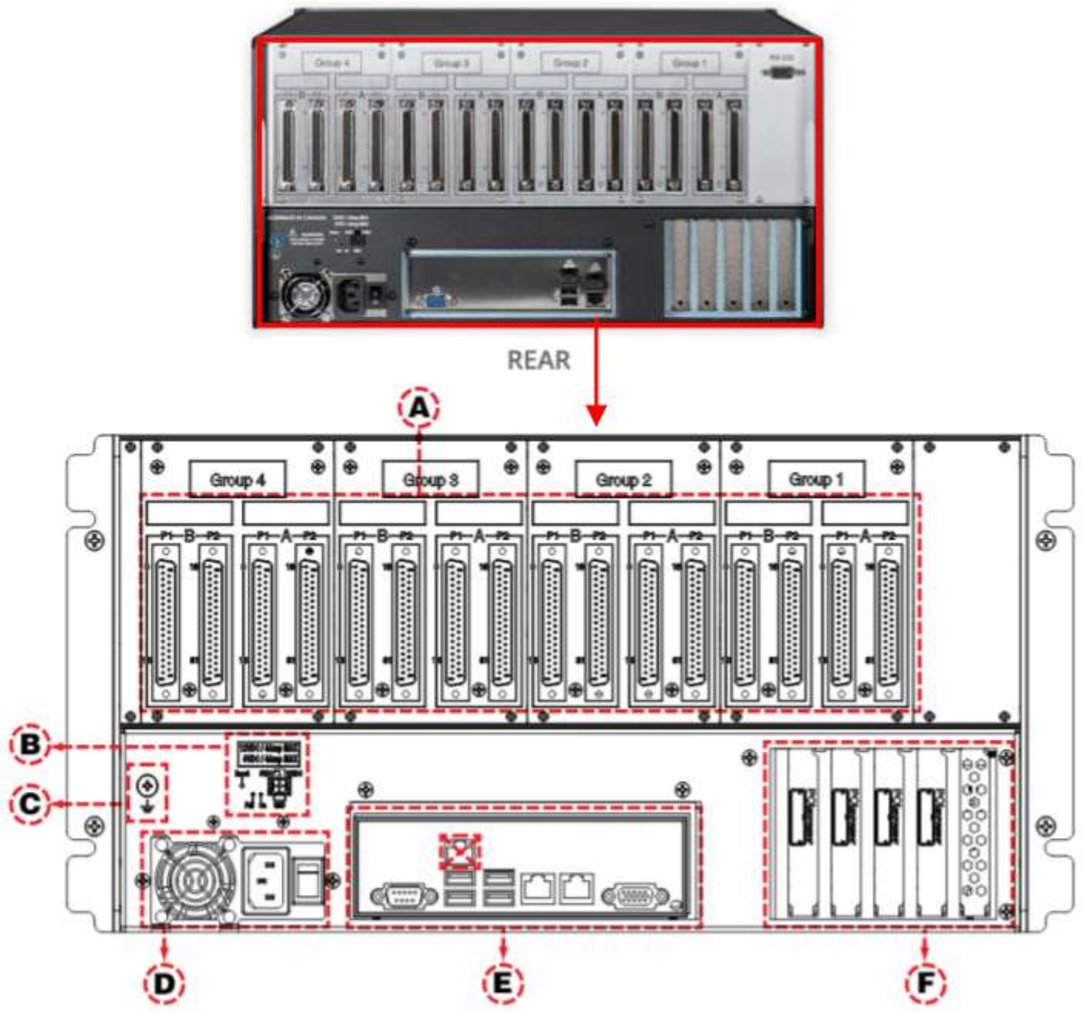


Fig. 4.5: Rear panel structure of OP5700 simulator

The rear connectors of the OP5700 simulator provide additional functionality and expandability. These connectors include:

A. **DB37F I/O Connectors**: Used for input/output operations, these connectors facilitate the integration of external devices and systems with the simulator.
B. **Power Reset and +5/+12V Power Source Connector**: This connector includes a pushbutton reset for overcurrent protection and micro fit connectors for 5V or 12V power sources, which are used for testing I/O functionality.
C. **Ground Screw**: Ensures the simulator is properly grounded to prevent EMI-related damage, enhancing the reliability and safety of the system.
D. **Power Connector and Power On/Off Switch**: Provides the main power connection to the simulator and includes a switch for turning the system on and off.
E. **Standard Computer Connectors**: These include ports for the mouse, keyboard, USB devices, monitor, and network connections, facilitating easy integration with standard computer peripherals.
F. **Low-profile PCIe Slots**: These slots provide expandability for additional PCIe cards, allowing users to enhance the simulator's capabilities with third-party I/O or communication boards.

4.4.1.3. Advantages of using OP5700 RT-LAB

High Performance: The combination of a powerful CPU and FPGA ensures that the OP5700 can handle complex simulations with high fidelity and in real time.

Scalability: With the capability to expand I/O lines and integrate with multiple systems, the OP5700 provides a scalable solution for various applications.

Ease of use: Standard connectors and user-friendly interfaces simplify the setup and operation of simulations, reducing the learning curve for new users.

Versatility: The OP5700 supports a wide range of applications, from power systems to automotive testing, making it a versatile tool for engineers across different fields.

4.4.2. Overview of OP8660 HIL controller and Data Acquisition Interface [82]

The OP8660 HIL controller is a sophisticated and versatile hardware component designed to support hardware-in-the-loop (HIL) simulations. This controller is engineered to work seamlessly with OPAL-RT's real-time simulators, such as the OP5700 series, providing advanced data acquisition, signal conditioning, and I/O capabilities essential for accurate and reliable real-time simulation and testing. The photo of the OP8660 HIL controller is shown in Fig. 4.6. It has the following features:

Fig. 4.6: OP8660 HIL controller and data acquisition interface

- **High Voltage and Current Measurements:**

The OP8660 can handle voltage measurements up to 600V and current measurements up to 15A, making it suitable for high-power applications like motor drives, power converters, and energy systems.

- **Analog and Digital I/O:**

The controller offers multiple channels for both analog and digital inputs and outputs, facilitating comprehensive system testing and enabling precise control and monitoring of various simulation parameters.

- **Encoder Inputs and Inverter Outputs:**

Specialized connectors for interfacing with motor control systems and other applications requiring precise position and speed feedback.

- **Integration with Real-Time Simulators:**

Designed to complement the OPAL-RT real-time simulators, the OP8660 enhances the overall simulation capabilities by providing robust I/O support, thereby extending the functionality and application range of the simulators.

4.4.2.1. The front panel of the OP8660

The OP8660 system's front panel structure is shown in Fig. 4.7.

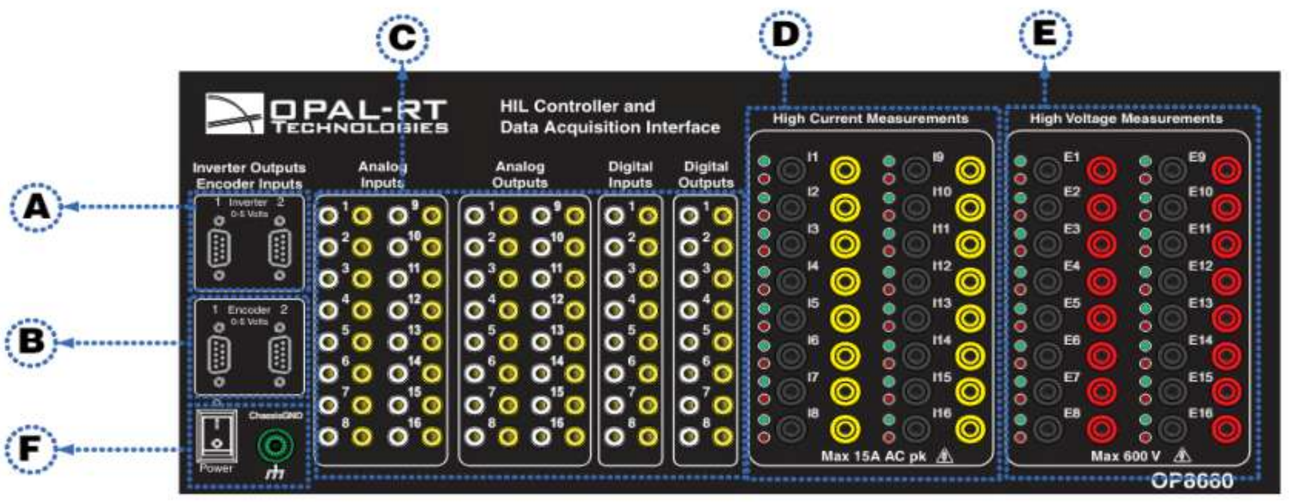


Fig. 4.7: Front panel structure of OP8660 HIL Controller

The front panel of the OP8660 HIL simulator provide additional functionality and expandability. These connectors include:

A. 6 Pulse Inverter Output (DB9 connector) - Used to send control pulses to the motor.

B. Encoder Input Connector - Reads motor speed and position using differential ABZ encoder signals.

C. Analog and Digital Input/Output Monitoring Connectors - For each channel (16 analog or 8 digital).

D. High Current Probe Connectors - Maximum 15 A AC, with red and green LEDs indicating channel activity.

E. High Voltage Probe Connectors - Maximum 600 V, with red and green LEDs indicating channel activity.

F. Power Switch and Ground Connector - For powering the device on and off and grounding.

4.4.2.2. The rear connectors of OP8660

The OP8660 system's rear panel structure is shown in Fig. 4.8.

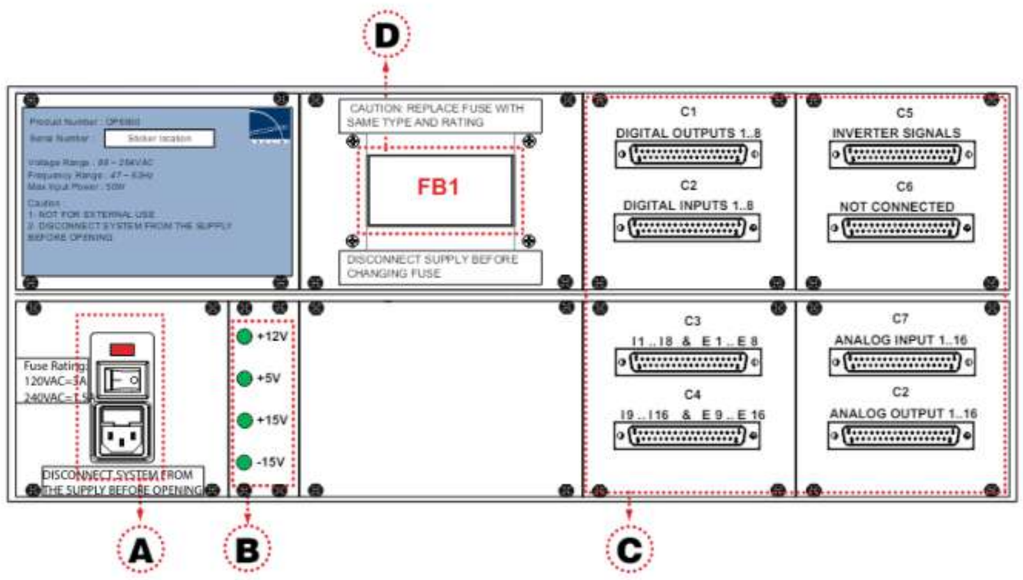


Figure 3: OP8660 rear connector panels

Fig. 4.8: Rear panel structure of OP8660 HIL Controller

The rear panel of the OP8660 includes the following connectors:

A. Power Connection Port and Switch - For connecting to the power supply and turning the device on and off.

B. Main LEDs - Indicate various power statuses:

- +12V: Indicates DC-DC power supply status.
- +5V: Indicates inverter power supply status.
- 15V: Power supply status for current and high voltage probes.
- -15V: Power supply status for current and high voltage probes.

C. DB37F I/O Connectors (C1 to C8) - For various input and output connections (refer to "Pin Assignments" for details).

D. Fuse Box - Contains the fuse for the device, with specifications and cautionary information regarding replacement.

4.5. The steps for using RT-LAB [83, 84]

The process of complete execution in RT-LAB involves several key steps. Initially, the Simulink model must be integrated into RT-LAB, necessitating modifications to regroup the model into subsystems, specifically the console subsystems (SC) and master subsystems (SM). OpComm blocks are added to these subsystems to manage communication. The SC subsystems include user interface elements like scopes and displays, while SM subsystems handle computational tasks such as mathematical operations and I/O blocks. After these modifications, RT-LAB communication protocols are configured, and the model is built and

compiled. This compiled model is then loaded onto the OP5700 real-time simulator, which executes the master subsystems. The system connects to external hardware, processes signals, and manages real-time operations. The final steps involve running the model in RT-LAB, monitoring the hardware interaction, and ultimately stopping the execution to collect and analyze results in MATLAB.

4.5.1. Grouping the Simulink model into subsystems

In the context of using OPAL-RT OP5700 RT-LAB for real-time simulation, grouping into subsystems is a critical step to manage the complexity of the model, enhance modularity, and ensure efficient simulation execution. In this process, we organize the overall model into smaller, manageable units known as subsystems, each of which represents a specific part of the simulated system. Typically, we categorize the subsystems as SM (main calculation subsystem) and SC (graphical user interface subsystem).

- **SC_ Subsystems:** handles the graphical user interface (GUI) operations. It does not perform calculations itself, but rather runs on the PC to provide a console interface for data exchange with the base station's Windows operating system. This subsystem operates asynchronously, at a lower frequency than the calculation subsystems. Its main purpose is to display information such as scopes, status indicators, constant values, and manual control switches to allow the user to monitor and interact with the system.
- **SM_Subsystems:** serves as the system's primary calculation engine and executes synchronously at the chosen calculation step rate, allowing for real-time or accelerated calculations. This subsystem handles the core mathematical logic, signal generation, input/output operations, and physical modeling required for the application. To maximize performance, the SM_subsystem uses the simulator's dedicated single CPU core for its computational workload.

4.5.1.1. Benefits of Grouping into Subsystems

- **Modularity:** Subsystems allow for a modular approach to modeling, where each part of the system can be developed, tested, and debugged independently. This modularity simplifies maintenance and updates to the model.
- **Parallel Development:** By dividing the system into subsystems, different teams can work on various parts of the model simultaneously. This parallel development can significantly reduce the overall development time.
- **Simplified Testing and Debugging:** Subsystems can be tested individually before being integrated into the complete model. This approach helps in isolating and resolving issues more effectively.
- **Resource Management:** Subsystems enable better management of computational resources. Each subsystem can be allocated specific resources, ensuring that the overall simulation runs efficiently without overloading any single component.

- **Reusability:** Once a subsystem is developed and validated, it can be reused in different projects or simulation scenarios, enhancing productivity and consistency across projects
- **Scalability:** Subsystems facilitate scalability of the model. As the system complexity grows, new subsystems can be added without disrupting the existing structure.

4.5.1.2. Creating Subsystems

In RT-LAB, subsystems are created using graphical modeling tools. Each subsystem can be represented as a block in the overall model, encapsulating its internal components and logic. As shown in Figs. 4.9 and 4.10, the model must contain only blocks grouped into subsystems. The arrangement of blocks within a single block, known as a "subsystem", allows for the following:

- Simplify the model by grouping blocks;
- Create a hierarchical diagram:
- Keep blocks functionally linked together.

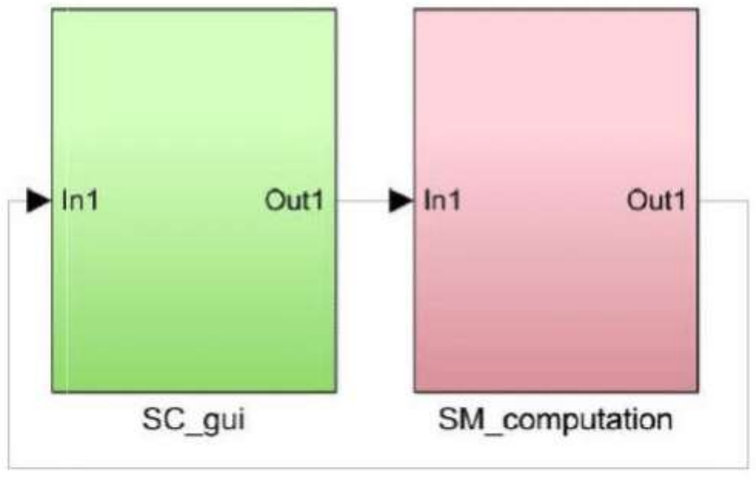


Fig. 4.9: The two main subsystems that must be contain in a model.

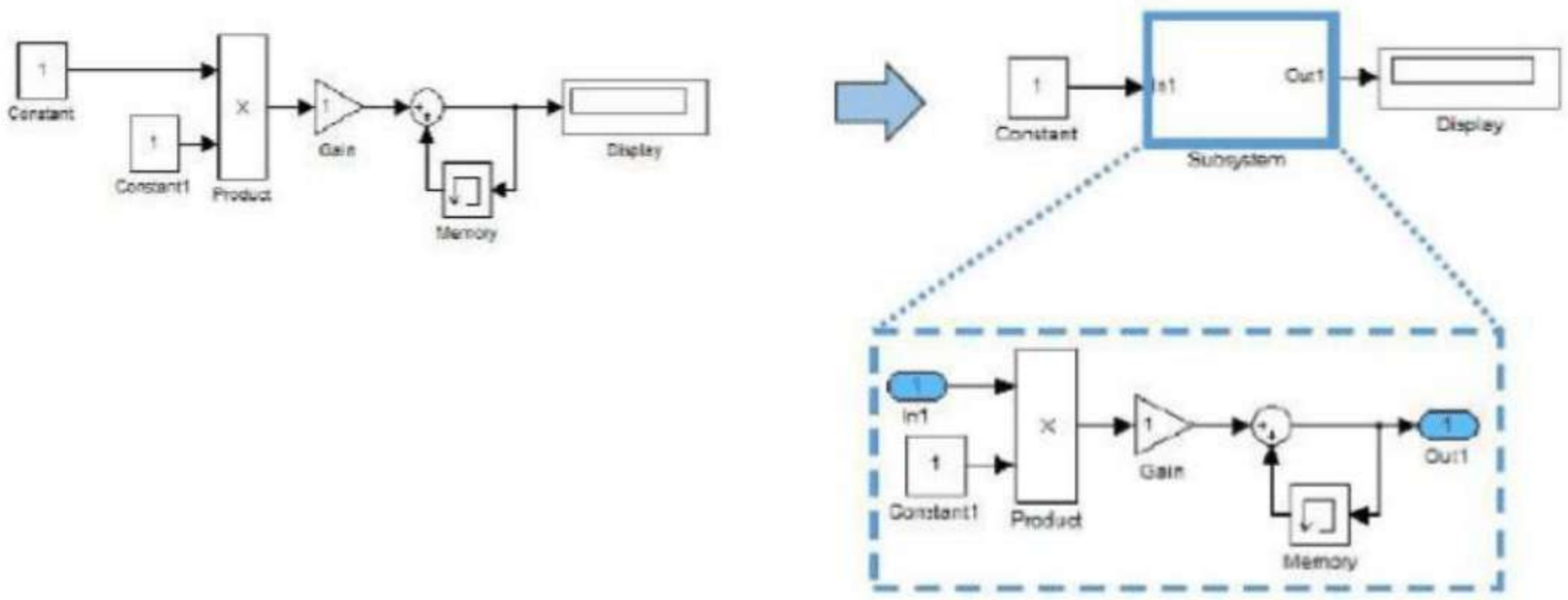


Fig. 4.10: Grouping of blocks into subsystems

4.5.1.3. Interfacing subsystems

Subsystems communicate with each other through defined interfaces. These interfaces can include signal lines, data buses, and network connections, ensuring seamless integration of the subsystems into the complete model

4.5.1.4. Mapping to hardware

Once the subsystems are defined, they are mapped to the hardware resources available. RT-LAB allows for efficient allocation of CPU cores, FPGA resources, and I/O channels to each subsystem, optimizing the simulation performance

4.5.1.5. Synchronization and coordination

RT-LAB ensures that all subsystems are synchronized and operate in a coordinated manner. This synchronization is crucial for maintaining the real-time performance of the simulation, especially in complex systems with multiple interacting subsystems.

4.5.2. Adding OpComm blocks

In RT-LAB, OpComm blocks are essential components used for communication between subsystems and for managing the data exchange in a real-time simulation environment. These blocks facilitate the transfer of signals and data between different parts of the model, ensuring synchronization and coordination across the entire simulation. The OpComm blocks are added to the Simulink model as follows:

1. Start by opening your RT-LAB model in the Simulink environment and ensure that the Simulink model is well organized, with clear definitions for each subsystem.
2. Navigate to Simulink's RT-LAB Library, locate the OPCOMM blocks, and drag them to the appropriate locations in your Simulink model, as shown in Fig. 4.11. Generally, you should position these blocks on the interfaces where the subsystems require data exchange.

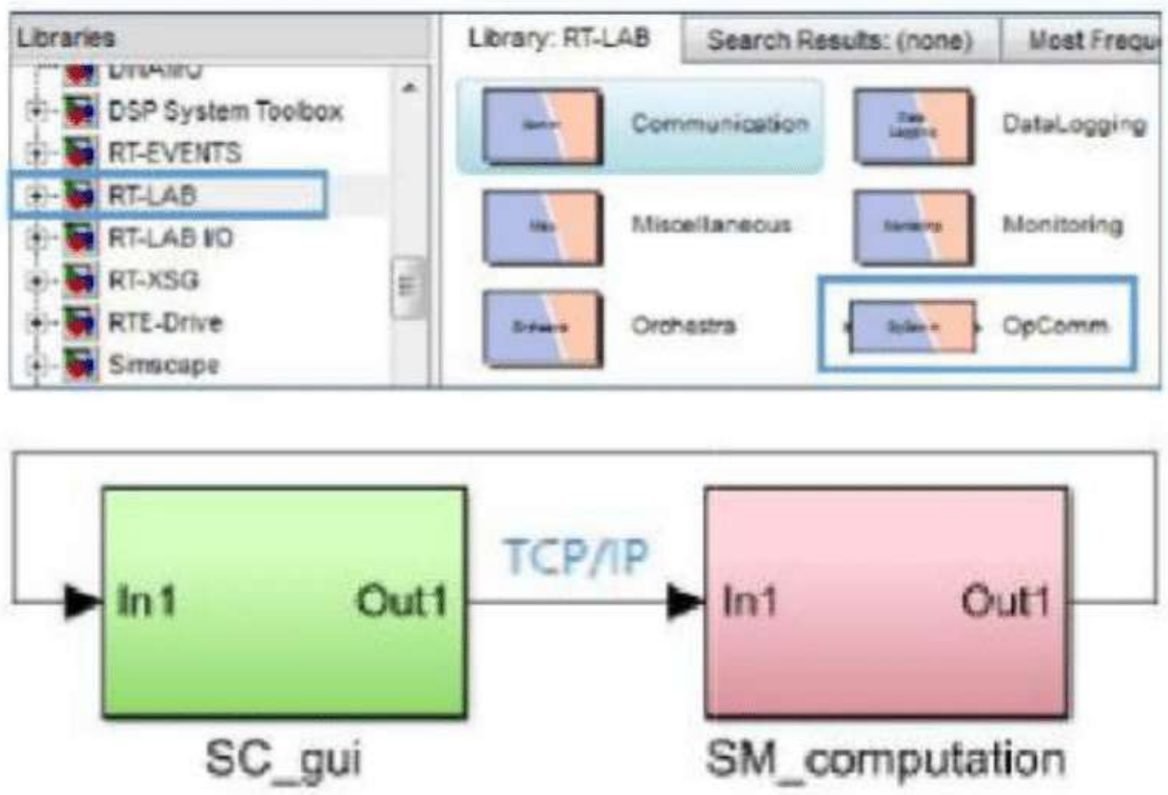


Fig. 4.11: Adding the OpComm Blocks of the RT-LAB library under MATLAB/Simulink

To load and process the model on the RT platform, you must insert or add an 'OpComm' block, responsible for communication from the RT-LAB library, available in the Simulink® library browser after RT-LAB installation. Place it either between two calculation subsystems, or between a graphical interface subsystem and a calculation subsystem. Next, place an OpComm inside each SM and SS subsystem, as illustrated in Fig. 4.12.

All subsystem inputs (SM, and SC) must first pass through an OpComm block before any operation on the signals with which they are associated. We install the OpComm block after creating and renaming the subsystems (SM and SC).

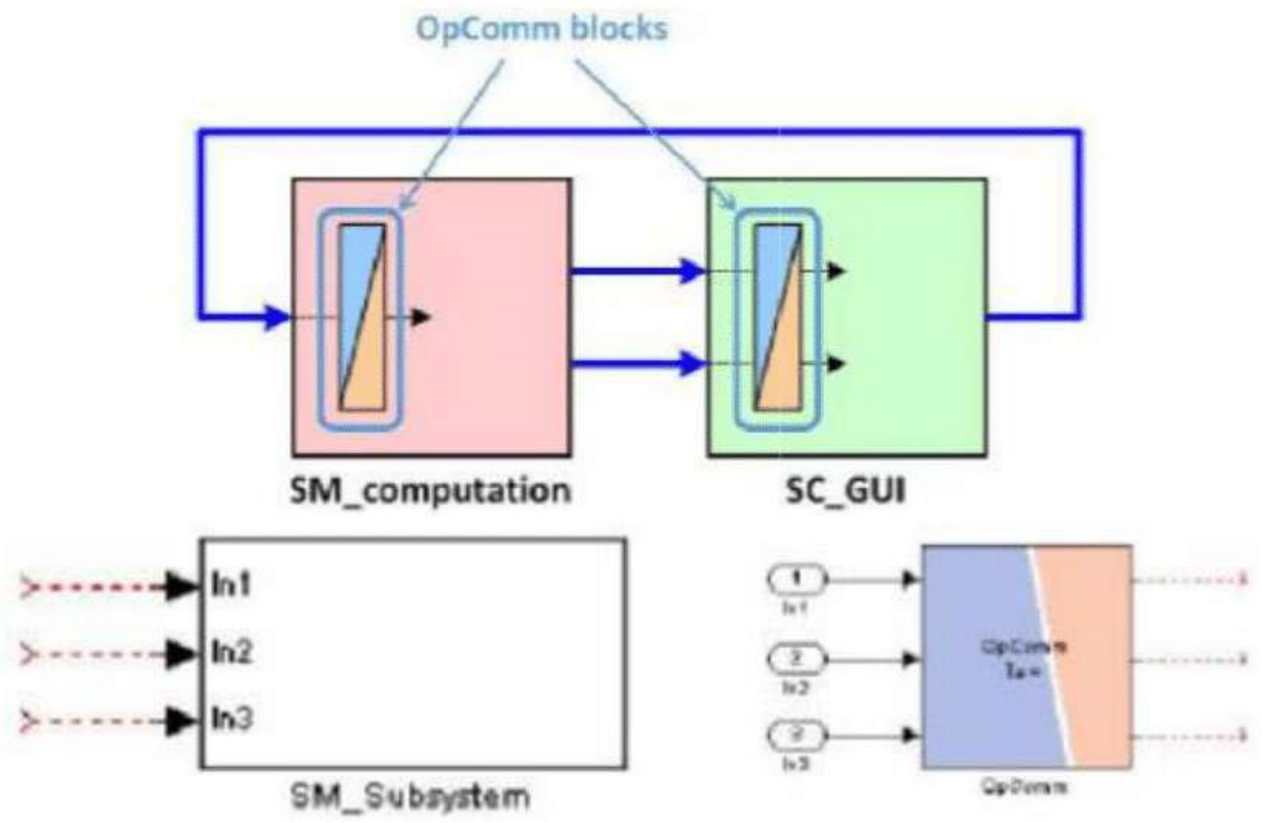


Fig. 4.12: OpComm inserted in both subsystems (SM and SC)

Fig. 4.13 shows the different connections between different subsystems through the OpComm.

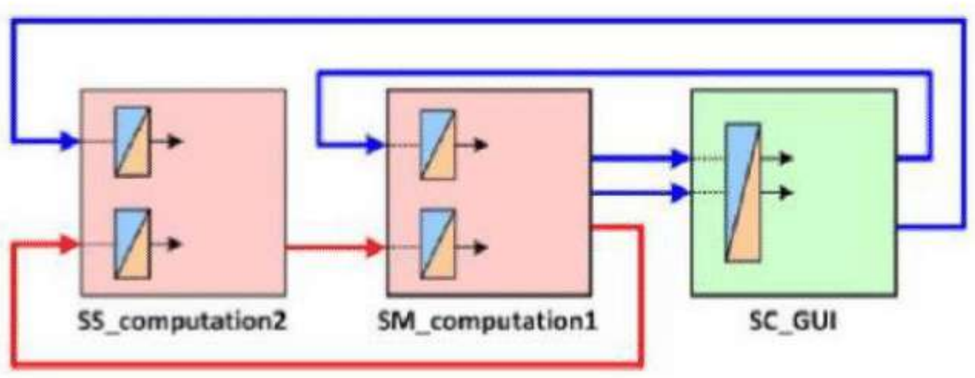


Fig. 4.13: Communication between subsystems via OpComm (red=synchronous, blue=asynchronous)

Fig. 4.14 illustrates how the calculation subsystems are assigned to the simulator's cores (CPU). The calculation subsystem is, of course, attributed to the Host PC.

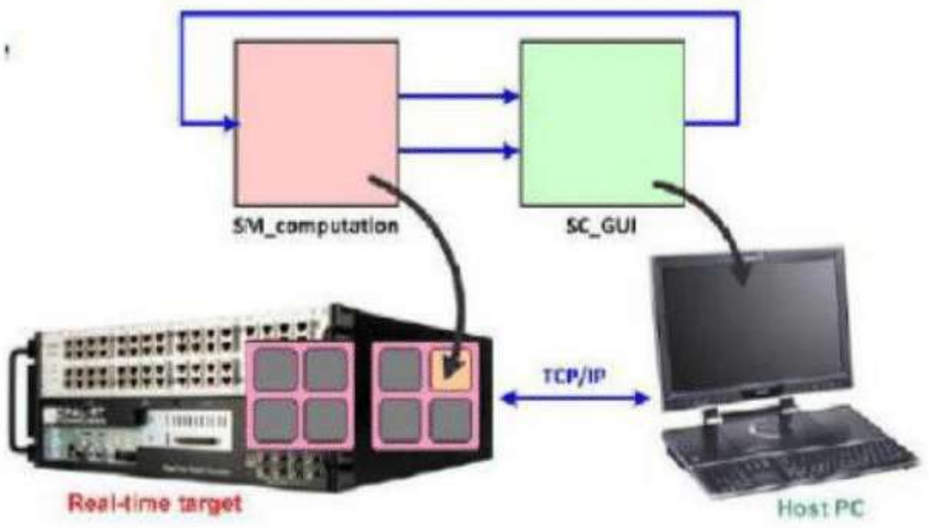


Fig. 4.14: Processing of OpComm and occupation of the simulator's CPU cores and Host PC

4.5.2.1. Configuration the OpComm blocks

Configure the OpComm blocks according to the requirements of your simulation. This includes setting parameters for data types, signal names, and communication protocols. Ensure that the configurations match the needs of the subsystems involved.

4.5.2.2. Connect subsystems

Use the OpComm blocks to connect the subsystems. Draw lines between the output ports of one subsystem and the input ports of another, using the OpComm blocks as intermediaries. This setup will facilitate the flow of data between subsystems.

4.5.2.3. Verify connections

Double-check all connections to ensure that data paths are correctly established. Verify that the OpComm blocks are configured properly and that there are no mismatches in data types or signal names.

4.5.2.4. Test the model

Run a simulation test to ensure that the OpComm blocks are functioning as expected. Monitor the data exchange between subsystems to confirm that the communication is synchronized and accurate.

4.5.3. Adding Input-Output Blocks in RT-LAB

In RT-LAB, input-output (I/O) blocks are essential for interfacing the simulation model with external hardware and for managing the data exchange within the simulation environment. These blocks facilitate the transfer of signals and data between the model and real-world devices, ensuring accurate and real-time interaction.

4.5.3.1. Purpose of Input-Output Blocks

- **Data Acquisition:** I/O blocks allow the simulation to acquire data from external sensors and measurement devices. This data can be used to inform the simulation and ensure that it accurately reflects real-world conditions.
- **Signal Generation:** These blocks are used to generate signals that can be sent to actuators, controllers, and other devices. This capability is crucial for testing and validating control algorithms and system responses.
- **Real-Time Interaction:** I/O blocks enable real-time interaction between the simulation model and external hardware, allowing for hardware-in-the-loop (HIL) testing and rapid control prototyping (RCP)
- **Synchronization:** They ensure that the data exchange between the model and external devices is synchronized, maintaining the real-time performance of the simulation.

The adding of I-O Blocks in RT-LAB is as follows:

1. Start by opening your RT-LAB model in the Simulink environment. Ensure that your model is properly structured and that the locations for the I/O blocks are identified.
2. Navigate to the RT-LAB library in Simulink. Locate the input-output blocks suitable for your application and drag them into the model. These blocks can be found under categories such as Analog Input, Analog Output, Digital Input, Digital Output, etc.
3. Configure each I/O block according to the specifications of your external hardware. This configuration includes setting parameters such as channel numbers, signal ranges, sampling rates, and data types. Ensure that the configurations match the capabilities and requirements of the external devices.
4. Use the I/O blocks to connect your subsystems to the external hardware. Draw lines from the outputs of sensors or measurement devices to the input blocks, and from the output blocks to the inputs of actuators or controllers.
5. Double-check all connections to ensure they are correctly established. Verify that the I/O blocks are properly configured and that there are no mismatches in data types or signal ranges.
6. Conduct a test simulation to verify that the I/O blocks are functioning correctly. Monitor the data exchange between the model and the external hardware to confirm that the interaction is accurate and synchronized.

By integrating I-O blocks into your RT-LAB simulations, you can achieve a more interactive and realistic simulation environment, capable of interfacing with external hardware and performing real-time testing and validation efficiently.

4.5.4. Preparation of a model [02]:

Initially, we need to run the RT-LAB program and establish a new project, as shown in Fig. 4.15.

- In the menu: File> New> RT-LAB Project,
- From the Project Explorer view.
- Give a project name, then click on "Next" to add an example model at RT-LAB project. Click on "Finish" to create an empty project and add manually A model.

The process for adding an example model to the project under RT-IAB is depicted in Fig. 4.16.

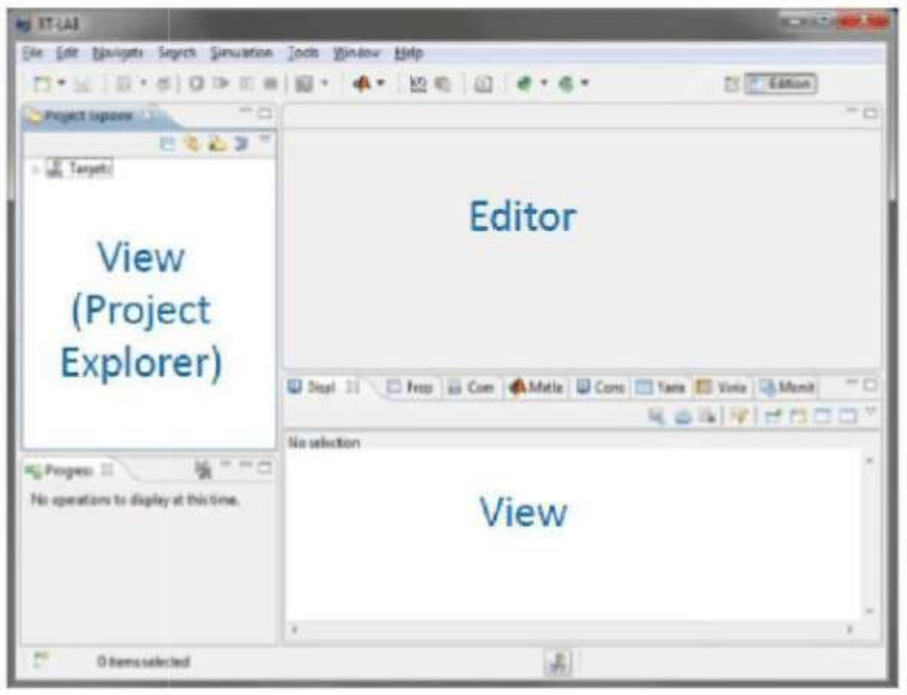


Fig. 4.15: Main window after launching the RT-LAB software

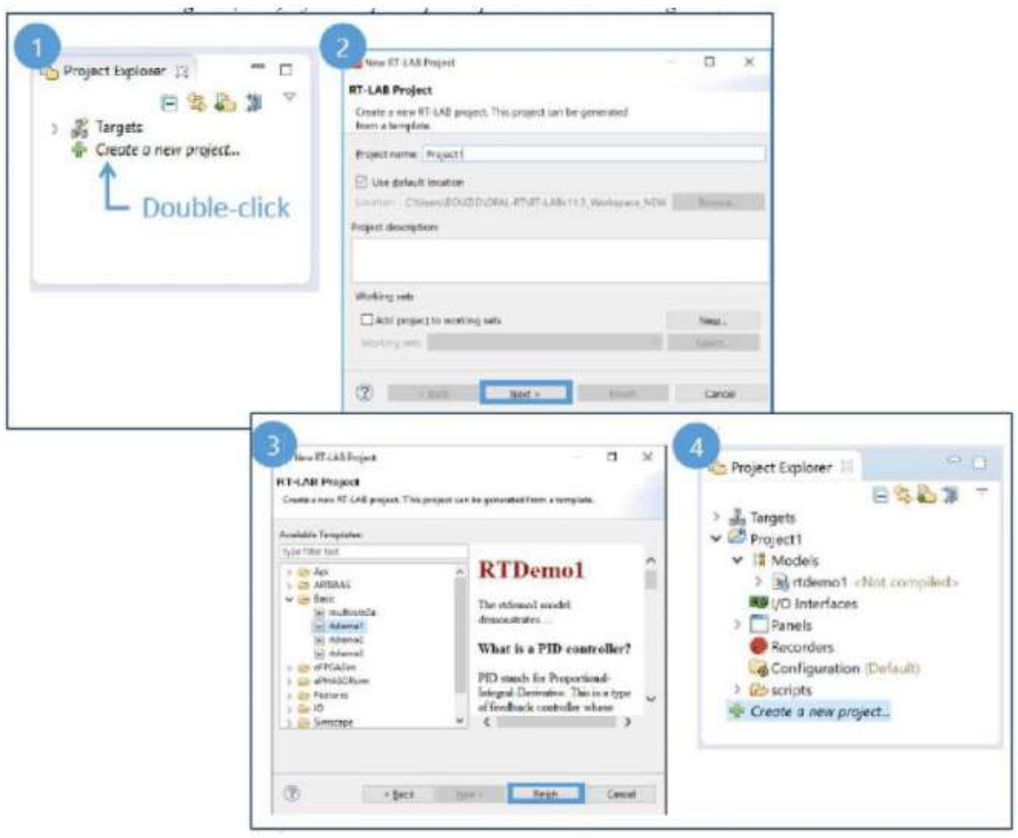


Fig. 4.16: Steps for adding an example model to the project in RT-LAB

The RT-LAB menu also allows us to add an example of an existing model in the project. As an example, C:\OPAL-RT\RT-LABx.x.x\Examples, shown in Fig. 4.17.

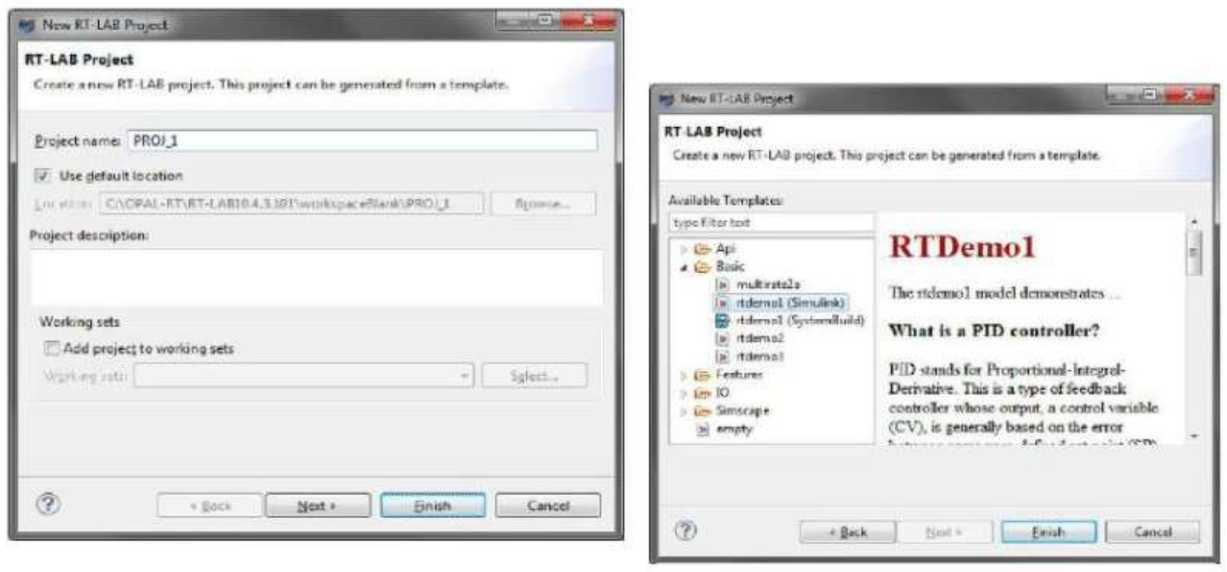


Fig. 4.17: Windows for adding a model to the project under RT-LAB

As shown in Fig. 4.18, you can also add a new blank model to the project or subsystem by:

- File > New > RT-LAB Model

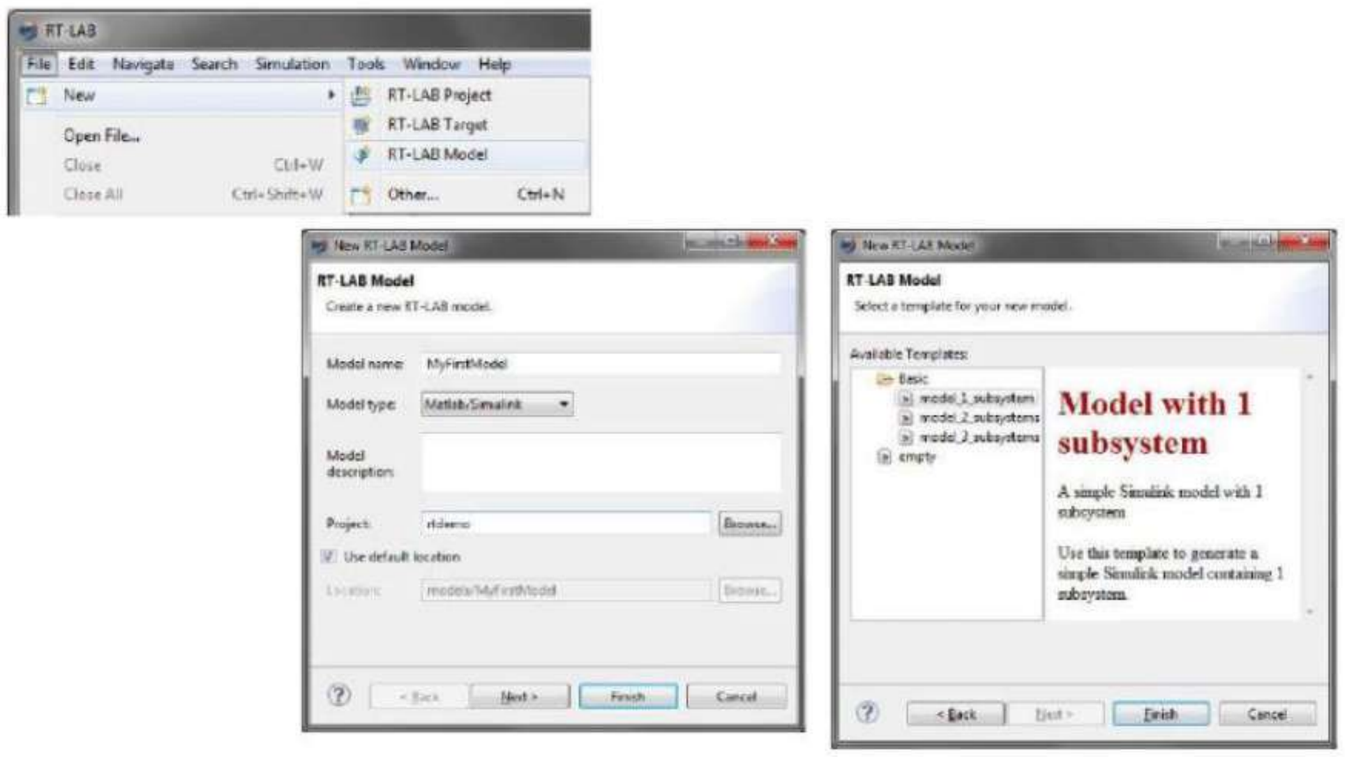


Fig. 4.18: Creation of a new blank model for the project under RT-LAB

Given that the project can include an existing user model:

Add (a link): Click "Add" to modify the original model.

To duplicate the model into the workspace, you may also use Import:

These manipulations are shown in Fig. 4.19.

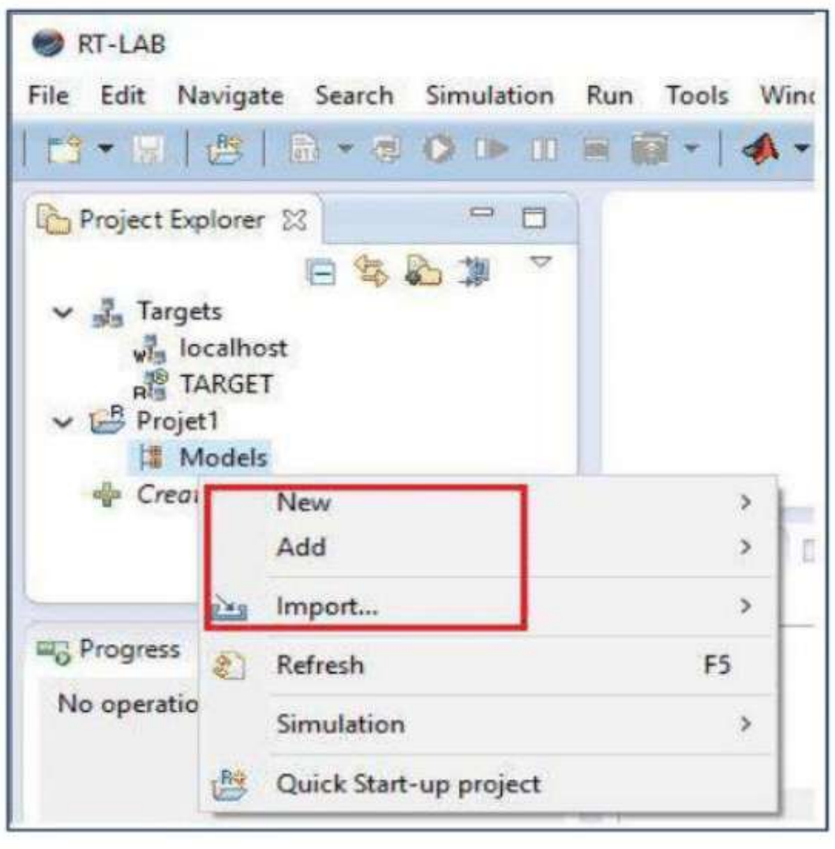


Fig. 4.19: Window to "Add" or "Import" existing models

Once the project is created, the model added or added, we open the model by default with the specified version of MATLAB/Simulink. Using: "Edit", the model will be edited and explore under a chosen version of Matlab/Simulink. And the model opens. The Fig. 4.20 shows this procedure more.

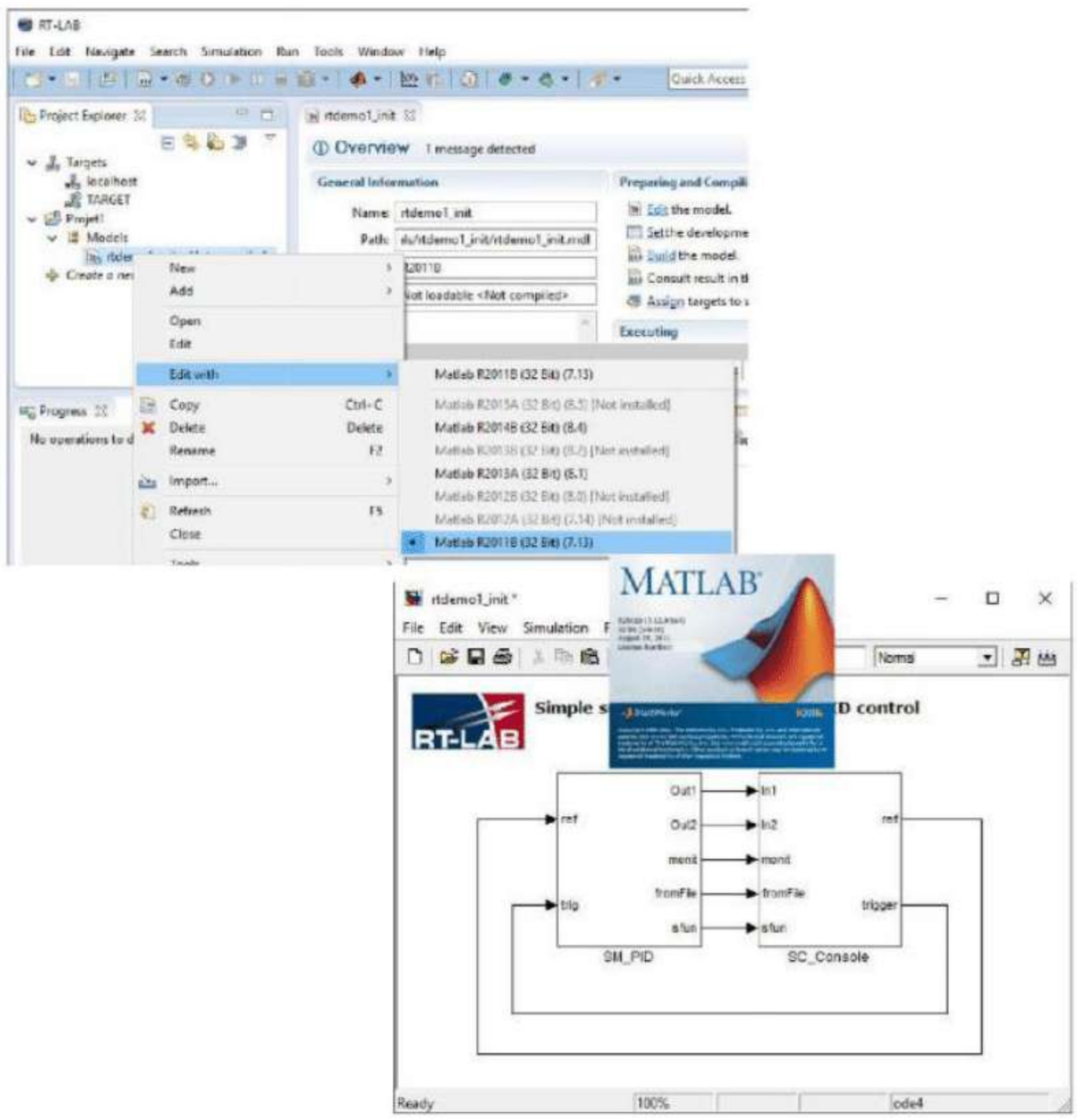


Fig. 4.20: "Edit" and selection the MATLAB/Simulink version to open the model

So far, the simulator (Hard) is not operational, we must establish the connection between the PC and the simulator via the "Add a target" target menu:

- Manually, using the IP address.
- Using discovery targets (automatic search for accessible targets). "Discover target".

Knowing that we have already configured the network data of the IP addresses, because the "host" PC and the target must be connected via Ethernet with a compatible IP address.

The address of the target: "192.168.10.101" and that of the PC "192.168.10". valid for OP5700. This step is illustrated in Fig. 4.21.

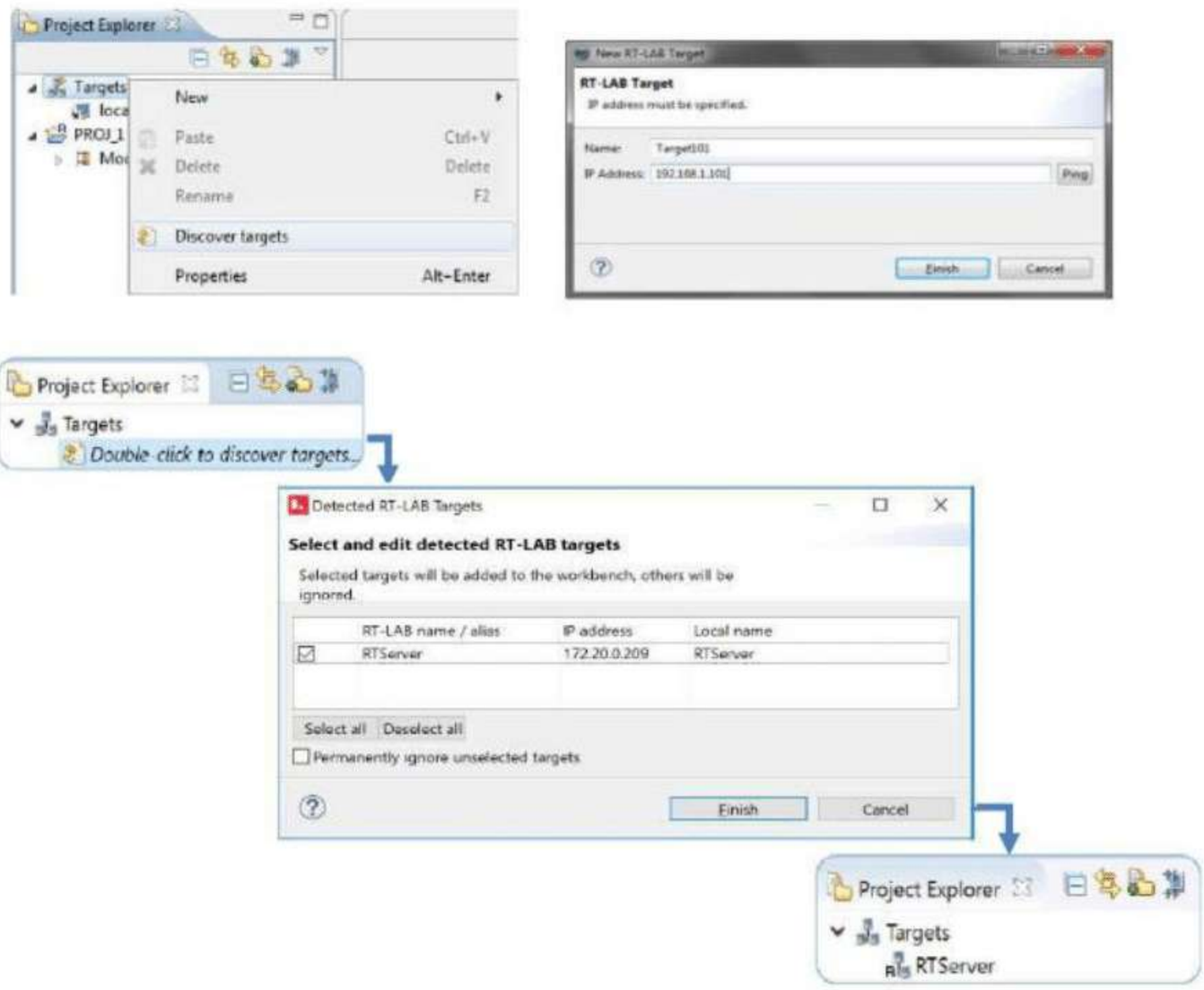


Fig. 4.21: Windows of the activation of target "PC-Simulator"

4.6. Build and execution of a Simulink model in real time

To build a Simulink model in RT-LAB, follow these steps:

4.6.1. Select the "Build" Menu

- Choose the appropriate development platform, including software versions and target platforms.
- Divide the model into several .mdl files corresponding to the top-level subsystems (such as SM, and SC).
- Generate C Code: RT-LAB generates C code from the Simulink models.
- Transfer the Generated C Code: The generated code is transferred for building.
- Build the C Code: The target compiler compiles and links the files to create a real-time executable.
- Transfer the Built Model: The executables are transferred back to the host computer for execution.
- Figure 2.22 in the document illustrates the model building phase with RT-LAB.

These steps ensure that the model is ready for real-time execution, enabling effective simulation and testing of systems in a controlled environment.

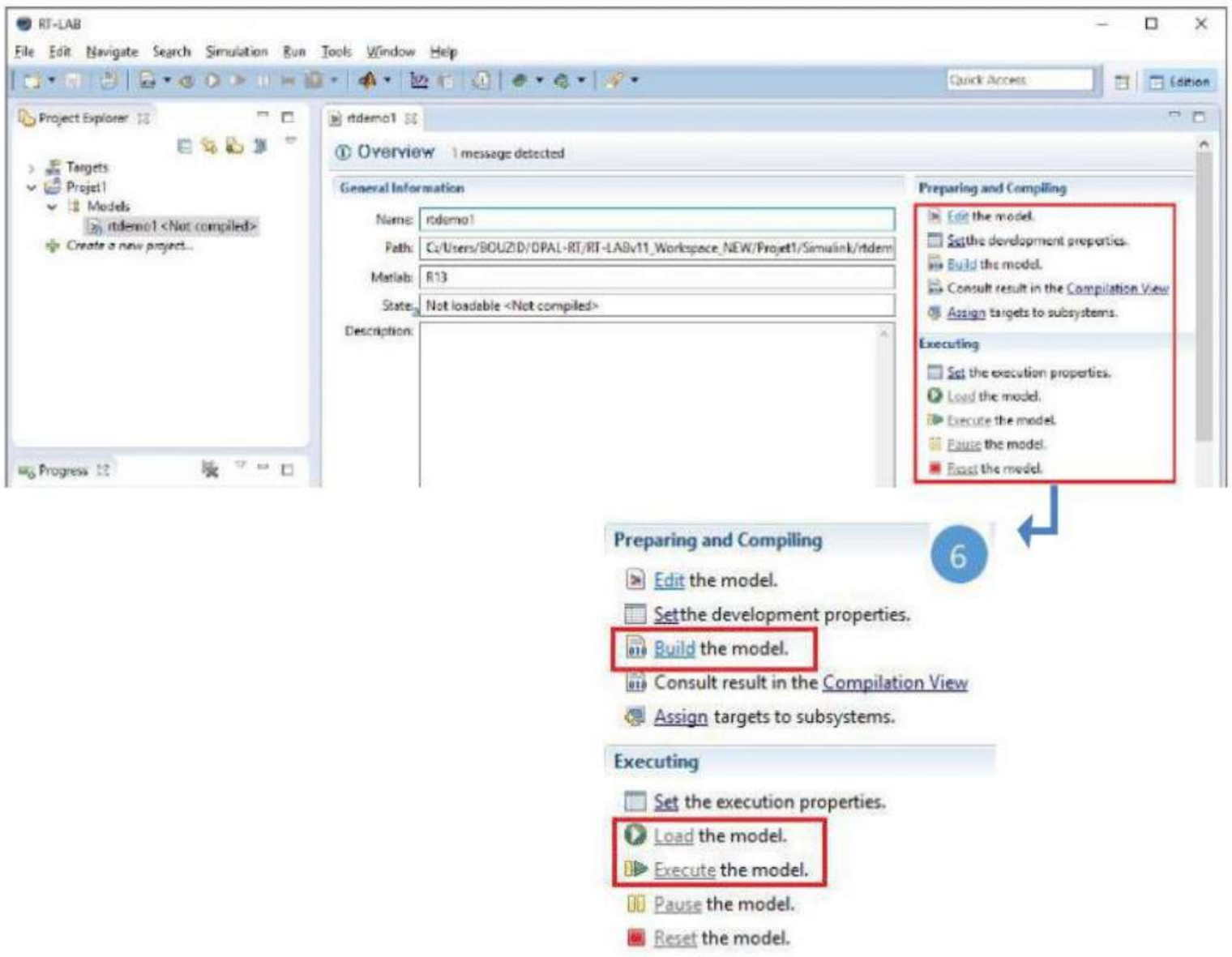


Fig. 4.22: Building a model in RT-LAB

4.6.2. Load and execute the model on the target

To load and execute the model on the target, they are four steps need to follow:

1. Select the simulation mode: Simulation, Software Synchronized, or Hardware Synchronized;
2. Launch the "Load" menu to load the model; a console window will appear;
3. Launch "Execute" or "Run" to start the real-time execution of the model on the simulator;
4. To end the real-time simulation and record results or reset the model, activate "Reset".

Figs 4.23 and 4.24 illustrate the execution and resetting of the model.

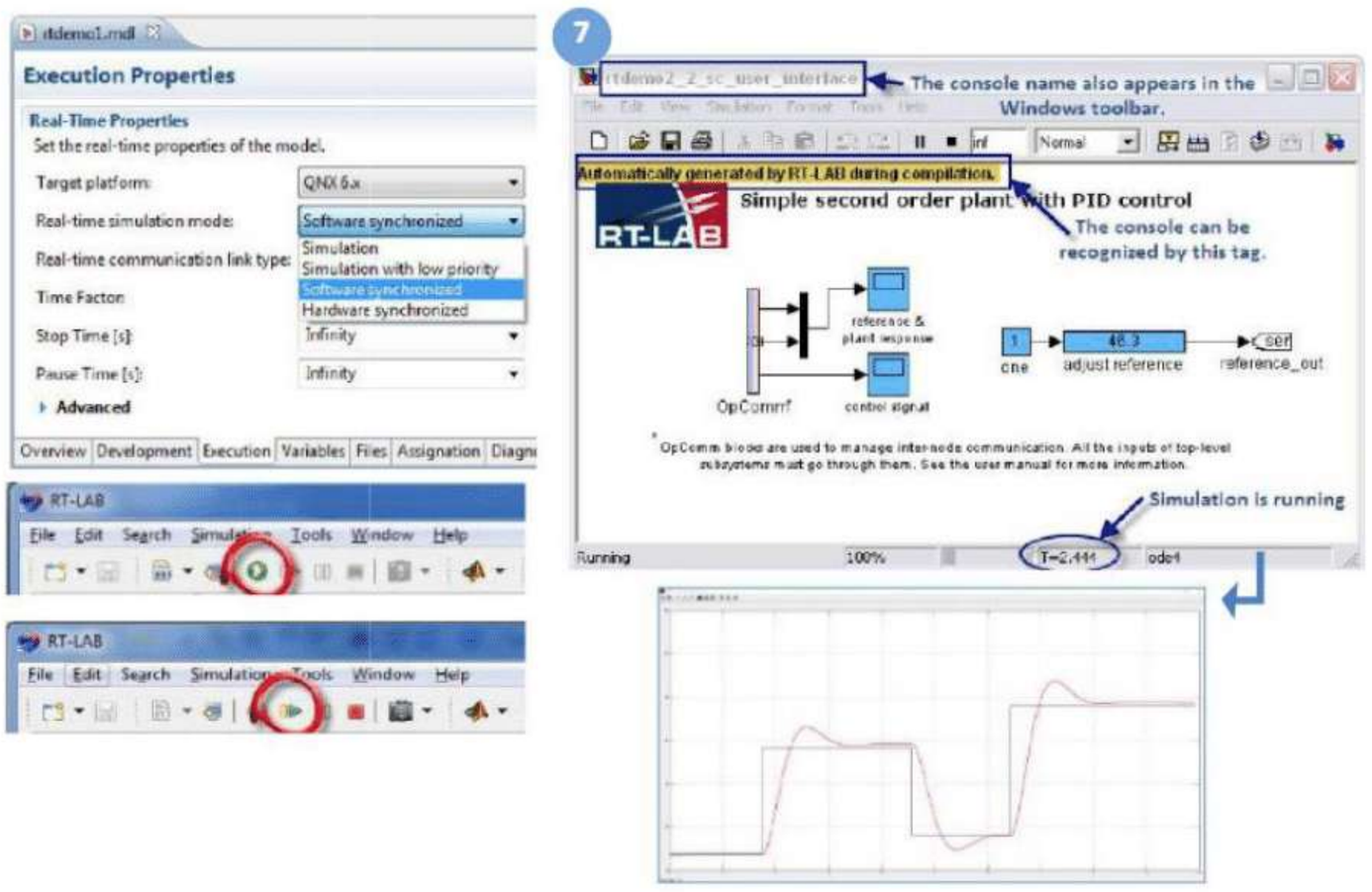


Fig. 4.23: Model execution and console generated by RT-LAB in MATLAB/Simulink

The "Reset" order stops the simulation, it does not restart the simulator, after this step the model is in "idle" state

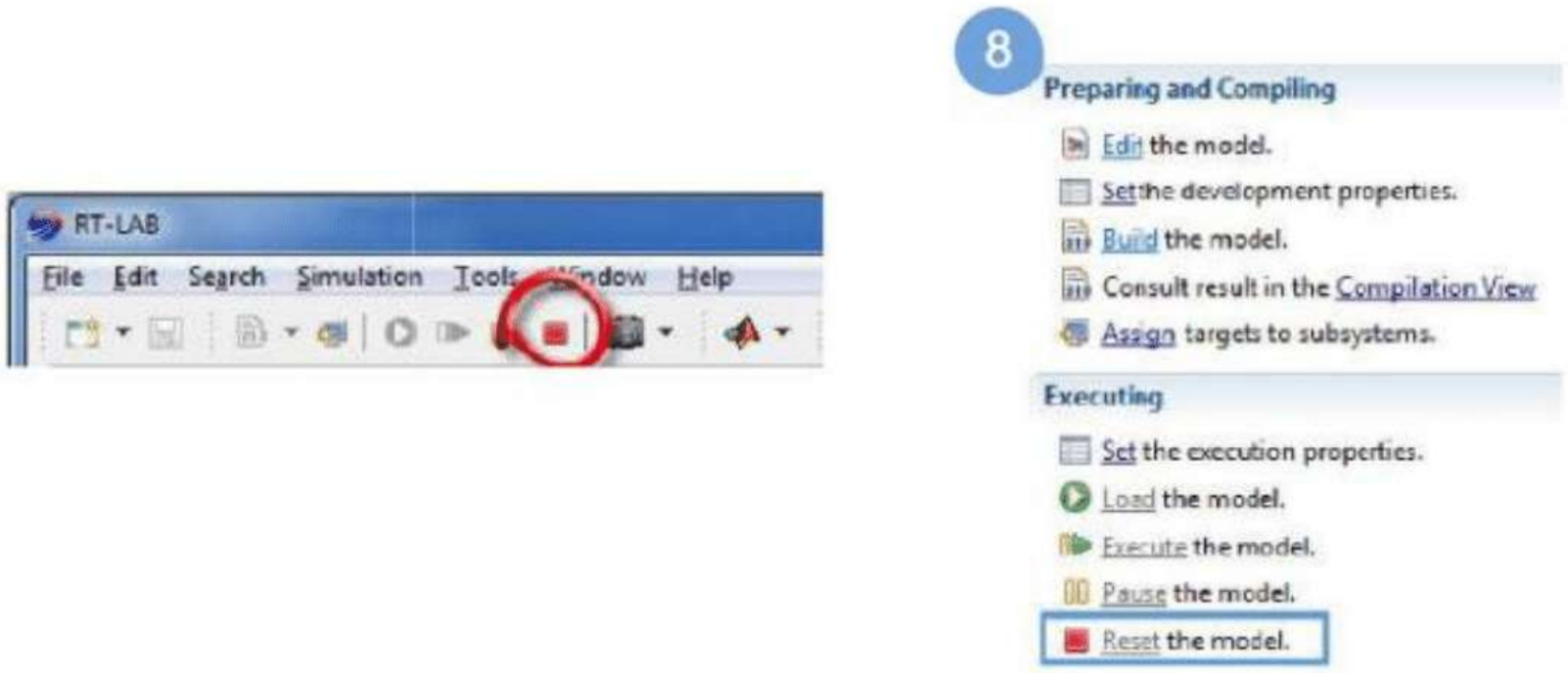


Fig. 4.24: Simulink console saved results generates after reset

4.7. Hardware-in-the-Loop (HIL) real time simulations

Hardware-in-the-Loop (HIL) real time verification of simulation results of the three methods produced in Chapter 3 are presented in this section. The proposed adaptive virtual complex impedance-based droop control method is tested in the real time digital simulator OPAL-RT. For the real-time simulation, the Simulink model of each control method-based IMG that investigated in this thesis has been compiled with RT-LAB software in order to convert the Simulink model to C language. The compiled model in RT-LAB of each control method is loaded in OPAL-RT to verify this control method in real time. The Opal-RT-4510 testing system comprises target nodes, oscilloscope, host PC, real-time and Ethernet communication links, and input and output boards. A picture of the lab setup can be seen in Figure 26. The power circuit, control circuit, and load parameters used for the HIL real time verification are similar to those used in previous simulations as described in Tables A.1 and A.2. The HIL real time validation is done for the three control methods produced in Chapter 3.

4.7.1. HIL real time simulation results of the traditional droop control method

The real-time simulation results obtained using the traditional droop control method are displayed in Figs. 4.25 to 4.29. Fig. 4.25 illustrates the active power outputs of the three DG units, Fig. 4.26 illustrates the reactive power outputs of the three DG units, Fig. 4.27 shows the first phase line currents of the three DG units, Fig. 4.28 displays the circulating currents between the three DG units, and Fig. 4.29 exhibits the RMS voltage outputs of the three DG units.

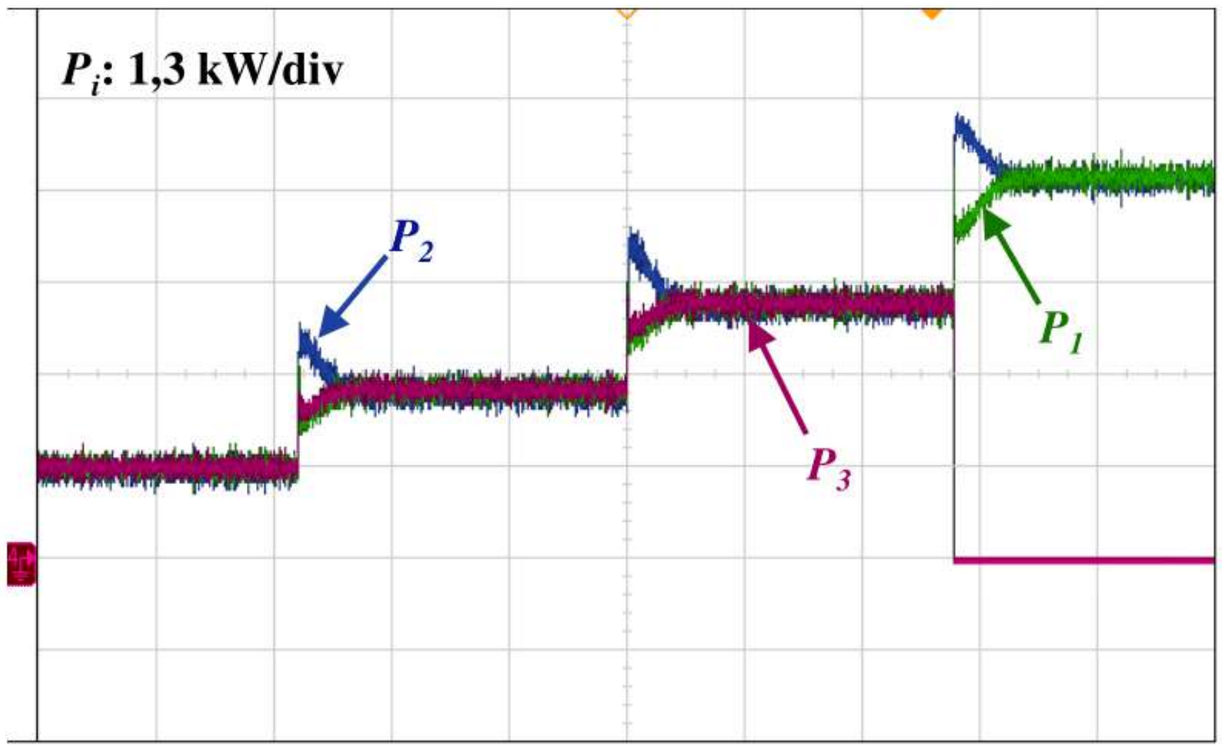


Fig. 4.25: Output active power of the three DG units

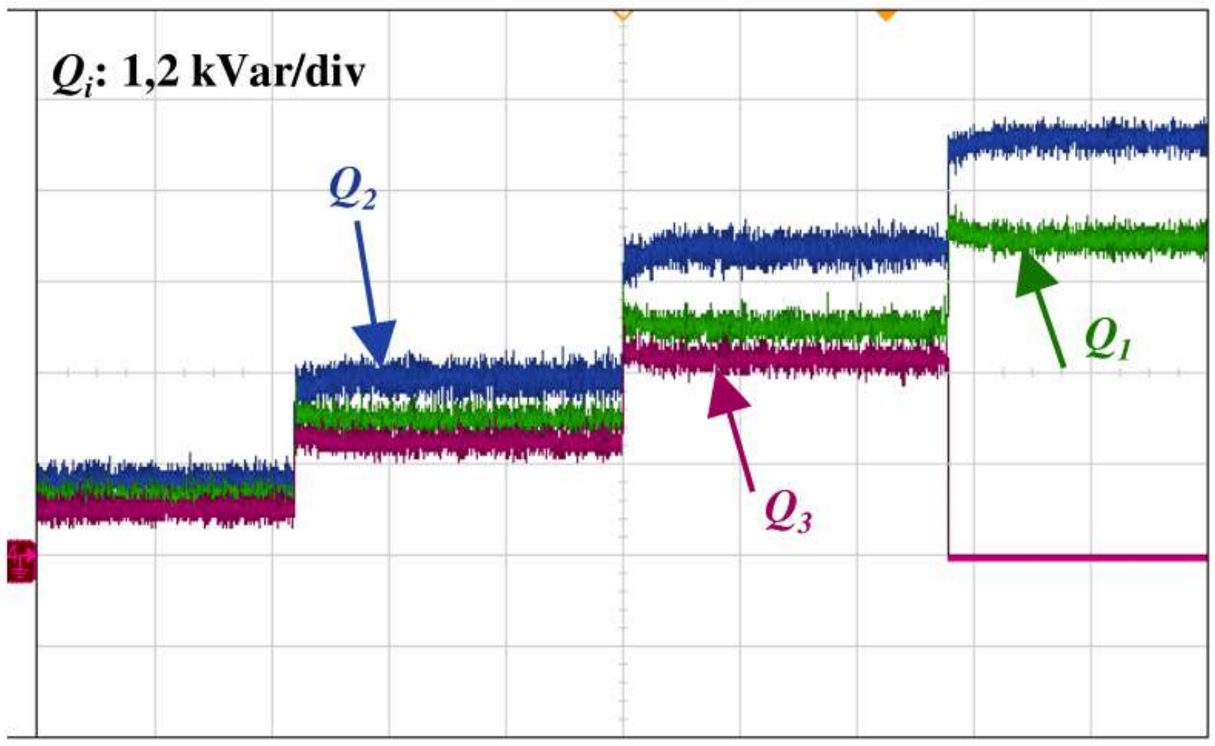


Fig. 4.26: Output reactive power of the three DG units

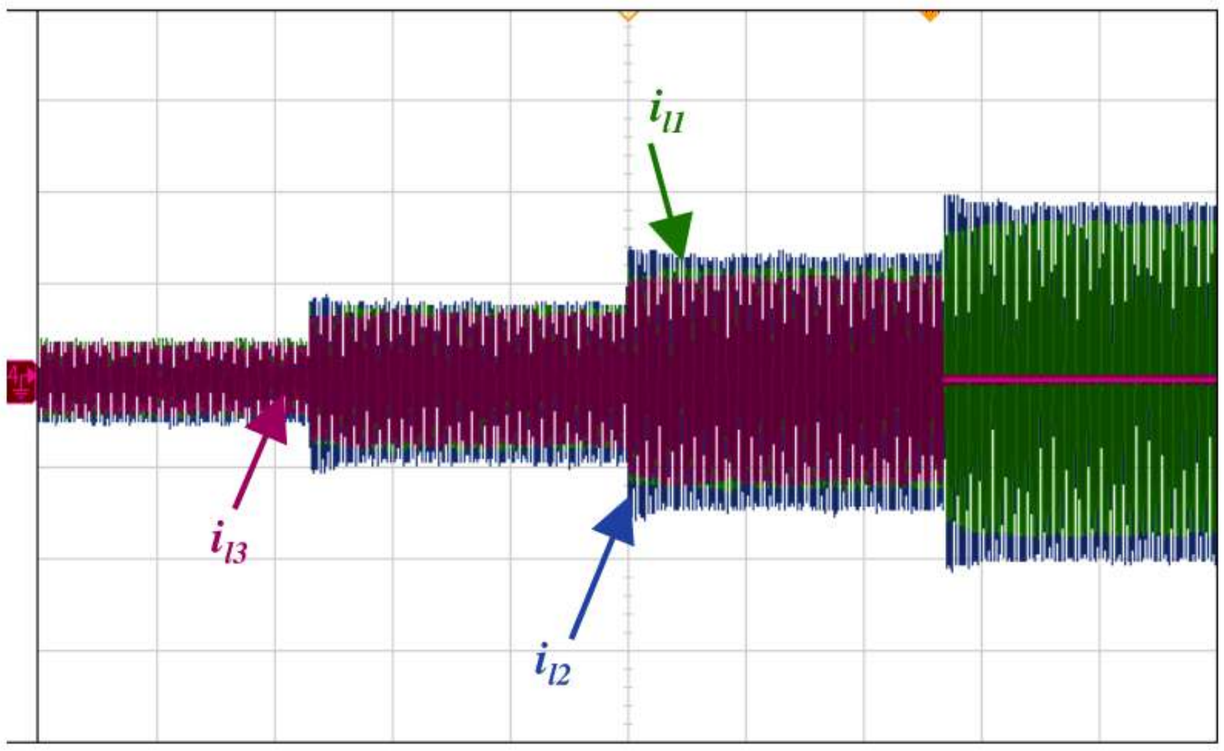


Fig. 4.27: First-phase line current of the three DG units

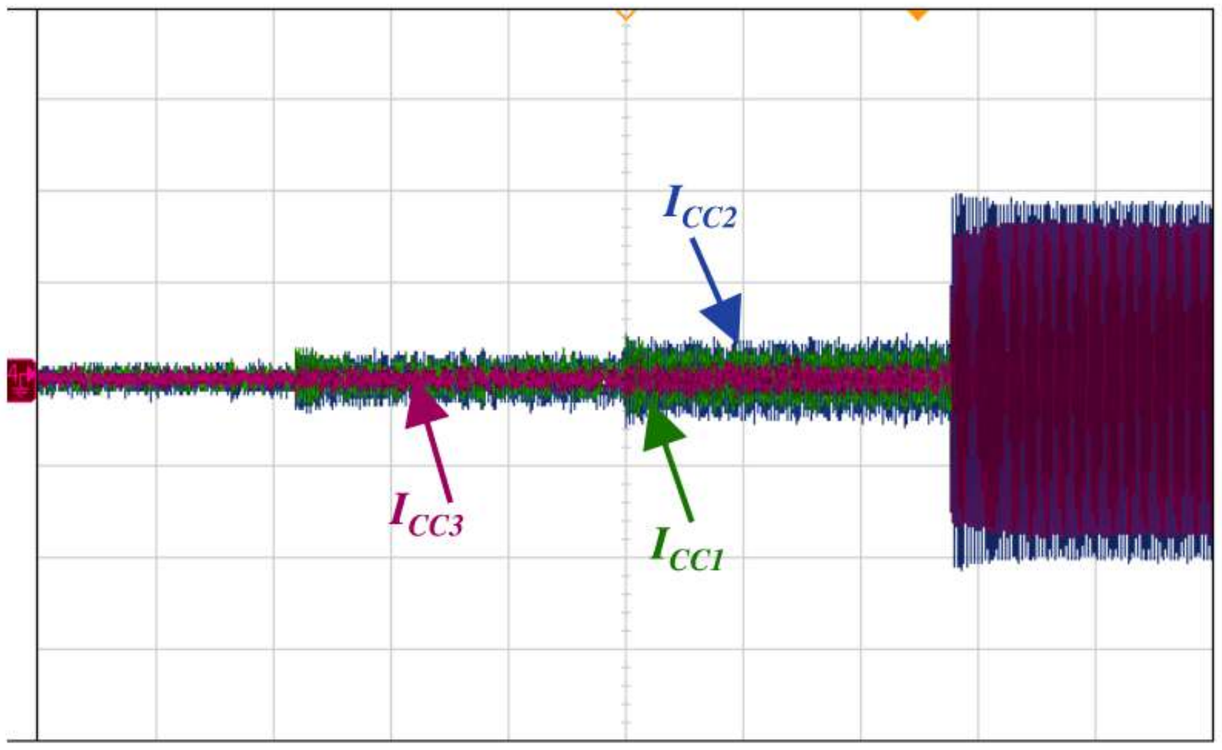


Fig. 4.28: Circulating currents

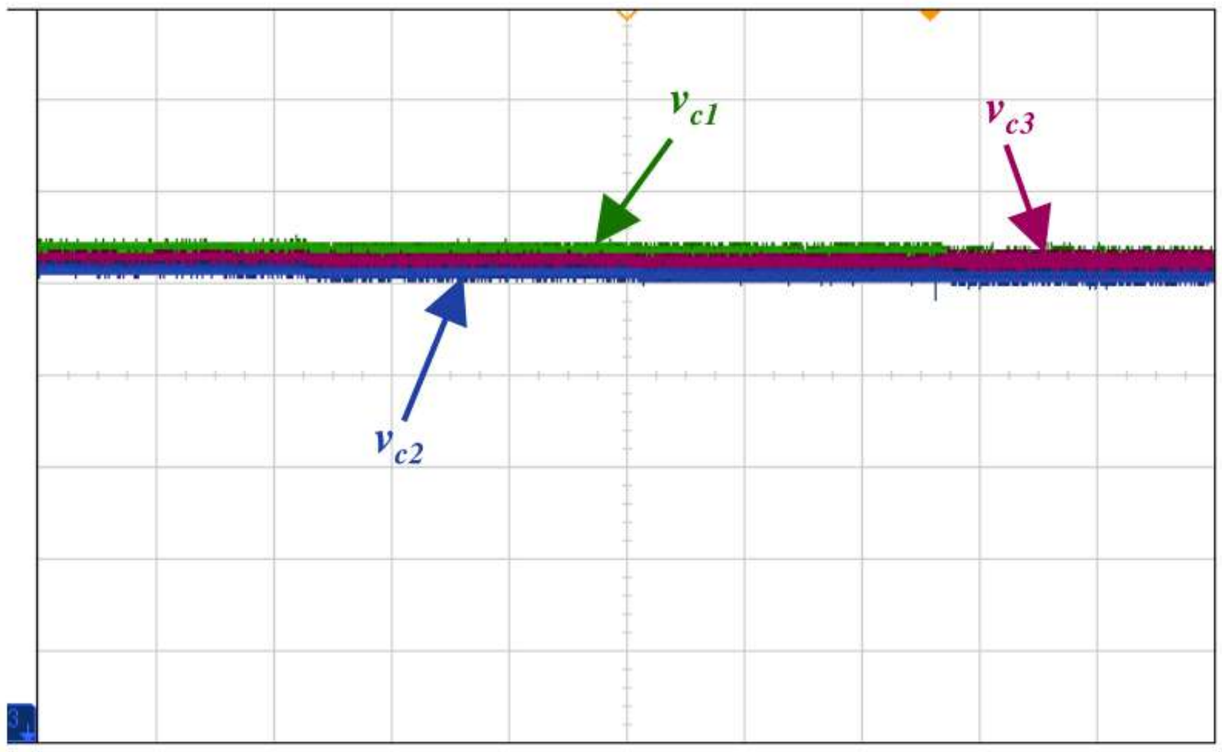


Fig. 4.29: Output RMS voltage of the three DGs

4.7.2. HIL real time simulation results of the virtual complex impedance-based droop control method

The real-time simulation results obtained using the virtual complex impedance-based droop control method are displayed in Figs. 4.30 to 4.34. Fig. 4.30 illustrates the active power outputs of the three DG units, Fig. 4.31 illustrates the reactive power outputs of the three DG units, Fig. 4.32 shows the first phase line currents of the three DG units, Fig. 4.33 displays the circulating currents between the three DG units, and Fig. 4.34 exhibits the RMS voltage outputs of the three DG units.

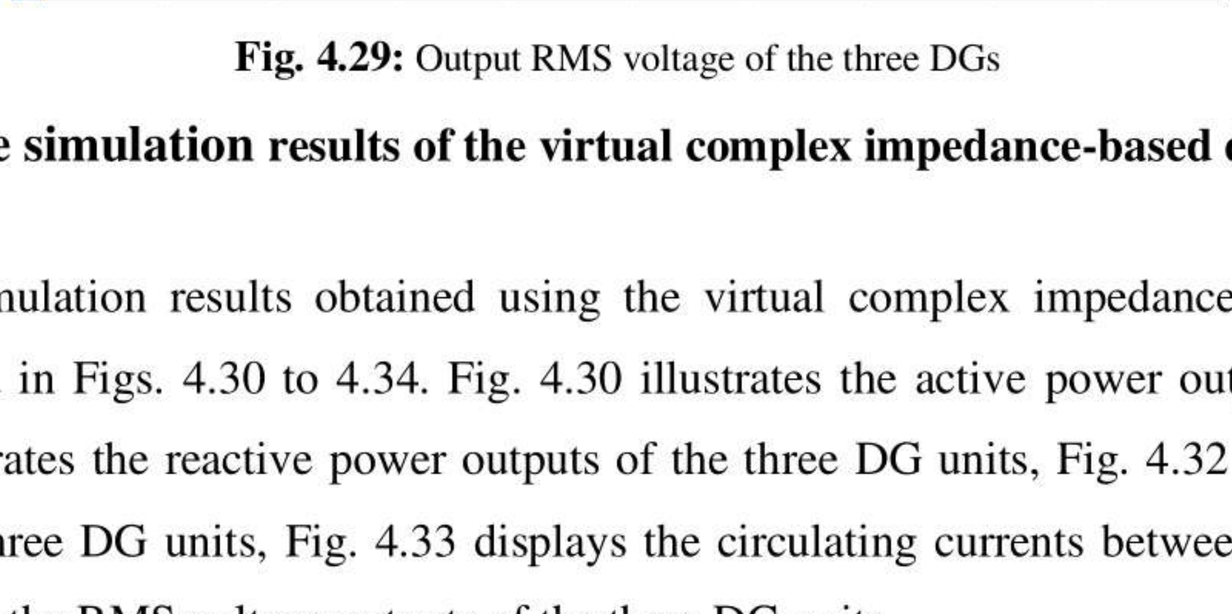


Fig. 4.30: Output active power of the three DG units

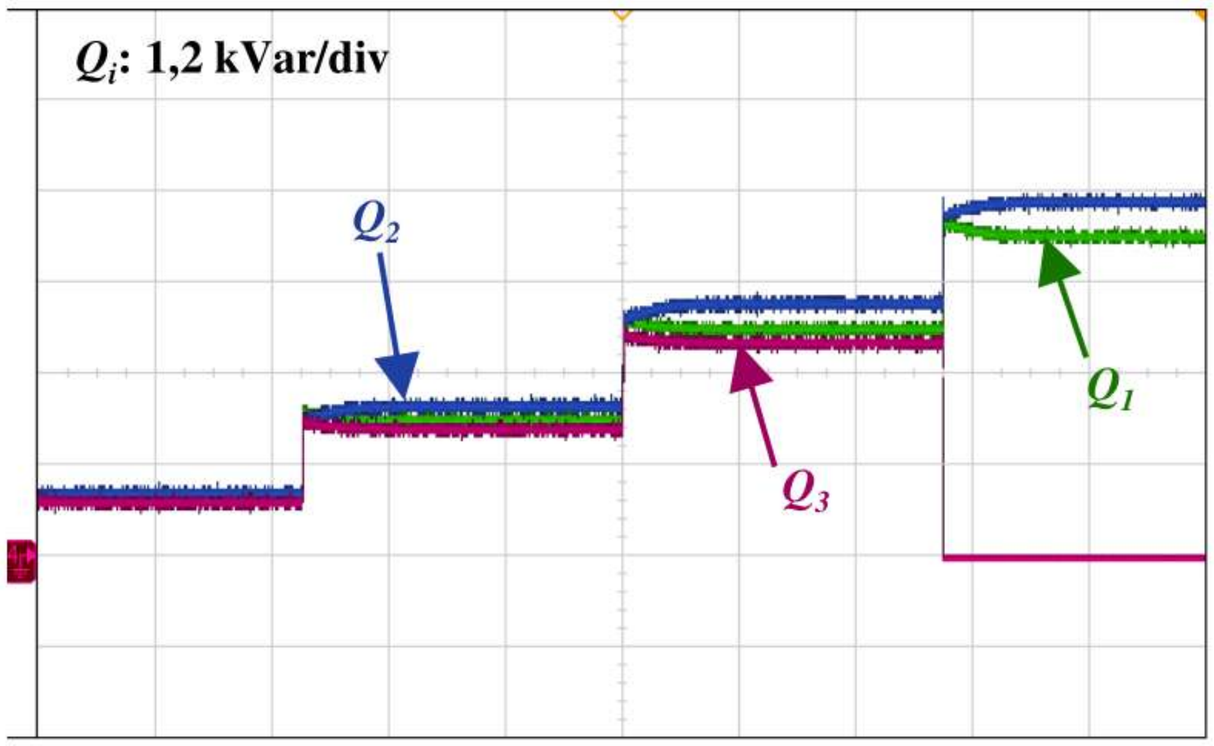


Fig. 4.31: Output reactive power of the three DG units

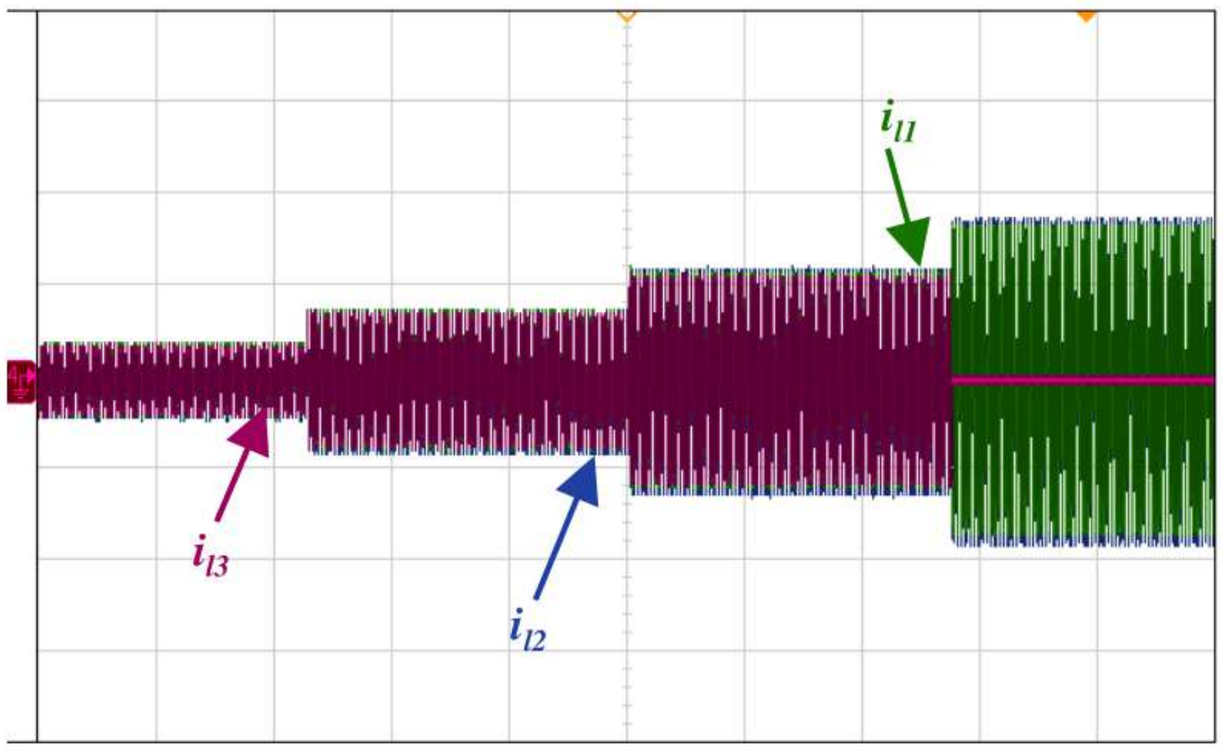


Fig. 4.32: First-phase line current of the three DG units

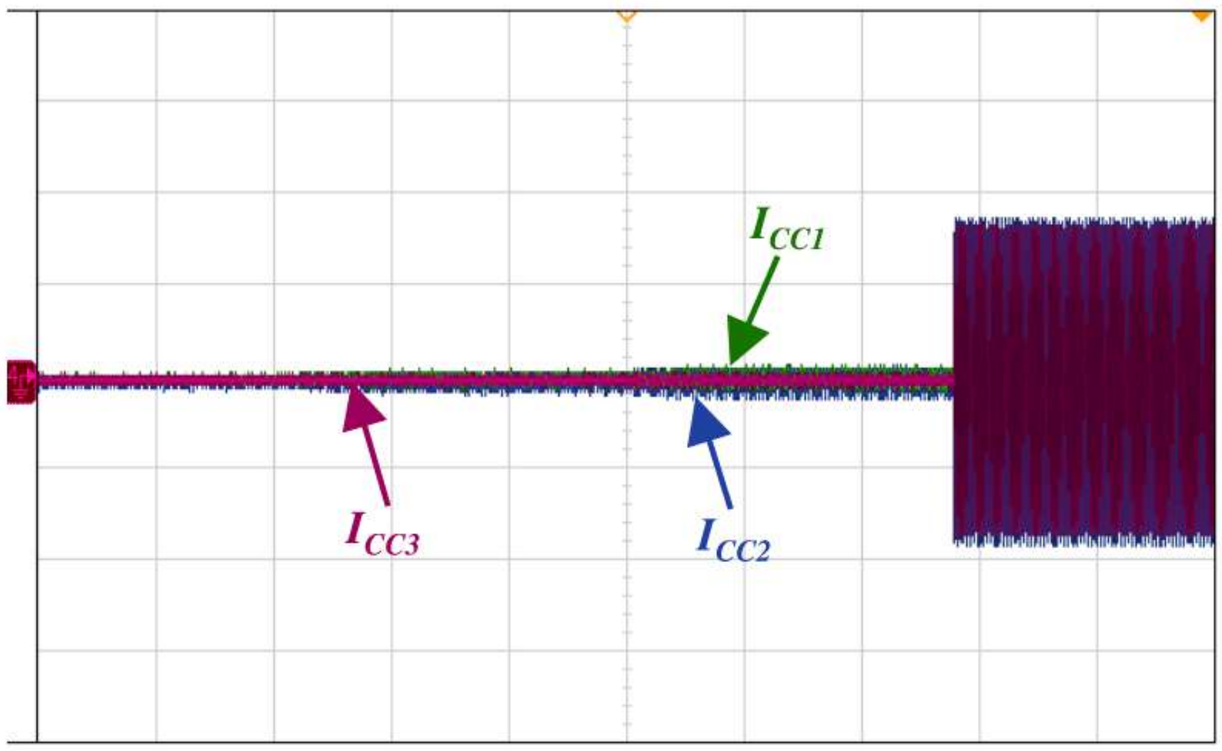


Fig. 4.33: Circulating currents

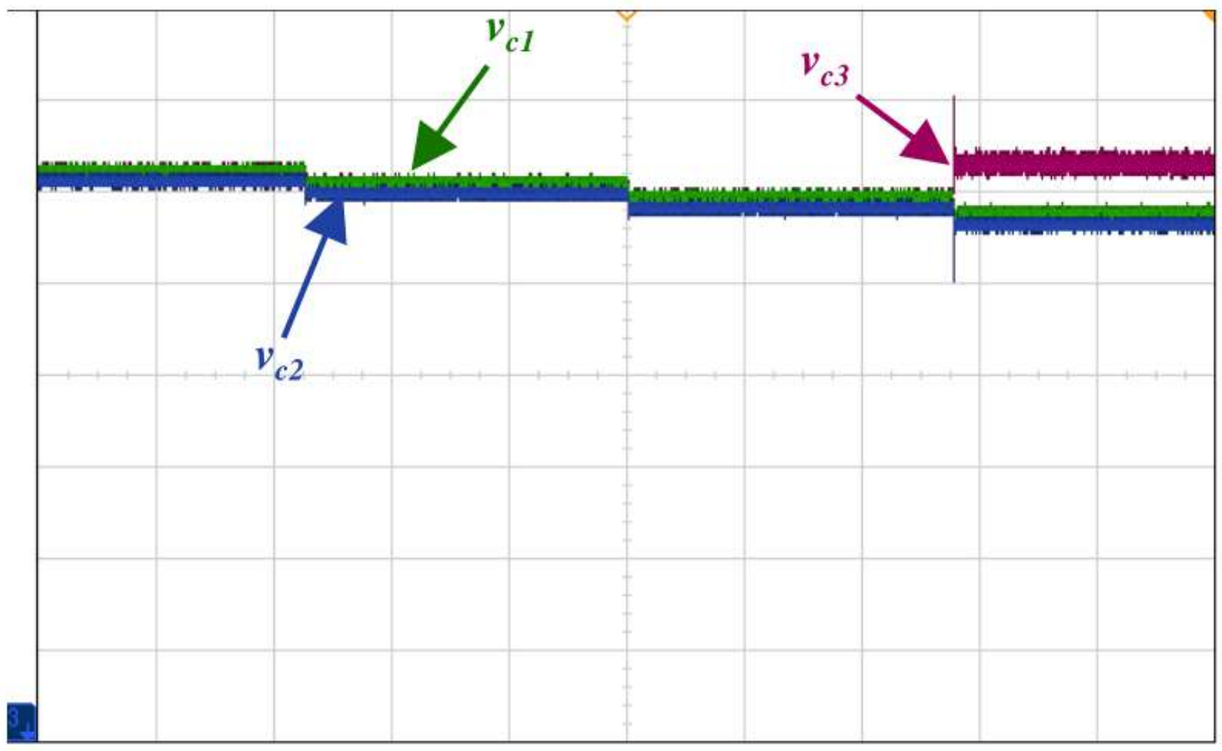


Fig. 4.34: Output RMS voltage of the three DGs

4.7.3. HIL real time simulation results of the virtual complex impedance-based droop control method

The real-time simulation results obtained using the virtual complex impedance-based droop control method are displayed in Figs. 4.30 to 4.34. Fig. 4.30 illustrates the active power outputs of the three DG units, Fig. 4.31 illustrates the reactive power outputs of the three DG units, Fig. 4.32 shows the first phase line currents of the three DG units, Fig. 4.33 displays the circulating currents between the three DG units, and Fig. 4.34 exhibits the RMS voltage outputs of the three DG units.

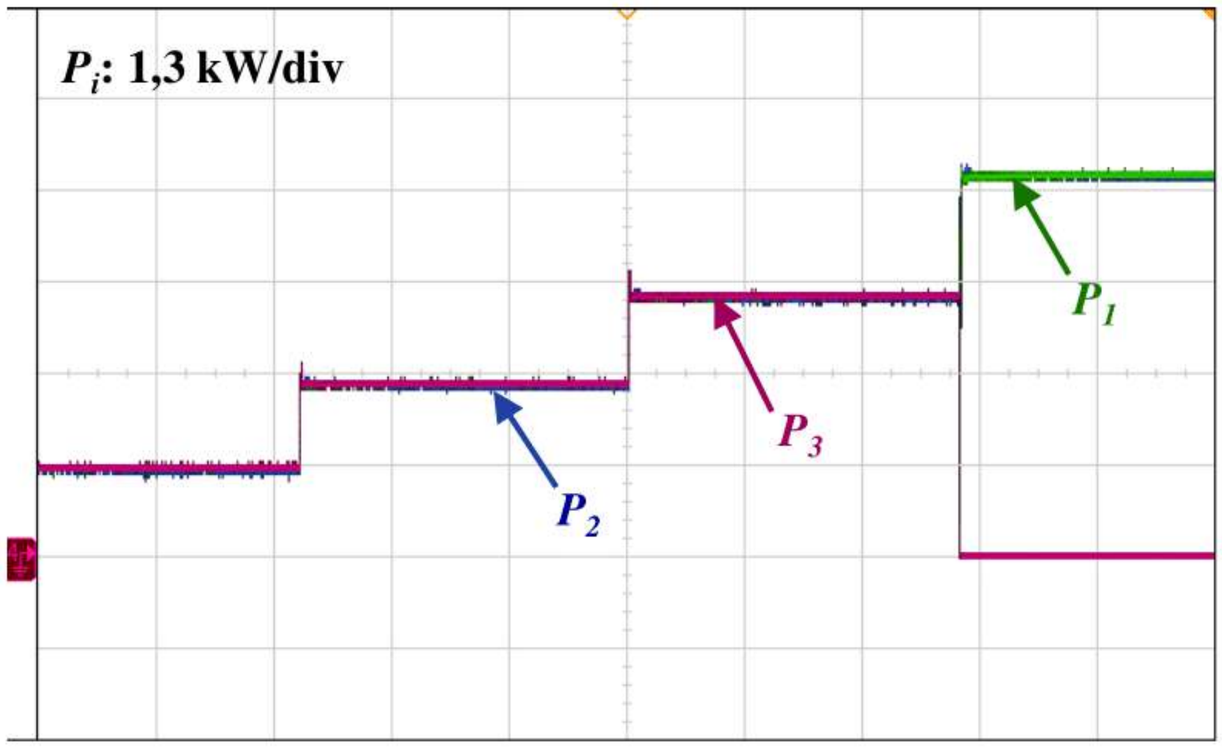


Fig. 4.35: Output active power of the three DG units

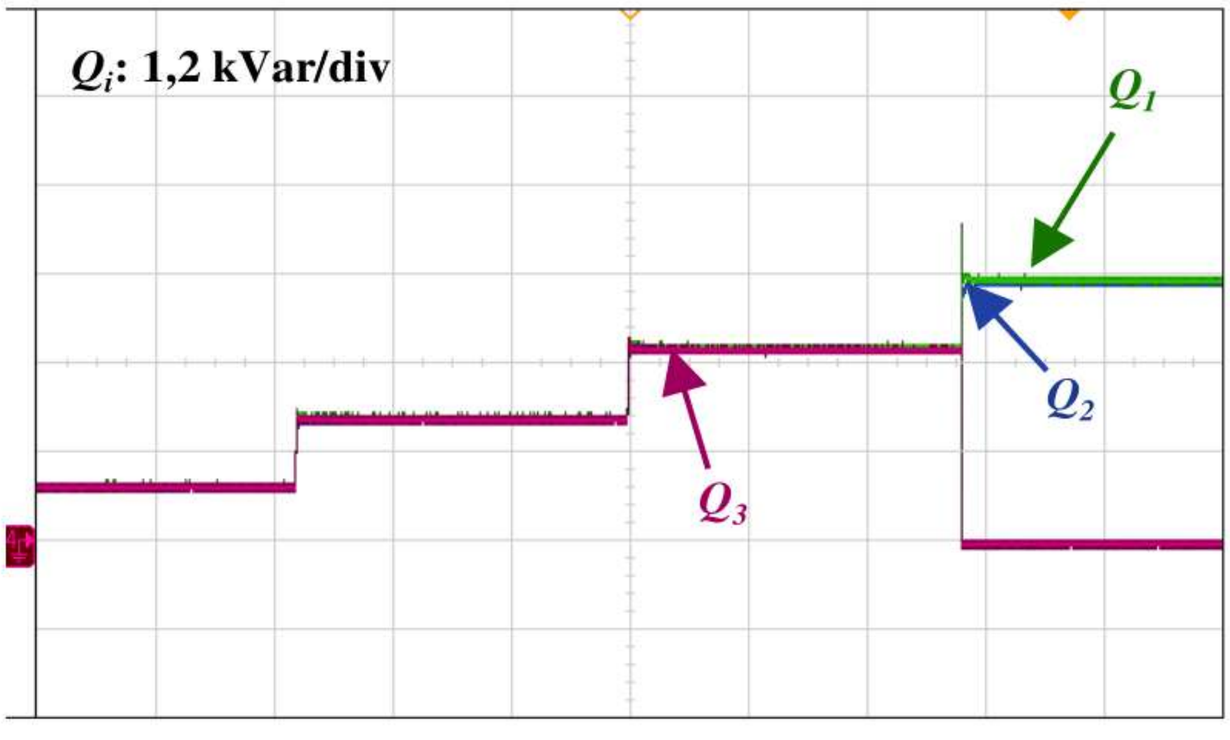


Fig. 4.36: Output reactive power of the three DG units

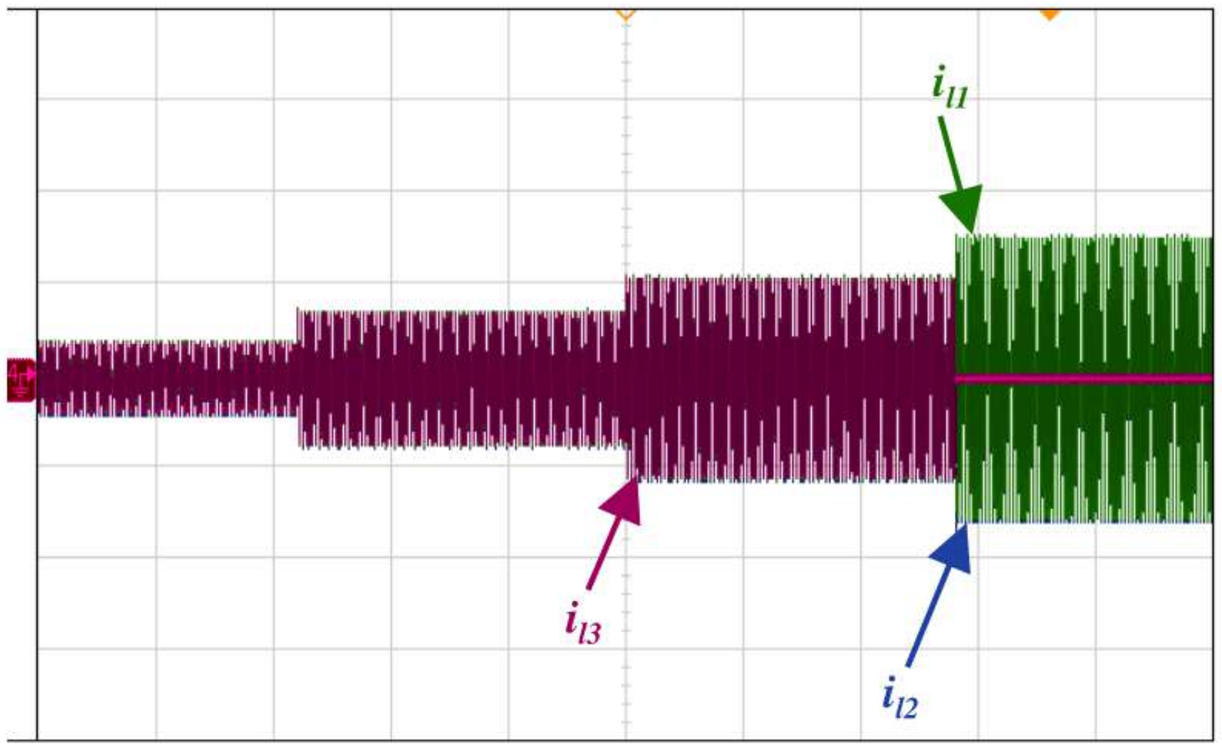


Fig. 4.37: First-phase line current of the three DG units

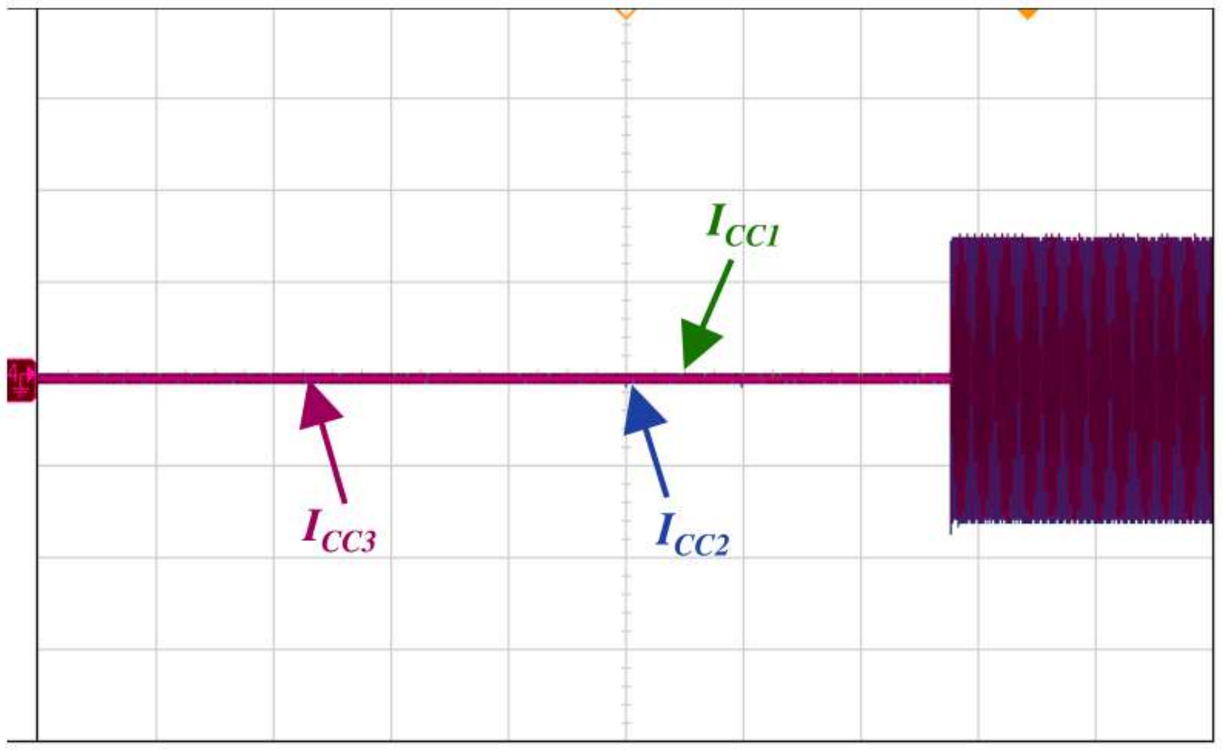


Fig. 4.38: Circulating currents

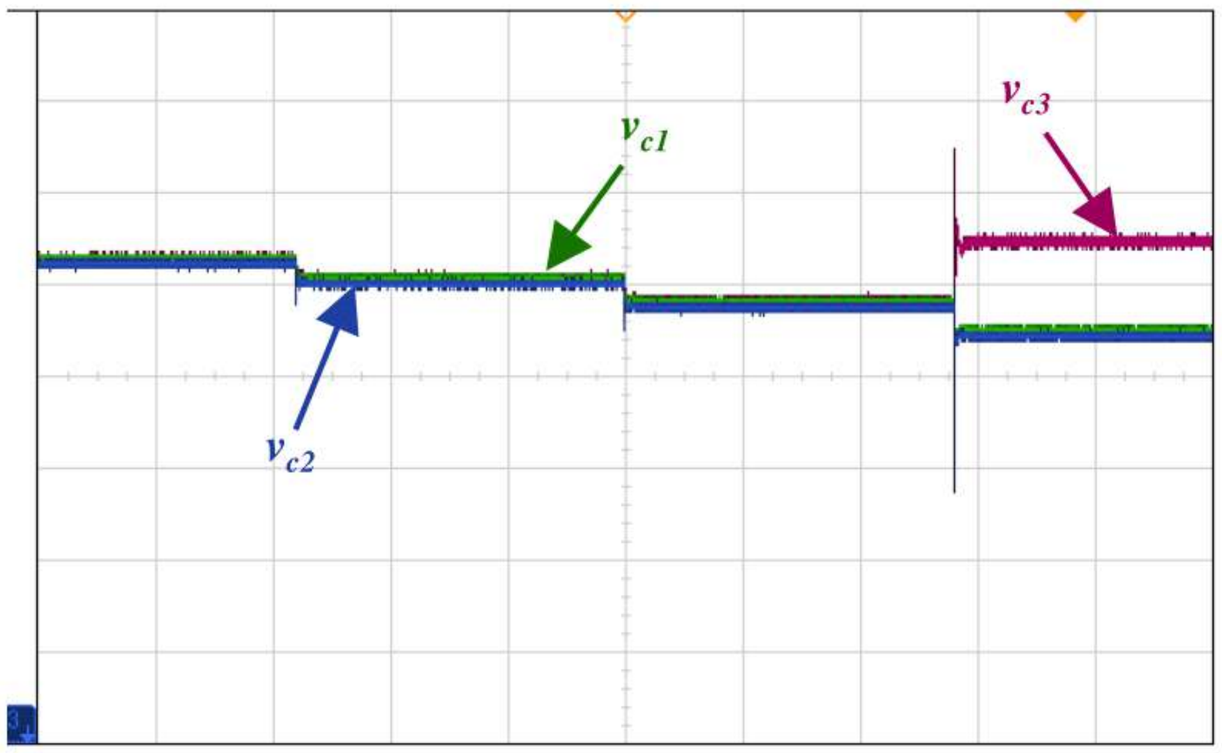


Fig. 4.39: Output RMS voltage of the three DGs

Upon scrutinizing the all-HIL real-time simulation results of the three control methods, it is observed that the HIL real-time simulation results obtained for the three control methods are found to be similar to those obtained with MATLAB/Simulink in Chapter 3. Furthermore, the HIL simulation results show the superiority of the adaptive virtual complex impedance-based droop control method under the mismatch of line impedance of three parallel DG units-based the investigated IMG. This includes power sharing, power decoupling, power overshoot reduction, and power oscillation elimination, as well as circulating current suppressions.

4.8. Conclusion

In this chapter, a detailed description of the hardware-in-the-loop (HIL) real-time simulation using the OPAL-RT OP5700 associated with the HIL controller OP8660 was presented, followed by HIL real-time simulations of the three control methods produced in Chapter 3. As a result, the HIL real-time simulation results of the three control methods demonstrate that the IMG, which is based on the adaptive virtual complex impedance-based droop control method, successfully establishes control over active and reactive power sharing, power decoupling, power oscillation elimination, and circulating current suppression. Furthermore, the validation of the proposed adaptive virtual complex impedance-based droop control method using the OPAL-RT simulator and HIL controller increased the value of its effectiveness. This implies that implementing the suggested control method-based IMG in practical applications will be easy.

General Conclusions

This master's thesis aims to enhance the control performance of VSI-based distributed generation (DG) units in an islanded microgrid, focusing on power sharing, power decoupling, power oscillation reduction, and circulating current eliminations, all while utilizing a decentralized method. The virtual impedance concept-based droop control methods are a powerful way to improve the performance and power quality of IMGs. This is especially true when power decoupling, accurate power sharing, and circulating currant suppression are very important. However, these virtual impedance-based methods also have some limitations, including increased control complexity and potential stability issues due to improper design or tuning of the virtual impedance. In this context, we investigated an adaptive virtual complex impedance-based droop control method for three VSI-based DG units in an IMG, and we validated its results using Hardwar-In-the-Loop (HIL) real-time simulation and the OPAL RT OP5700 associated with the OP8660 HIL controller.

In the first chapter of this master's thesis, a brief overview of microgrids discussed in the literature was presented, and then attention was focused on an IMG, which shows many advantages compared to the others, including improved reliability and resilience, energy efficiency and reduced transmission losses, and economic benefits, as well as its utilisation for power requirements in remote and isolated communities, critical infrastructure and facilities (hospitals, data centres, military bases, and emergency services require a highly reliable and uninterrupted power supply), and campus environments (Universities, research parks, and large commercial or industrial complexes).

In the second chapter, we presented a comprehensive analysis of a three-phase voltage source inverter (VSI) with LC filter used as a DG unit in the IMG. We divided this chapter into two main parts. In the first part, we presented the mathematical model of a VSI-based DG module, including the dynamics of both VSI output current and capacitor voltages in different reference frames (*abc*, *αβ*, and *dq*). We use the model in the dq reference frame to develop the inner voltage and current controllers, employing PI controllers to manage the output active and reactive powers and regulate the capacitor voltages. In the second part, we simulate the three phase VSI-based DG unit using the designed controllers in MATLAB/Simulink environment. Simulation results demonstrate that the VSI-based DG unit responds effectively in terms of output currents, capacitor voltages, line currents, and active and reactive powers, as well as load power requirements under any change. These results form the foundation for constructing an IMG with three VSI-based DG units in the subsequent chapter, where an advanced control method is proposed to enhance power sharing, power decoupling, and the elimination of circulating currents within the IMG.

Two virtual impedance-based droop control methods in the dq reference frame have been developed in the third chapter to enhance the control performance of the IMG and their dynamic responses, including power sharing, power decoupling, reduction of power overshoot and oscillation, and elimination of circulating current. The first droop control method is based on the complex virtual impedance concept, and the second droop control method is based on the adaptive complex virtual impedance concept. Simulation results using

MATLAB/Simulink confirm that the virtual impedance-based droop control method is completely possible for controlling the three parallel VSI-based DG units of the IMG. The method enhances power sharing, eliminates power overshoot, and eliminates circulating current in situations where line impedances are mismatches. However, the results obtained from this method demonstrate that any change in the IMG's structure, such as a change in load, swiftly erases these performances. This method's main drawback stems from the selection of the resistive and inductive values of the complex virtual impedance method in the ideal IMG scenario, rendering it incapable of adapting to any changes in the system's structure. In order to address this issue and improve the performance of the IMG, an adaptive virtual complex impedance-based droop control method based on the output reactive power and voltage amplitude of each DG unit is applied. The method's results significantly enhance the control performances of the IMG. The system shares the active and reactive powers equally with few oscillations. It also gets rid of the three DG units' reactive power errors and stops the circulating currents completely. It can be concluded that this control method yields favorable performance and notable enhancements under line impedance mismatches and load changes when compared to both the traditional droop control and the virtual complex impedance-based droop control method.

To validate and examine the performance of the adaptive virtual complex impedance-based droop control method used for controlling the three VSI-based DG units of the IMG, HIL real-time simulations of the three control methods are performed in the fourth chapter using the OPAL RT OP5700 associated with the OP8660 HIL controller. The HIL simulation results show complete similarity to those previously obtained by simulations, further demonstrating the superiority of the proposed adaptive virtual complex impedance-based droop control method. It's interesting to note that the HIL real-time simulations done with the OPAL RT OP5700 and the OP8660 HIL controller pretty much match the real-time implementations. This result indicates that the proposed control method is ready for practical implementation.

This master's thesis is open to a variety of future research avenues. We have listed some of the important aspects of future research below.

- Practical implementation of the proposed control method;
- Applications of new control methods, such as secondary control, for power sharing, voltage, and frequency stabilization;
- Improvement of the IMG systems by using new power VSIs, such as multi-leg and multi-level VSIs.

Appendix A

Table A.1. Parameters of the system

Parameter	value
Output RMS voltage V_i	325 V
Nominal frequency f	50 Hz
DC bus voltage V_{dc}	800 V
Filter inductance L_f	4 mH
Filter resistance R_f	0.05 Ω
Filter capacitor C_f	140 μF
First line impedance L_{L1}, R_{L1}	1mH, 0.05 Ω
Second line impedance L_{L2}, R_{L2}	0.5mH, 0.1 Ω
Third line impedance L_{L3}, R_{L3}	1mH, 0.1 Ω
First load L_1, R_1	50mH, 25 Ω
Second load L_2, R_2	60mH, 20 Ω
Third load L_3, R_3	70mH, 15 Ω

Table A. 2. Parameters of the MATLAB/simulations, HIL simulation, and controller algorithms.

Parameter	value
ω-P droop loop coefficient m_i	1.10^{-5}
V-Q droop loop coefficient n_i	2.10^{-4}
LPFs cut-off frequency ω_{cLPF}	15π rad/s
PIv damping factor ξv	1
PIv cut-off frequency ω_{cv}	400 rad/s
PIi damping factor ξi	1
PIi cut-off frequency ω_{ci}	4000rad/s
Initial virtual inductance L_v	0.23mH
Initial virtual resistance R_v	0.1 Ω
Adaptive virtual inductance coefficient k_{Zviri}	0.00014
Adaptive virtual inductance coefficient k_{Rviri}	0.007
Sampling time	6us

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Abstract:

Islanded microgrid (IMG) systems are recognized as adaptable small-scale power systems that integrate various forms of renewable energy resources (RESs) for electricity generation in rural areas, industrial parks, commercial, and institutional campuses, among other places. They can also incorporate energy storage systems, such as batteries, to store excess energy for later use. Other important benefits of the IMGs include lower transmission and distribution costs, greater reliability, and lower energy losses.

This master's thesis aims to enhance the control performance of VSI-based distributed generation (DG) units in an IMG under mismatches of line impedances, focusing on power sharing, power decoupling, power oscillation reduction, and circulating current eliminations, all while utilizing a decentralized method. The virtual impedance concept-based droop control methods are a powerful way to improve the performance and power quality of IMGs. This is especially true when power decoupling, accurate power sharing, and circulating currant suppression are very important. However, these virtual impedance-based methods also have some limitations, including increased control complexity and potential stability issues due to improper design or tuning of the virtual impedance. In this context, an adaptive virtual complex impedance-based droop control method for three VSI-based DG units in an IMG based on the output reactive power and voltage amplitude of each DG unit is proposed.

To validate and examine the performance of the adaptive virtual complex impedance-based droop control method used for controlling the three VSI-based DG units of the IMG, simulation using MATLAB/Simulink and Hardwar-In-the-Loop (HIL) real-time simulations of the three control methods using the OPAL RT OP5700 associated with the OP8660 HIL controller are performed. Both simulation and HIL real-time simulation results demonstrate that the proposed method can significantly enhance the control performances of the IMG. The system shares the active and reactive powers equally with few oscillations. It also gets rid of the three DG units' reactive power errors and stops the circulating currents completely.

Keywords: Islanded microgrid (IMG); Renewable energy resources (RESs); Distributed generation (DG); Voltage source inverter (VSI); Adaptive virtual complex impedance-based droop control method; Power sharing; Hardwar-In-the-Loop (HIL) real-time simulation; OPAL RT OP5700.

ملخص:

تُعرف أنظمة الشبكات الصغيرة الجزرية (IMG) بأنها أنظمة طاقة صغيرة الحجم قابلة للتكيف والتي تدمج أشكالًا مختلفة من موارد الطاقة المتجددة (RESs) لتوليد الكهرباء في المناطق المعزولة مثل الارياف، المجمعات الصناعية، الحرم الجامعي، والمؤسسات التجاري. ويمكنها أيضًا دمج أنظمة تخزين الطاقة، مثل البطاريات، لتخزين الطاقة الزائدة لاستخدامها لاحقًا. تشمل الفوائد الهامة الأخرى لـ IMGs انخفاض تكاليف النقل والتوزيع، وزيادة الموثوقية، وانخفاض خسائر الطاقة.

تهدف رسالة الماجستير هذه إلى تعزيز أداء التحكم في وحدات التوليد الموزعة (DG) القائمة على المقومات ثلاثية الطور VSI في IMG في ظل عدم تطابق ممانعات الخط، مع التركيز على تقاسم الطاقة، وفصل الطاقة، وتقليل تذبذب الطاقة، وإزالة التيار المتداول بين المقومات. تعد طرق التحكم في التدلي القائمة على مفهوم المعاوقة الافتراضية المركبة ذات القيم الثابتة طريق قوية لتحسين الأداء وجودة الطاقة لـ IMGs وهذا صحيح بشكل خاص عندما يكون فصل الطاقة، وتقاسم الطاقة الدقيق، وقمع الكشمش المنتشر أمرًا مهمًا للغاية. ومع ذلك، فإن هذه الأساليب المعتمدة على المعاوقة الافتراضية المركبة ذات القيم الثابتة لها أيضًا بعض القيود، بما في ذلك زيادة تعقيد التحكم ومشكلات الاستقرار المحتملة بسبب التصميم غير المناسب في ضبط قيم المعاوقة الافتراضية. في هذا السياق، تم اقتراح طريقة جديدة تعتمد على المعاوقة الافتراضية المركبة من مقاومة و وشيعة ذات القيم المتغيرة للتحكم في التدلي لثلاث وحدات DG قائمة على VSI في IMG استنادًا إلى القدرة التفاعلية الناتجة وسعة الجهد لكل وحدة DG.

ولتحقق من صحة وفحص أداء طريقة التحكم في التدلي المعتمدة على المعاوقة المركبة من مقاومة و وشيعة ذات القيم المتغيرة المستخدمة للتحكم في وحدات DG الثلاث المستندة إلى VSI لـIMG، بالاضافة الى المحاكاة باستخدام MATLAB/Simulink -تم إجراء عمليات محاكاة زمنية و Hardwar-In-the-Loop (HIL) باستخدام OPAL RT OP570 المرتبط بوحدة التحكم OP8660 HIL لطرق التحكم الثلاثة .توضح كل من نتائج المحاكاة باستخدامMATLAB/Simulink ومحاكاة HIL في الوقت الفعلي أن الطريقة المقترحة يمكن أن تعزز بشكل كبير أداء التحكم فيIMG.حيث يتم توزيع الطاقة بالتساوي بين كل التوليد و التوزيع DGs مع وجود تذبذبات قليلة. كما أنه يتخلص من أخطاء الطاقة التفاعلية لوحدات DG الثلاث ويوقف التيارات الدائرية المتداولة بين المقومات بشكل كامل.

الكلمات المفتاحية: شبكة الجزر الصغيرة(IMG) ؛ موارد الطاقة المتجددة (RESs)؛ وحدات التوليد و التوزيع (DG)؛ مقومات ثلاثية الطور(VSI) ؛ طريقة التحكم في التدلي المعتمدة على المعاوقة الافتراضية المركبة ذات القيم المتغيرة، تقاسم الطاقة بالتساوي؛ محاكاة-Hardwar In-the-Loop (HIL) في الوقت الحقيقي؛ OPAL RT OP5700.