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Présentée Par

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Abstract

In recent decades, the depletion of fossil energy resources has become commonplace. This depletion results in an ever-increasing expense of energy. Furthermore, these fossil energy resources are frequently blamed for being the main cause of global warming. This challenge necessitates the search for a feasible substitute for these fossil energy resources. On the other hand, a growing interest in the development of new technologies for the exploitation of renewable energy sources due to their technology maturation and low cost. Therefore, utilizing renewable energy for electricity production has become a popular solution. One of these solutions is the Microgrid system concept, which is particularly compatible and beneficial to electricity generation as well as the integration of renewable sources and energy storage systems. Despite the benefits of the DC Microgrid system, constant power loads provide a stability challenge due to the incremental negative impedance of their loads. This negative incremental impedance (INI) decreases the damping factor of the DC Microgrid, resulting in an undamped oscillation in the output current and voltage. As a result of these undamped oscillations, the DC Microgrid becomes unstable. This thesis treats the study and implementation of a DC Microgrid supplying constant power load (CPL), in which a boost converter with a tightly regulated output voltage emulates the CPL. This thesis work proposes a robust nonsingular terminal sliding mode controller to stabilize the system by avoiding the INI characteristic and conserving energy availability. The robust non-singular terminal sliding mode controller is characterized by the avoidance of the singularity problem that occurs by the traditional terminal sliding mode controller.

Apart from the challenge of the DC MG supplying a CPL, the power sharing issue between the distributed power systems that comprise the DC MG is also addressed. Using a case study of two paralleled buck converters supplying a single resistive load, the power-sharing problem is addressed utilizing a primary control level (Droop control method). The primary control level has been carried out using PI controllers for current and voltage regulation, as well as the addition of a virtual resistive load to avoid current circulation. The suggested controllers are confirmed using simulations and an experimental setup.

Keywords: DC Microgrid, droop control, constant power loads, power sharing, incremental negative impedance, terminal sliding mode, Nonsingular terminal sliding mode controller, singularity problem, PI controller.

Résumé

Au cours des dernières décennies, l'épuisement des ressources énergétiques fossiles est devenu monnaie courante. Cet épuisement se traduit par des dépenses d'énergie toujours plus importantes. En outre, ces ressources énergétiques fossiles sont souvent accusées d'être la principale cause du réchauffement climatique. Ce défi nécessite la recherche d'un substitut réalisable à ces ressources énergétiques fossiles. D'autre part, un intérêt croissant pour le développement de nouvelles technologies pour l'exploitation des sources d'énergie renouvelables en raison de leur maturation technologique et de leur faible coût. Par conséquent, l'utilisation des énergies renouvelables pour la production d'électricité est devenue une solution populaire. L'une de ces solutions est le concept de système Microgrid, qui est particulièrement compatible et bénéfique à la production d'électricité ainsi qu'à l'intégration de sources renouvelables et de systèmes de stockage d'énergie. Malgré les avantages du système de micro-réseau à courant continu, les charges à puissance constante posent un problème de stabilité en raison de l'impédance négative incrémentale de leurs charges. Cette impédance négative incrémentielle (INI) diminue le facteur d'amortissement du micro-réseau DC, ce qui entraîne une oscillation non amortie du courant et de la tension de sortie. En raison de ces oscillations non amorties, le micro-réseau DC devient instable. Cette thèse traite de l'étude et de l'implémentation d'un micro-réseau DC alimentant une charge à puissance constante (CPC), dans lequel un convertisseur boost avec une tension de sortie étroitement régulée émule la CPC. Ce travail de thèse propose un contrôleur robuste à mode glissant terminal non singulier pour stabiliser le système en évitant la caractéristique INI et en conservant la disponibilité énergétique. Le contrôleur robuste à mode glissant terminal non singulier est caractérisé par l'évitement du problème de singularité qui se produit avec le contrôleur à mode glissant terminal traditionnel.

Outre le défi que représente l'alimentation d'un CPC par le Micro-réseau DC, le problème du partage de la puissance entre les systèmes d'alimentation distribués qui composent le Micro-réseau est également abordée. En utilisant une étude de cas de deux convertisseurs buck en parallèle alimentant une charge résistive unique, le problème du partage de la puissance est abordé en utilisant un niveau de contrôle primaire. Le niveau de contrôle primaire a été réalisé en utilisant des contrôleurs PI pour la régulation du courant et de la tension, ainsi que l'ajout d'une charge résistive virtuelle pour éviter la circulation du courant. Les contrôleurs proposés sont validés par des simulations et un montage expérimental.

Mots clés : Micro-réseau DC, charges à puissance constante, partage de puissance, impédance négative incrémentielle, mode glissant terminal, contrôleur de mode glissant terminal non singulier, problème de singularité, contrôleur PI.

Acronyms

DC MG: DC Microgrid.

AC MG: AC Microgrid.

CPL: Constant Power Load.

RES: Renewable Energy Sources.

PWM: Pulse Width Modulation.

CCM : Continuous Conduction Mode.

DCM : Discontinuous Conduction Mode.

VDC: Voltage Direct Current.

ESS: Energy Storage System.

SMC: Sliding Mode Control.

VSS: Variable Structure Systems.

TSM: Terminal Sliding Mode.

NTSM: Nonsingular Terminal Sliding Mode.

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General Introduction

In recent years, there has been a growing interest in the development of new technologies for the production and distribution of electric energy in order, on one hand, to evolve towards more efficient and reliable systems and, on the other hand, accelerate the deployment of renewable energy sources to reduce greenhouse gas emissions. This strategic vision of changing the old paradigm of energy production and distribution towards a new one based on distributed electric energy production, quickly motivated the scientific community to investigate and develop the concepts of micro-grids. Moreover, as energy production in the distributed paradigm is consumed locally; i.e. the installations are close to final consumers for a more reliable and efficient power supply, they also contribute to making the energy delivery more secure and lossless. The concept of microgrids (MGs) is a promising solution that can provide substantial support to the old power system paradigm in terms of energy efficiency and reliability. Moreover, this new paradigm can be an effective way to promote and accelerate the deployment of renewable sources and energy storage systems. On the other hand, the low cost of installation and operability, the high energy efficiency, and the simplicity of their concept is considered among many other merits that make the MGs features very attractive [1], [2].

According to several reports and research papers related to the concepts of MGs, it appears clearly that DC MGs have gained much focus and interest over the remaining types of MGs. This is mostly owing to the advantages that DC MGs provide in terms of high reliability, ease of integration, and cost-effectiveness. Furthermore, problems inherent to AC buses such as harmonic content, synchronization issues, and control complexity are further arguments that consolidate the focus and interest in DC MGS [3]. Moreover, the absence of reactive power in a DC microgrid makes it more efficient and reliable compared to the AC one. Indeed, a DC microgrid has only active power transmitted in the lines, thus reducing the wire sizing while an AC microgrid has to consider the presence of reactive power leading to the need to oversize the DC link capacitor and the inverter, as well as considering the losses in the transmission line. Therefore, contrary to what happens in the AC microgrid, there is no increase in power loss in the lines due to nonlinear load, in either the transformer nor the converter. That improves greatly the efficiency and reliability of a DC microgrid compared to the AC one. Besides, electronic loads in domestic applications are DC native and they are preponderant. For instance, led lighting, laptops, computers, mobile phones, and televisions use an adapter including a rectifier in order to be supplied from the AC grid. As for resistive loads such as

heating and universal motor based appliances such as mixers and vacuum cleaners, they can operate on both AC and DC power. Hence integrating these home appliances into a DC-based power system will also result in reducing the power conversion stages while increasing efficiency and reliability. For all the above-mentioned reasons, DC microgrids have been substantially investigated and studied in many research groups. However, despite the aforementioned advantages of DC MGs, there are still some challenges related to the proliferation of new kinds of loads that can threaten the overall stability of the DC MG. For instance, constant power loads (CPL) are one of the loads that threaten the overall stability of a DC MG. Serially connected DC-DC converters, one as a feeder and the second one as a load with the output voltage tightly regulated behaves as a CPL [4-6]. For this reason, a DC MG feeding a CPL takes the interest of thesis work.

Main contributions:

The main contributions of the thesis are presented in the following points:

- The primary control level using a droop control method is performed, taking a case study of two DC-DC Buck converters feeding a single resistive load. This strategy allows current sharing between buck converters as well as regulating output voltages.

- Nonsingular terminal sliding mode and sliding mode controllers are suggested to stabilize a DC-DC Buck converter supplying a tightly controlled boost converter (acting as a CPL). These improved controllers maintain the system stable in the presence of external fluctuations in the input voltage and power load demand.

- Experimental validation of the suggested controllers based on DSP delfino TMS320F28335.

Publications:

These results are presented in the following publications:

- **Journal papiers**

1. K. Louassaa, A. Chouder, and C. Rus-Casas, “Robust Nonsingular Terminal Sliding Mode Control of a Buck Converter Feeding a Constant Power Load,” Electronics, vol. 12, no. 3, p. 728, Feb. 2023, doi: 10.3390/electronics12030728.

2. M. Boukerdja, A. Chouder, L. Hassaine, B. Ould Bouamama, W. Issa, and K. Louassaa, "H∞ based control of a DC/DC buck converter feeding a constant power load in uncertain DC microgrid system," ISA Transactions, vol. 105, pp. 278–295, Oct. 2020.

- **International conferences:**

1. K. Louassaa, A. Chouder, M. Boukerdja, A. Cherifi, and A. Aillane, “An Enhanced Primary Control Level for a DC Microgrid Systems,” 2022 19th International Multi-Conference on Systems, Signals & Devices (SSD), May 2022, doi: 10.1109/ssd54932.2022.9955650.
2. M. Boukerdja, A. Chouder, and K. Louassaa, “Realizing the Accurate power sharing in DC Microgrid Using Droop Control Strategy,” 2019 International Conference on Advanced Electrical Engineering (ICAEE), Nov. 2019, doi: 10.1109/icaee47123.2019.9014692.
3. A. Cherifi, A. Chouder, A. Kessal, A. Hadjkaddour, A. Aillane, and K. Louassaa, “Control of a Voltage Source Inverter in a Microgrid Architecture using PI and PR Controllers,” 2022 19th International Multi-Conference on Systems, Signals & Devices (SSD), May 2022, doi:10.1109/ssd54932.2022.9955891.
4. K. Louassaa, A. Chouder, M. Boukerdja, A. Cherifi and A. Aillane, "Sliding Mode Control for a DC-DC Buck Converter Feeding a Constant Power Load: A Practical Implementation," 2022 International Conference of Advanced Technology in Electronic and Electrical Engineering (ICATEEE), M'sila, Algeria, 2022, pp. 1-5, doi: 10.1109/ICATEEE57445.2022.10093728.

5. A. Cherifi, A. Chouder, A. Kessal, A. Hadjkkadour, A. Aillane and K. Louassaa, "Control of Stand-Alone Inverter using Virtual Synchronous Generator," 2022 International Conference of Advanced Technology in Electronic and Electrical Engineering (ICATEEE), M'sila, Algeria, 2022, pp. 1-6, doi: 10.1109/ICATEEE57445.2022.10093091.

Organization of thesis manuscript:

The manuscript is organized as follows:

- **Chapter 1** presents an overview of Microgrid state of the art, including its available types, architectures, and control methods. This chapter also goes into detail about the DC MG issues that are available, such as the current circulation problem and the INI characteristic of CPL.

- **Chapter 2** presents the process to design the primary control level used for a DC MG feeding a resistive load. This chapter also goes over traditional controllers such PI, type 2, and type 3. The primary control level is validated by a simulation study using PSIM software.

- **Chapter 3** presents the approach to designing the SMC and NTSM controllers used for the output voltage regulation of a DC-DC Buck converter feeding a CPL. These proposed controllers aim to ensure the robustness of the buck converter against perturbations caused by the INI characteristic of CPL and external disturbances. The simulation study is carried out using PSIM software to validate the suggested approaches.

- **Chapter 4** presents the experimental validation of the primary control level of the DC MG under several scenarios. This chapter also includes experimental validation of the proposed NTSM controller and SMC for a buck converter feeding a CPL.

Chapter 1: Context and state of the art of Microgrid systems

1.1. Introduction

Energy has long been acknowledged as necessary for humanity's progress and flourishing, but the approval in 2015 of the new United Nations Sustainable Development Goals (SDGs) as part of the 2030 Agenda signified a new level of governmental awareness of the significance of energy to development [7]. The SDGs were accepted by UN member states from 193 nations, both developed and developing, and contain, for the first time, an aim to provide access to cheap, dependable, sustainable, and modern energy for everyone [8].

Recently, much attention has been paid to the advancement of new technologies for the generation and distribution of electric energy in order, on the one hand, to develop more efficient and reliable systems aimed at providing energy for everyone and, on the other hand, to speed up the implementation of renewable energy sources in order to decrease emissions of greenhouse gases [9-12].

This strategic goal of rapidly transitioning the old energy production and distribution model to a new one based on distributed electric energy generation drove the scientific community to explore and develop micro-grid technologies. Our major focus in this thesis is on the deployment of DC Microgrid systems and resolving the issues of control and loads.

As a result, in this chapter, we will examine the state of the art in microgrids while explaining our selection of DC microgrids and addressing the many types of DC microgrids and their control levels.

1.2. Microgrid definition

A microgrid, as defined by the US Department of Energy Microgrid Exchange Group, is a combination of interconnected distributed energy resources, energy storage systems, and loads connected via a bus, which act as a single controllable unit. A microgrid can connect and disconnect from the grid to enable it to operate in both grid-connected or island-mode [13].

Microgrids, according to the CIGRÉ C6.22 Working Group, are defined as distribution systems of electricity that include distributed energy resources and loads, in particular, energy storage systems and distributed generators, and controlled loads, which can act as a controlled unit. Microgrids can operate in network or island mode [14].

In summary, a microgrid is a controlled unit autonomous power system that can perform in either connected or disconnected mode and is constituted of distributed generation (DG), loads, and energy storage systems (ESS) associated in parallel via a bus.

Despite the benefits of large-scale electrical grids that have served citizens for decades, the microgrids concept has attracted increasing attention in recent years. The power consumed in

large-scale electrical grids is generated by fossil fuels (such as coal, gas, nuclear ...etc.) in order to supply many cities with their electricity needs. On the contrary, in the concept of microgrids, power is consumed locally, i.e. the installations are close to consumers to a more reliable and efficient system while reducing losses generated by the distribution and transport processes.
Furthermore, a single faulty part in a large-scale electrical grid can affect a large area of the grid, whereas in a microgrid system, it only affects a small area of the grid, i.e. fewer consumers.

1.3. The fundamental components of a microgrid

A microgrid's major components are distributed generators, energy storage systems, and controlled or uncontrolled loads connected via a bus. The Microgrid concept can be connected to the grid but can also disconnect, i.e. operate as an island mode as needed, as maintained in the previous definition.
Within the context of a microgrid, distributed generators (DGs) act as an energy producer, which can be any energy source such as photovoltaic arrays, wind turbines, diesel generators, etc. DGs are connected via power converters to produce an appropriate voltage and current for the microgrids process.
Energy storage systems provide a broad array of technologies used for managing the export/ import of energy from/ to the network. Many forms of energy are used in these storage technologies, including chemical, thermal, nuclear, electrical, motion, gravitational, elastic, and radiant energy. Batteries, flywheels, thermal energy storage systems, ultra-capacitors, pumped-hydro systems, and other storage technologies are examples. In short, energy storage systems (ESS) are important for compensating for power shortages in microgrid systems. It can also protect the microgrid from transient instability by supplying transient power during the transient.
Loads (whether controlled or uncontrolled) can play an important role in microgrid systems in terms of variability in low-power systems, which in turn can be more extreme in the systems of utility grid. Because of this variability, the overall system may become unstable.
Depending on the type of microgrid, the interconnection of the previously mentioned elements is accomplished via a bus, which can be either an AC or a DC link.

1.4. Microgrid types and architecture

Various configuration criteria, such as the type of energy sources, the number of energy sources, the type of bus, and the interaction with the grid, can be used to determine the architecture and types of microgrid. The microgrid can be defined as renewable, conventional, or hybrid based on the type of energy sources used.

The microgrid system can be classified as an individual-source, multi-source, or hybrid generation microgrid based on the number of energy sources. The microgrid system can be categorized as either self-connected or grid-connected based on its interaction with the power network. In terms of energy backup systems, the microgrid system can be defined as one in which the grid acts as an energy backup in order to continue supplying power. This system can be an emergency plant that acts as the system of energy backup, or it can be a microgrid system with ESS that acts as the system of energy backup.

Moreover, microgrids are categorized as AC, DC, or hybrid AC/DC microgrids based on the type of bus. This classification is explained in greater detail in the subsection that follows.

1.4.1. AC microgrid

Due to the increased demand for high reliability, there is a growing interest in AC Microgrid system studies and implementation, owing to its benefits in terms of the maturity of the AC distribution system [15]. Considering the maturity of the AC network in terms of infrastructure, production, and distribution, its design and implementation are becoming more prevalent. The structure of an AC microgrid is depicted in Fig. 1.1, which illustrates the commonly used architecture that is characterized by an AC Bus type. As a result, inverters are used to generate and distribute alternating current (AC).

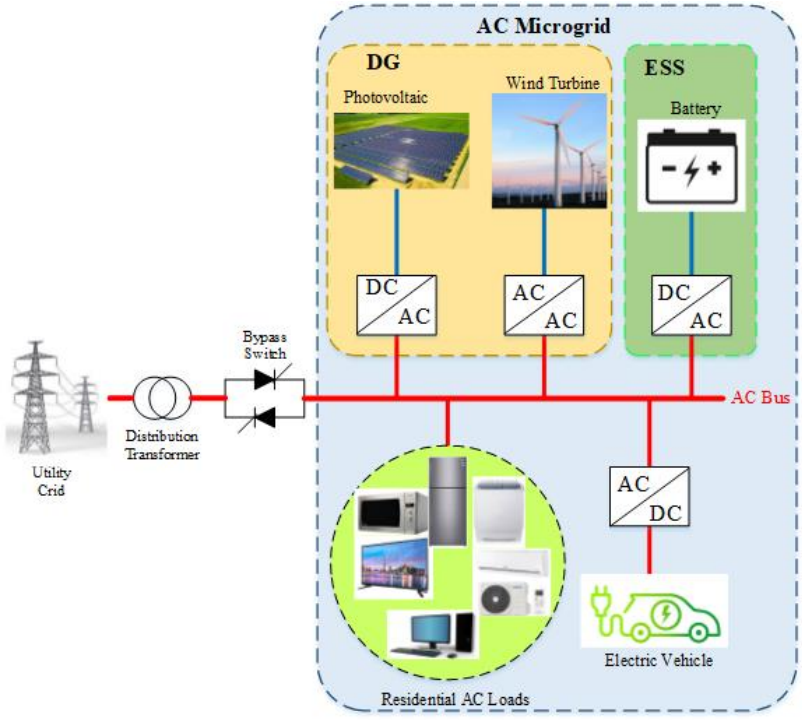


Fig. 1.1. The structure of AC Microgrid

1.4.2. DC microgrid

A DC microgrid has a DC bus that supplies power to the various DC loads connected to it. In comparison to the benefits of the AC microgrid, the DC microgrid has a higher efficiency due to the reduction of power converter stages operations [15]. Furthermore, due to the prevalence of electronic appliances of the DC native type in the residential domain, as well as, the ease of storage energy in DC form compared to the AC one, DC Microgrid has gained increasing traction. Fig. 1.2 shows an example of a residential DC microgrid, which expands on the use of existing DC battery storage.

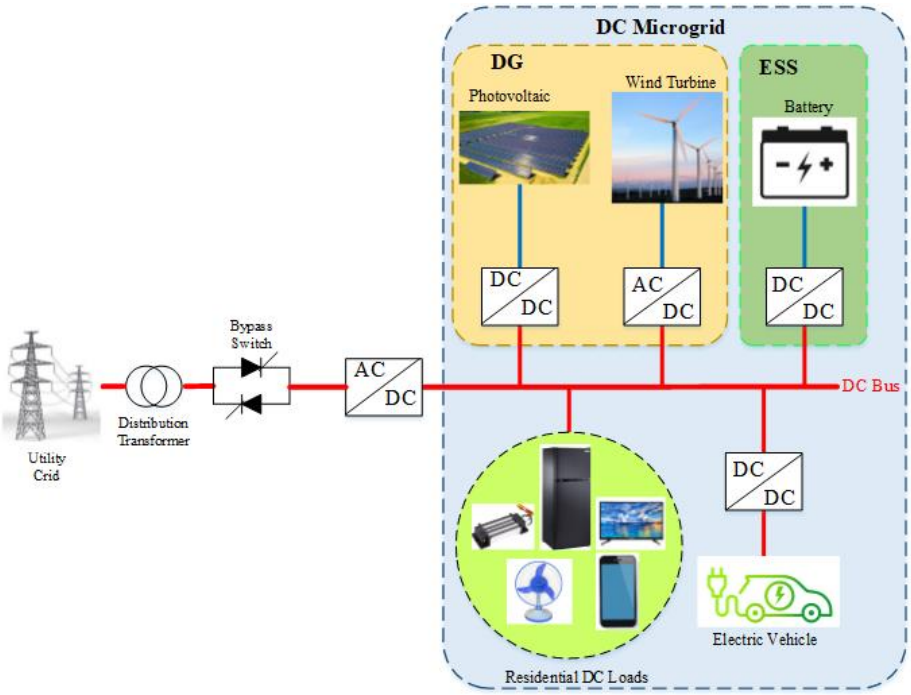


Fig. 1.2. The structure of DC Microgrid

1.4.3. Hybrid AC/DC microgrid

As the name implies, a hybrid AC/DC microgrid has a DC Bus and an AC Bus, as shown in Fig. 1.3. This type of microgrid combines the benefits of both AC and DC microgrids. The hybrid AC/DC microgrid eliminates multiple power conversions in AC or DC microgrids and enables the simultaneous connection of variable AC and DC sources and their corresponding loads.

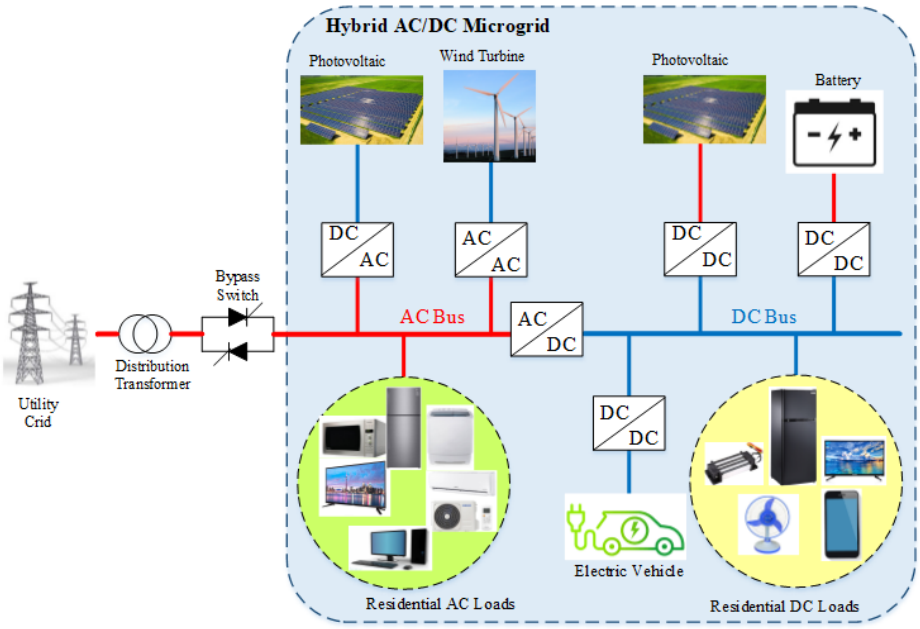


Fig. 1.3. The structure of Hybrid AC/DC microgrid

1.5. Control methods of microgrid

Once delving into the specifics of microgrid control, consider the following roles:

-Regulating the output voltage fluctuations of the converter connected to the bus.

- Guaranteeing an even and stable current sharing between the various parallel line-controlling converters.

- Assuring the desired power flow (i.e. from/to the microgrid) while being economically and technically viable.

- Working to ensure the possibility to transparently add or remove a new element from the microgrid, i.e. guaranteeing the microgrid elements' plug-and-play operation.

Sharing of the active load and droop control are two types of regulation methods characterized by the operating mechanism control of current redistribution and output voltage control. Each one of these controls is applied on the system hierarchically in three control loops, which are:

- The tertiary control loop, which includes an energy management operation, regulates the flow of power from and toward the microgrid systems with the goal of sharing the same power among the various distributed generators, transferring power between the utility grid and the microgrid systems, islanding and interconnection management, and optimizing variables such as cost and efficiency.

-The secondary control loop's objective is to restore the output voltage or frequency, compensate for harmonics, regulate voltage unbalance, and maintain synchronization between the utility grid and the microgrids, which is especially important for AC microgrids.

-The primary control loop provides a solution for distributing demand power among the DGs with the goal of reducing current circulation caused by voltage differences in parallel converters.

For microgrids to function properly, the time scale of the hierarchical control structure is increased as the control level increases, with upper-class control providing references for lower-class control. Fig. 1.4 depicts this hierarchical control structure.

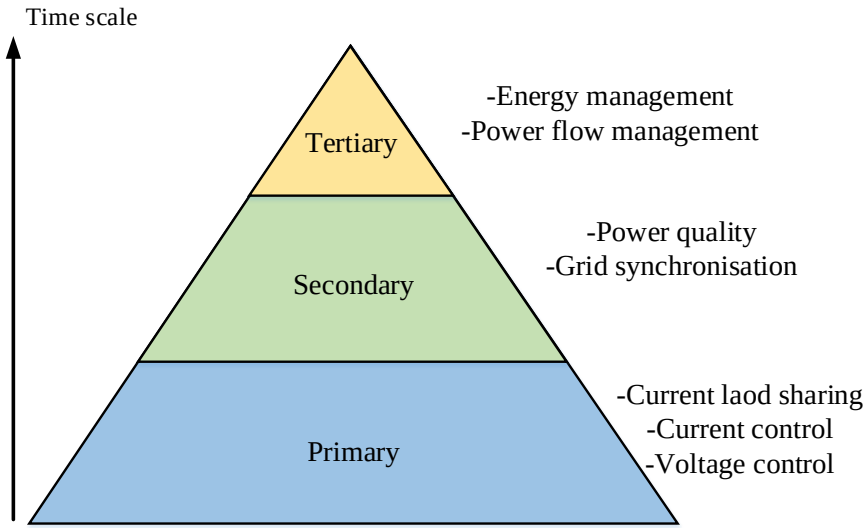


Fig. 1.4. Hierarchical control structure of Microgrid

1.6. Why DC Microgrid?

AC microgrid seems to be the first choice when it comes to residential application since traditionally, distribution systems for this field are generally in AC form. Nonetheless, the situation has changed, and DC-based power systems now provide more benefits in terms of simplicity, cost reduction, and efficiency enhancement [15]. Due to benefits such as high dependability, ease of integration, low cost, and simplicity of control, DC microgrid is a popular recent use of DC-power systems. For this reason, DC Microgrid concepts have received more attention than AC Microgrid concepts. Indeed, using a DC microgrid reduces the number of power converters used in power conversion operation, which leading to improve the overall efficiency and resulting in a significant reduction in system size while remaining cost-effective. When compared to AC Microgrid, DC Microgrid control is less complex because it only needs

to stabilize the voltage, whereas AC Microgrid must also deal with frequency stabilization. Furthermore, problems associated with AC buses, such as harmonic content and synchronization issues, are not present in the DC Microgrid, making it more efficient and reliable than the AC Microgrid. In addition, in DC Microgrid, active power is the only power transmitted through the lines, whereas in AC Microgrid, reactive power must be considered. This necessitates oversizing the DC link capacitor and the inverter, as well as accounting for transmission line losses. Moreover, harmonic current problems caused by nonlinear loads do not occur in DC microgrids. Therefore, compared to AC Microgrid, the power loss caused by nonlinear loads is not found in the transformer or the converter in DC Microgrid. When compared to an AC microgrid, this significantly enhances the efficiency and reliability of the DC microgrid. Also, in the domicile, technological devices such as laptops, computers, LED lighting, televisions, and mobile phones are mostly DC native and require a rectifier to be powered by the AC grid. As a result, integrating these home appliances into a DC-based power system will result in fewer power conversion stages while enhancing efficiency and reliability. For all of the aforementioned reasons, DC microgrids have been extensively researched and studied in numerous research groups and have been chosen to be implemented in this study.

1.7. DC microgrid instability

Despite the benefits of DC MGs mentioned above, there are some challenges associated with the proliferation of new types of loads that can threaten the overall stability of the DC MG. Constant power loads (CPL), for example, are one of the loads that threaten the overall stability of a DC MG. These loads are connected to a power electronic interface, which regulates their output voltages so that the entire controlled system appears to be drawing constant power.

1.7.1. The main causes of instabilities in distributed power system

The effect of paralleling subsystems that will interact with each other causes the problem of instability in distributed power systems. When two distributed power systems *Q'* and *Q''* are considered in parallel, as shown in Fig. 1.5, their cascading results in the following transfer function:

$$H(s) = \frac{H'(s)H''(s)}{1+\frac{Z_o}{Z_{in}}} \tag{1.1}$$

where:

H'(s): Upstream distributed power transfer function of *Q'*

H''(s): The downstream subsystem's transfer function of *Q''*

H(s): The cascading transfer function of *Q'* and *Q''*

Z_{in} : The output impedance of the system *Q''*

Z_o : The input impedance of the system *Q'*

When the stability of two distributed power cascade associations is determined, the loop gain Z_o/Z_{in} determines their stability. This gain is defined as the impedance ratio T_m between the two distributed power systems.

$$T_m = \frac{Z_o}{Z_{in}} \tag{1.2}$$

The whole system will be stable if and only if the condition $|Z_{in}| >> |Z_o|$ can be guaranteed for all frequencies. Even so, in a system consists of various distributed power systems, this condition is not always achieved. As a result, an appropriate stability method is required to ensure the stability of the distributed power system, as discussed in section 1.7.3.

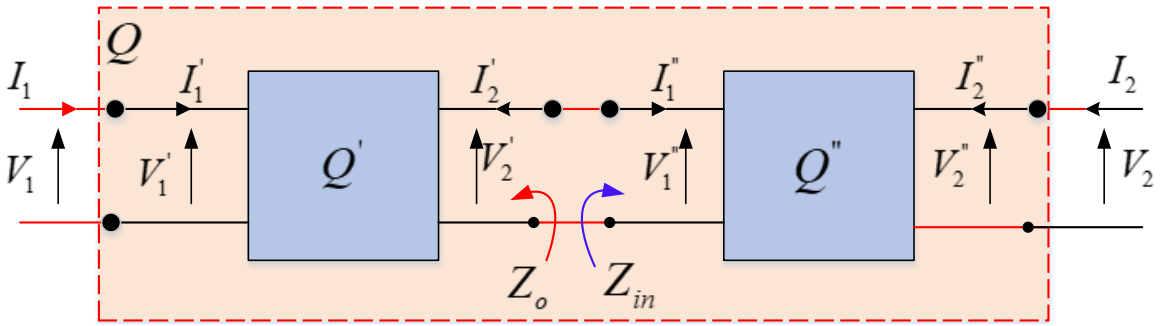


Fig. 1.5. Distributed power systems in parallel

1.7.2. CPLs and instability

In general, the behavior of constant power loads (CPLs) occurs in loads that necessitate the use of a tightly controlled regulator. When the frequency of a DC-DC converter operating in continuous conduction mode (CCM) and feeding a CPL is lower than the cut-off frequency of

the converter's voltage loop, the input impedance is equivalent to a negative resistance. However, when the frequency is greater than the cut-off frequency, this input impedance becomes equivalent to an inductance [16], [84].

The consumed power within the controller bandwidth for a CPL is constant, and its relationship is given by:

$$P_{CPL} = v \ .i = Cte \tag{1.3}$$

Where P_{CPL} : power absorbed by the CPL

v : the CPL's input voltage

i : the CPL's consumed current

By deriving the CPL current by respect to its voltage, and by inverting the result, the expression of the incremental impedance of the CPL is obtained as follow:

$$\frac{dv}{di} = -\frac{v}{i} = -\frac{P_{CPL}}{i^2} = -\frac{v^2}{P_{CPL}} \tag{1.4}$$

Thus

$$\frac{dv}{di} = -R_{CPL} < 0 \tag{1.5}$$

Equation (1.5) demonstrates that CPLs cause incremental negative impedance (INI), as shown in Fig. 1.6, which depicts the CPL characteristic in the context of a *V-I* graph.

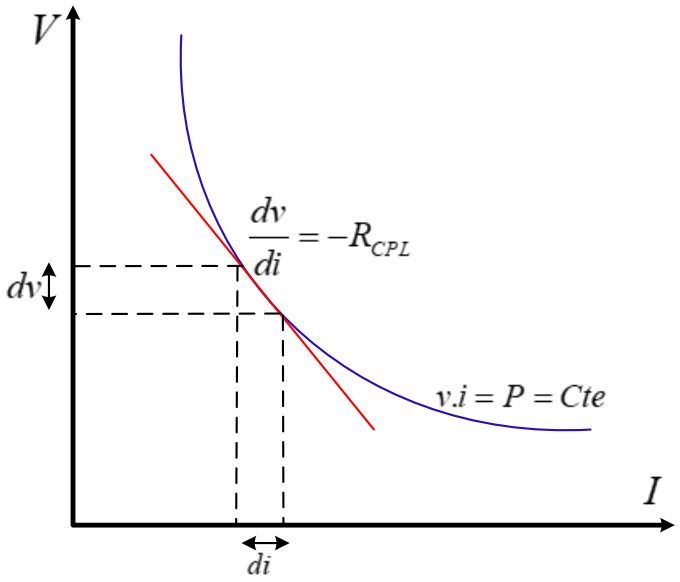


Fig. 1.6. The constant power load behavior of serially connected DC-DC converters

CPL has a -180° phase in the Bode diagram due to its negative incremental impedance. As a result, if the output impedance module of the source converter intersects the input impedance module of the CPL while the source converter's cut-off frequency is lower than the CPL's, instability occurs. Furthermore, the INI characteristic affects power quality and overall system performance [16].

1.7.3. Stability analysis tools

There are two methods for assessing the stability: 1- determining stability using the gain of minor loop, which is based on the relationship between source and load impedance [17-20]. 2- Utilizing a model of the system's appropriate state space to analyze stability [21-24].

The minor loop gain technique of stability analysis divides the system into two subsystems at an arbitrary DC point: source subsystem and load subsystem. By deriving the expressions for the load's input impedance Z_L and the source's output impedance Z_s. Assuming that both the load and source subsystems are individually well designed and perform admirably in terms of performance, the value of the minor loop Z_s/Z_L must meet the Nyquist criterion stability to ensure the overall system's stability. By paralleling all of the distributed generator's output impedances, the source's output impedance Z_s is calculated. Similarly, the load's input impedance represents the equivalent input impedance of all load subsystems with their respective input filters.

In contrast, using a model of the system's appropriate state space to analyze stability computes the eigenvalue of the overall system's Jacobian matrix using the first Lyapunov method in order to assess the overall system's asymptotic stability. This method takes into account both the power system's state equations and the controllers.

The benefit of conducting stability determination using the gain of the minor loop is that it ensures the individual stability of the system's components, which then induces the overall system's stability. Despite the benefits of conducting stability determination using the gain of the minor loop, linearization based on the average model of the system reduces system accuracy, i.e. the accuracy with which system dynamics can be described for all operating points is limited.

In terms of stability analysis using the first Lyapunov method, taking into account the system's nonlinearity is the main advantage of this method, which has higher accuracy and a wider range of system operations. However, this method has a disadvantage in terms of system complexity, i.e. the higher the relative degree of the system, the greater the system's complexity.

1.8. Load sharing problems in a DC microgrid

Despite the benefits of DC Microgrid, current sharing is the main constraint in DC Microgrid. In this section, we will examine current-sharing issues in DC Microgrid systems and discuss some current-sharing approaches proposed in the literature.

1.8.1. Causes of the load-sharing problem

If the output voltage of each distributed generator (DG) connected in parallel in a DC Microgrid cannot be adjusted, both DG interruption and load change can cause a power imbalance affecting the DC bus voltage and power quality of the entire DC MG and causing circulating currents to appear. Take into account the simplified configuration shown in Fig. 1.7 for analyzing the appearance of circulating currents, which involves two sources operating in parallel, each with its own cable resistance and connected to a resistive load [83].

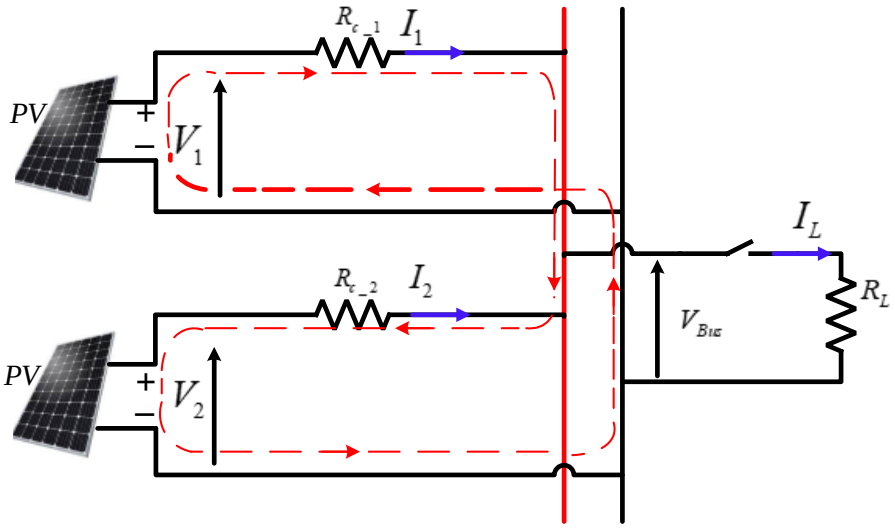


Fig. 1.7.The phenomenon of circulating current caused by two sources operating in parallel and sharing the same resistive load

Using Kirchhoff's law, we get the following equations:

$$V_1 - R_{c\_1} I_1 - R_L I_L = 0 \tag{1.6}$$

$$V_2 - R_{c\_2} I_2 - R_L I_L = 0 \tag{1.7}$$

$$I_L = I_1 + I_2 \tag{1.8}$$

By replacing I_L with its expression in (1.6) and (1.7), one can obtain the expressions of the currents I_1, I_2 of each circuit branch including a source and the circulating current $I_{c\_1,2}$ between these sources [83].

$$I_1 = \frac{\left(R_{c\_2} + R_L\right)V_1 - R_L V_2}{R_{c\_1}R_{c\_2} + R_{c\_1}R_L + R_{c\_2}R_L} \tag{1.9}$$

$$I_2 = \frac{\left(R_{c\_1} + R_L\right)V_2 - R_L V_1}{R_{c\_1}R_{c\_2} + R_{c\_1}R_L + R_{c\_2}R_L} \tag{1.10}$$

$$I_{c\_1,2} = \frac{V_1 - V_2}{R_{c\_1} + R_{c\_2}} = \frac{R_{c\_1}I_1 - R_{c\_2}I_2}{R_{c\_1} + R_{c\_2}} \tag{1.11}$$

According to (1.11), the circulating current phenomenon is induced by either an imbalance in the source voltages or a difference in cable resistance, which results in a voltage drop at the common bus.

Moreover, if the voltage sources for V_1 and V_2 are the same, the difference in value of cable resistance results in current-sharing error, which mean that the current generated by each source varies depending on the cable resistance that connects these sources to the common bus, as shown in Fig. 1.8.

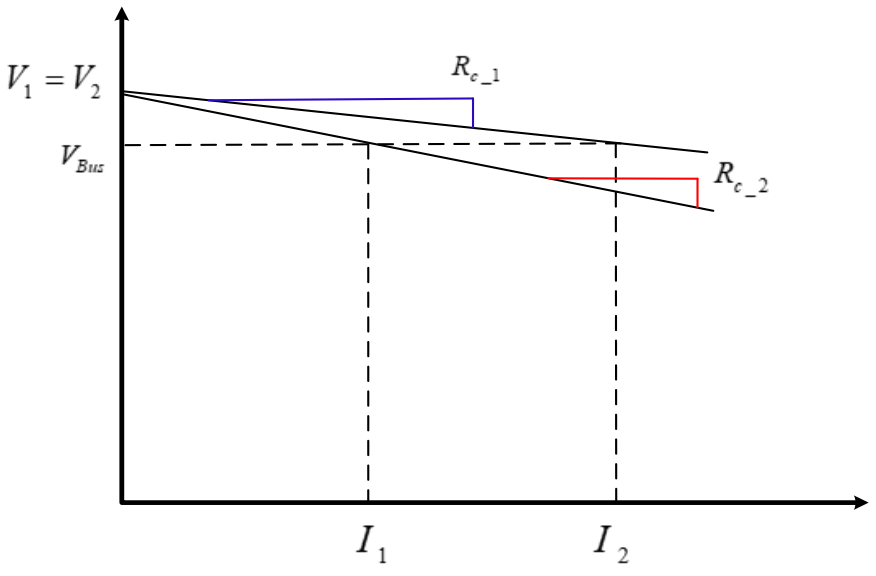


Fig. 1.8.V-I characteristics of two paralleled DC-DC converters

As shown in Fig. 1.8, the current generated from the source using a lower resistance wire is greater than the current generated from the source using a higher resistance wire.

Furthermore, the greater the resistance difference between the wires, the greater the stress carried by the source with the lower resistance wire. The DG and its power converter relate to the source in the systems of distributed power, such as a DC microgrid. As a result, if a current sharing error occurs in a DC Microgrid, the effect of the current sharing error is borne by a source converter. Furthermore, the current circulation problem will cause the converter to rapidly age due to the effect of heating, and one of the converters will be overworked because of the current sharing error. In the worst-case scenario, this overworked converter could reach its maximum current before supplying the load's required current, causing it to fail. The load will be forced onto the other converter, which will eventually fail as well. Therefore, current sharing must be improved to ensure the microgrid's proper functioning.

1.8.2. Examination of current-sharing methods

Many research studies have proposed various methods to avoid current circulation in order to solve the issue of current sharing in DC Microgrid systems. These techniques can be classified as either droop control methods or active load sharing methods. The current sharing is used in the hierarchical control's primary loop.

1.8.2.1. Method of active load sharing

To achieve current sharing in DC Microgrid, the technique of load sharing is employs a communication link between the power converters. The active load sharing technique is further subdivided into three controls: master-slave, centralized, and circular chain [85].

The centralized control technique is based on obtaining a current reference for each converter by dividing the load current i_{LOAD} by the number of converters module *N*.

The current reference for each k^{th} converter is expressed as

$$i_{k\_ref} = \frac{i_{load}}{N} \tag{1.12}$$

Fig 1.9 depicts a block diagram of the centralized control technique.

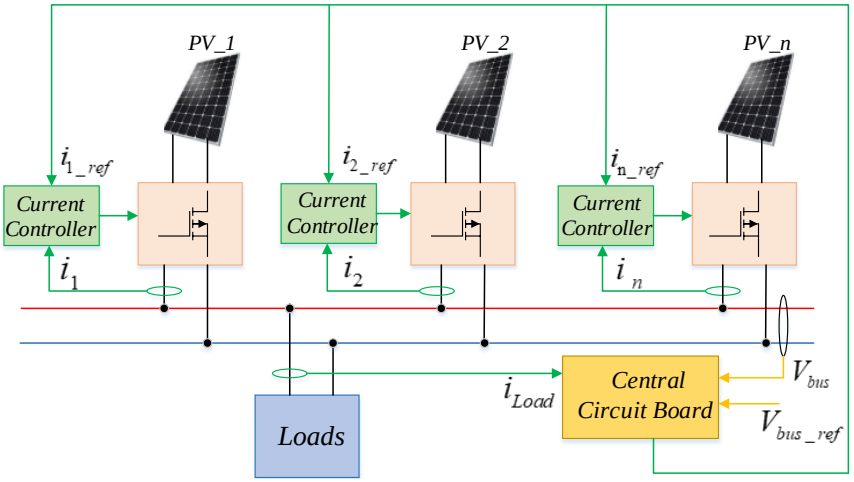


Fig. 1.9. The centralized control technique

As a result, in order to be carried out, the centralized control type necessitates knowledge of the total currents of the load, as well as, this control requires a central control platform [86]. The type of master-slave control depicted in Fig. 1.10 is based on defining the master, which is the converter module in this control. The designed master incorporates the voltage regulation loop, which generates a reference current as a result. This reference current is passed on to the other converters, each of which is referred to as a slave. In this type of master-slave control, the master converter serves as a voltage source, whereas the slave converters serve as current sources. In the event that the master converter fails, another converter will be designated as the master [87].

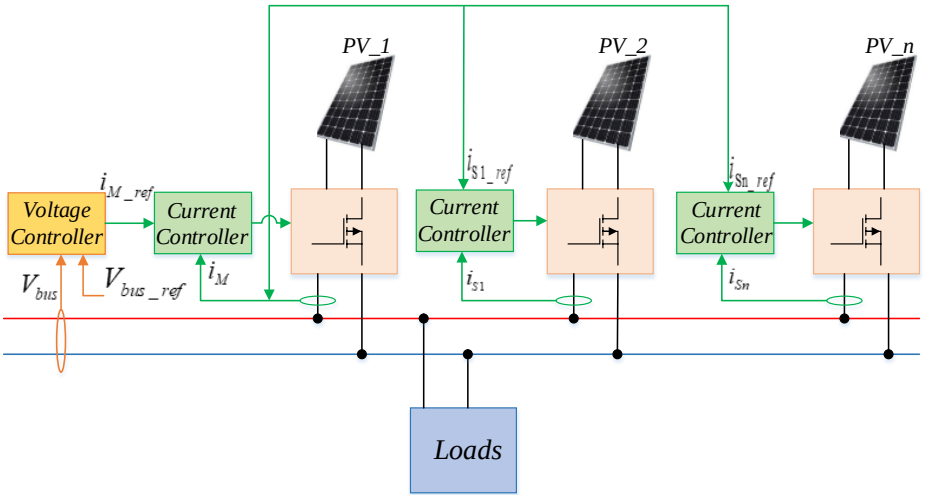


Fig. 1.10. Master-slave control technique

In the circular chain control type, the output current of the subsequent module converter is used as a reference current, resulting in a circle control. i, e. the first module's reference current is

equal to the last module's determined current [88]. Fig. 1.11 depicts the circular chain control block diagram.

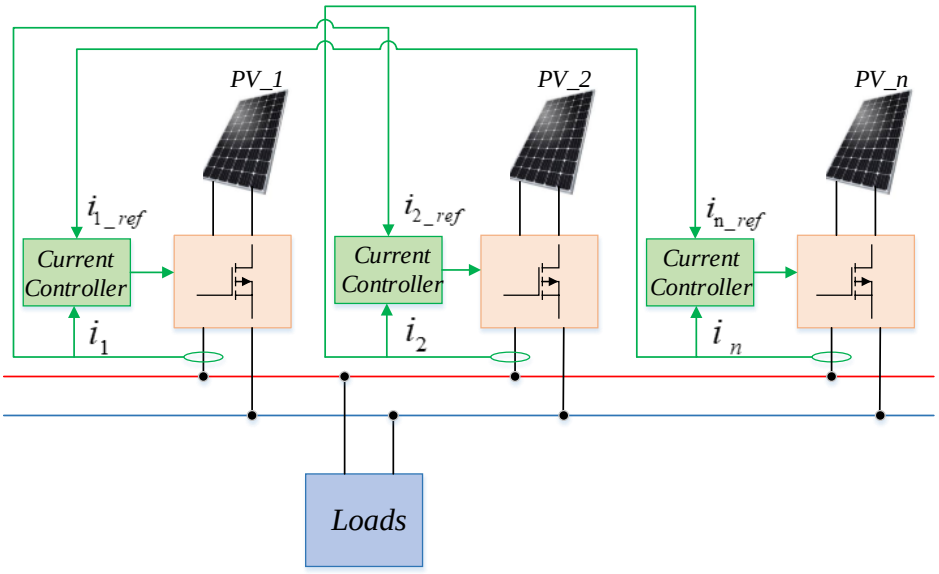


Fig. 1.11. Circular control method

Despite the benefits of circular control in terms of achieving current sharing across converters, the most significant disadvantage is the communication link between converters with a huge bandwidth. This communication link is required in order to move and distribute data among various converter modules. This type of control is not only physically constraining, but it also lacks flexibility.

1.8.2.2. Droop control method

A droop control approach involves creating a virtual series resistance using a control loop in order to create a current balance between several converters connected in parallel. The current balance between the converters can be adjusted using this control loop. This virtual series resistance, on the other hand, causes a voltage drop on the main DC bus. In order to limit DC bus voltage loss, a voltage restoration loop is inserted into the droop control loop [2-3], [17]. Fig. 1.12 depicts the control scheme.

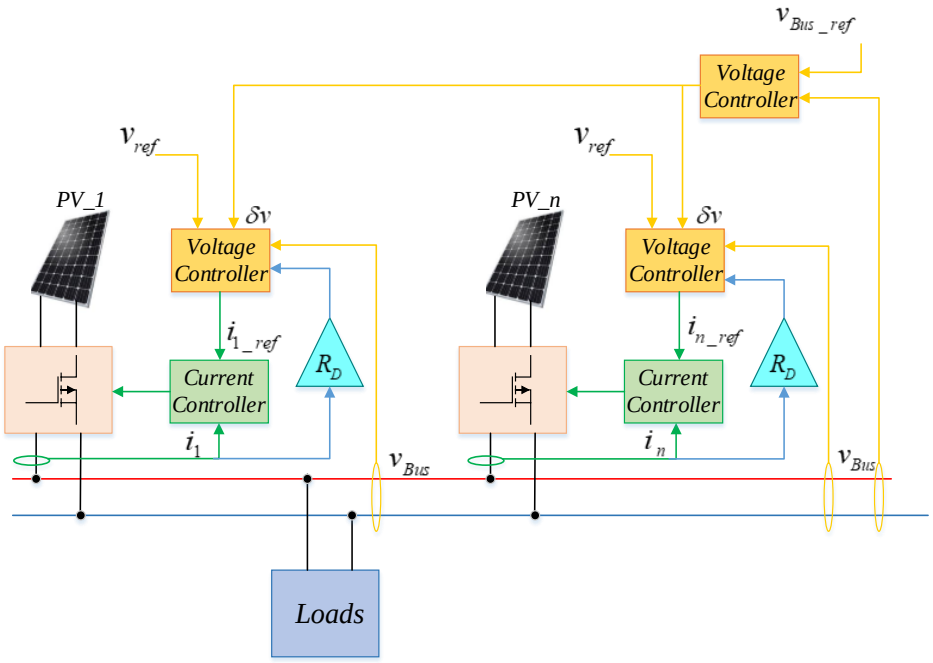


Fig .1.12. Droop control technique.

Droop control strategy does not necessitate a high-bandwidth communication link. Additionally, each source converter performs bus voltage management, allowing the distributed power system to be more flexible and extensible. Therefore, for this working thesis, droop control will be used as the current sharing mechanism with resistive and constant power loads in both connected and island modes of DC Microgrid [2-3], [17].

1.9. Conclusion

This chapter discusses the environment in which this working thesis was completed. The major goal is to design primary and secondary controls for a DC Microgrid that feeds constant power or resistive loads in both connected and island modes. A review of the literature on microgrids was conducted, as well as the benefits of deploying DC microgrids. Various challenges linked to the installation of DC microgrids, such as instability and current sharing problems, have also been examined. Droop control strategy will be selected at the conclusion of this literature evaluation to improve DC Microgrid current sharing. The system will be subjected to a stability study in order to assure the DC microgrid's continuous existence in the face of external disturbances.

Chapter 2: Primary Control Level of a DC Microgrid System

2.1. Introduction

The DC microgrid and its control are accomplished using PSIM software in this chapter, i.e. the primary control when referring to Fig. 1.4. In order to show the practicality of the proposed primary control, two DC-DC Buck converters connected in parallel, forming a DC-Microgrid, are simulated. The parallel connecting of the DC-DC Buck converters created the current circulation problem. Furthermore, external disturbances such as changes in the input voltages of the DC-DC Buck converters, sudden changes in the DC Microgrid's resistive load, and the challenge of removing one of the DC-DC Buck converters from the DC Microgrid's DC Bus might cause instability. In order to deal with these issues, a primary control level based on the PI controller is suggested, which can effectively avoid current circulation and external disturbances. The simulation study, which is divided into three scenarios to validate the proposed primary control, is carried out using Matlab and PSIM software.

Furthermore, this chapter describes in detail the processes of the single double lead controller (Type-II), the integral double lead controller (Type-III), the PI controller, and the cascade controller, all of which are needed to construct the proposed primary controller.

Because the transfer function of the DC-DC Buck converter, which forms the DC Microgrid, must be provided in this study, let us first look at the method of an average linear equivalent circuit that will be utilized to generate the transfer function.

2.2. Buck converter average linear equivalent circuit in continuous conduction mode

Fig. 2.1 depicts a Buck power converter component, which is the main ingredient of the DC-MG that connects the renewable energy resources (RESs) to the main DC bus. Because it contains at least one diode and one transistor that function as switches, a buck power converter is a highly nonlinear system. A buck power converter usually has a control process to accurately regulate the output voltage against load fluctuations and input voltage variations. Frequency response, transient response, and stability are common control facets for the DC-DC converters. In order to achieve a good study for a DC-DC Buck converter, on the one hand, the small-signal

dynamic performance of the DC-DC Buck converter and its influence on the DC-MG. On the other hand, the perturbation accrued on the DC-DC Buck converter, a linear control theory is well established [25-38]. However, in case of applying this theory, the DC-DC Buck converter must be averaged and linearized using the average linear equivalent circuit method.

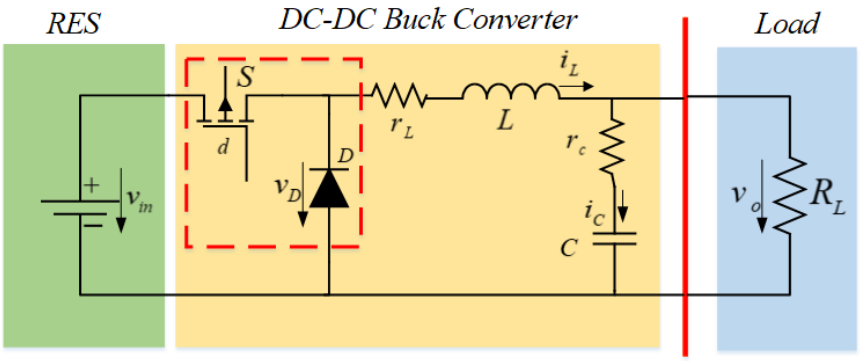


Fig. 2.1. The equivalent electrical circuit of a buck power converter

The small-signal modeling method is a well-known technique for physically representing PWM converters and their derivatives using controlled sources. The small-signal modeling method directly averages the PWM converter waveforms instead of the PWM converter state-space equations. The small-signal averaging method is comparable to state-space averaging because it involves averaging and small-signal linearization.

The following steps are involved in the small-signal averaging method [26]:

1. Averaging of switching component current and voltage waveforms over a single switching time
2. Switching components (Diode and transistors) must be replaced with nonlinear dc dependent current and voltage sources.
3. The parasitic components of semiconductor switches, such as transistor on-resistance, diode forward resistance, and diode-offset voltage, must be averaged over one switching time.
4. To obtain large-signal time-dependent waveforms, perturb the average current, voltage, and duty ratio waveforms.
5. Nonlinear large-signal dependent current and voltage sources are used to replace dc-dependent sources.

6. Separating the dc and ac components of the large-signal current, voltage, and duty cycle waveforms.
7. Nonlinear dependent current and voltage sources must be linearized.
8. Dc and small-signal variables must be separated.
9. A dc circuit model is used to represent the dc variables, while a small-signal linear ac circuit model is used to represent the ac variables.

Depending on the preceding steps, the small-signal averaging method employs current and voltage-dependent sources, as well as the law of energy conversion, to establish the transfer function of the DC-DC buck converter model for continuous condition mode (CCM). The DC-DC buck converter's appropriate switching network is typically modeled using voltage and current dependent sources and the law of conservation of energy. The current- and voltage-dependent sources are used to model the ideal switching network and the law of conservation of energy is used to model parasitic components of switching devices, such as the transistor on-resistance, the diode forward resistance, and the diode offset voltage. The average linear regression model of the DC-DC buck converter is then disconcerted to change the current, voltage, and duty cycle. As a result, the DC-dependent sources in the model are dominated by large time-varying dependent sources. DC and AC components can be found in large-signal current, voltage, and duty cycles. Large-signal sources can be replaced by DC-dependent sources and AC small-signal dependent sources. The model can be linearized by ignoring the AC component product if the measured values of the small-signal components are small enough, resulting in a linear circuit model with both AC and DC components.

The following assumptions must be made before developing the model for a DC-DC buck converter [26].

1. Switching losses are ignored because the transistor output capacitance and diode capacitance are ignored.
2. The on-resistance of a transistor is linear, while the off-resistance of a transistor is infinite.
3. A linear battery and a linear forward resistance model the diode in the on-state. The diode is represented by an infinite resistance in its off-state.
4. Passive components are time-invariant, linear, and frequency independent.

A DC-DC buck converter is made up of two main components: a nonlinear discrete part and a linear analog part. Nonlinear components include semiconductor switches such as transistors

and diodes. The linear part includes a capacitor, inductor, and the DC-DC Buck converter's resistive load.

In general, the output voltage v_o of a DC-DC Buck converter operated for a CCM is less than the input voltage v_{in} and can be expressed as:

$$v_o = d.\ v_{in} \tag{2.1}$$

Where d ranges between 0 and 1.

The output current i_o of a DC-DC buck converter in a CCM with no power losses can be written as follows:

$$i_o = \frac{1}{d}.i_{in} \tag{2.2}$$

Due to the obvious PWM signal, the output voltage and current generate ripples $(\Delta i, \Delta v)$, which are commonly referred to as the DC-DC Buck converter specification, and can be approximated as:

$$\Delta i = \frac{V_o}{f_s.L}(1-D) \tag{2.3}$$

$$\Delta v = \frac{L}{2Cf_s} \tag{2.4}$$

The switching frequency is represented by f_s. The nominal output voltage is V_o. *D* denotes the nominal duty cycle.

The main goal of these ripples is to achieve the nominal values of the capacitors *C* and inductors *L* in the DC-DC Buck converter when it is used for a CCM.

The modeling strategy of the DC-DC Buck converter is based on two main roles: replacing the switching network (or components) with an analog (continuous) circuit model based on steady-state waveforms, as shown in Fig. 2.2, and leaving the analog part composed of linear components unchanged. For the Buck converter, Let us neglect the parasitic components as shown in Fig. 2.1 [26].

where: $V_{SD} = V_I, V_{SL} = V_I - V_o, and V_{LD} = V_o$

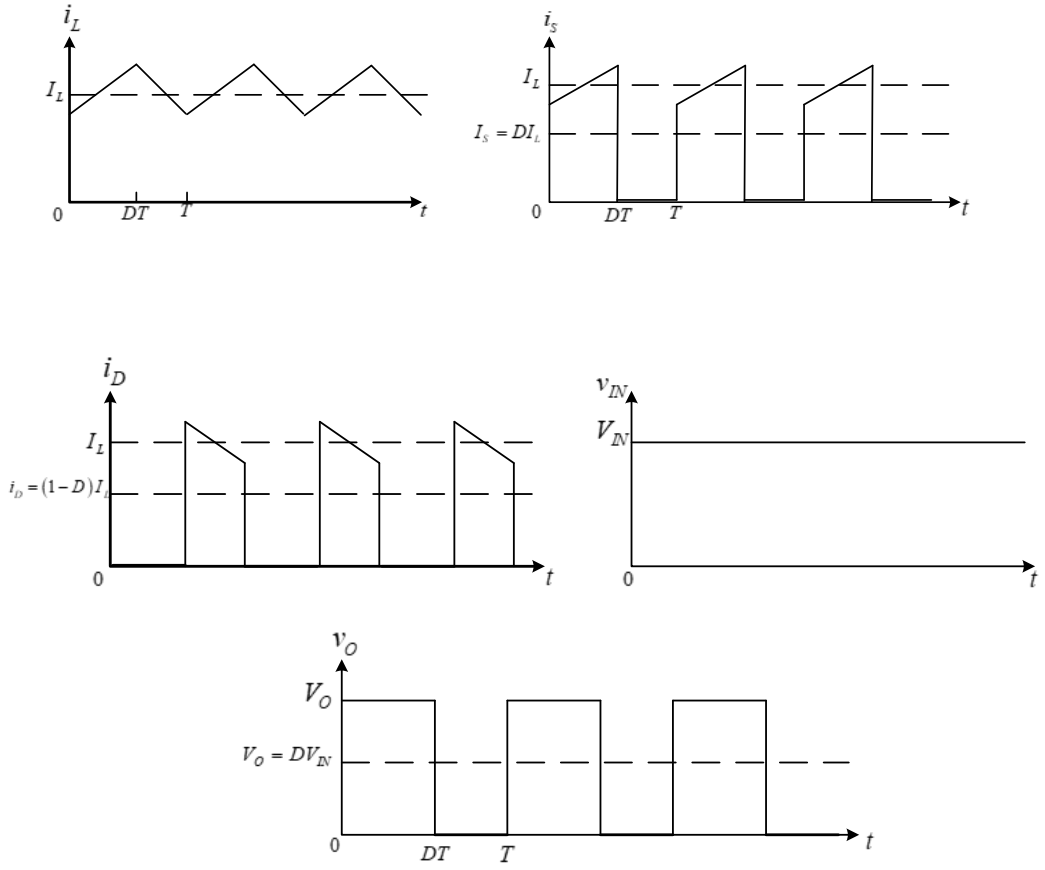


Fig. 2.2. The switching network of a DC-DC Buck converter's steady-state waveforms for CCM

The steady-state waveform of i_s, as shown in Fig. 2.2, can be assumed as follows:

$$i_s \approx \begin{cases} I_L & For \quad 0 < t \le DT \\ 0 & For \quad DT < t \le T \end{cases} \tag{2.5}$$

As a result, the dc component of the switch current describing an ideal dc current-controlled current source is

$$I_S = \frac{1}{T}\int_0^T i_S dt = \frac{1}{T}\int_0^{DT} I_L dt = DI_L \tag{2.6}$$

where I_L denotes the nominal DC value of i_L

Based on the Fig. 2.2, the steady state waveform of the voltage across the ideal diode can be written as

$$v_{LD} \approx \begin{cases} V_{SD} & For \quad 0 < t \le DT \\ 0 & For \quad DT < t \le T \end{cases} \tag{2.7}$$

Resulting in its dc component

$$V_{LD} = \frac{1}{T}\int_0^T v_{LD}dt = \frac{1}{T}\int_0^{DT} V_{SD}dt = DV_{SD} \tag{2.8}$$

Referring to Fig. 2.2, the steady-state waveform of the diode current can be approximated by

$$i_D \approx \begin{cases} 0, & For \quad 0 < t \le DT \\ I_L, & For \quad DT < t \le T \end{cases} \tag{2.9}$$

Resulting in its dc component

$$I_D = \frac{1}{T}\int_0^T i_D dt = \frac{1}{T}\int_{DT}^T I_L dt = I_L(1-D) \tag{2.10}$$

Using (2.6) and (2.10), the inductor current equation can be expressed as

$$I_L = \frac{I_S}{D} = \frac{I_D}{1-D} \tag{2.11}$$

The rms value of the switch current is calculated using (2.5) and (2.6) as follows

$$I_{S\_rms} = \sqrt{\frac{1}{T}\int_0^T i_S^2 dt} = \sqrt{\frac{1}{T}\int_0^{DT} I_L^2 dt} = I_L\sqrt{D} = \frac{I_S}{\sqrt{D}} = \frac{I_D\sqrt{D}}{1-D} \tag{2.12}$$

The power loss in the transistor on-resistance rT (MOSFET) can be written as

$$P_{rT} = rT.\mathrm{I}_{S\_rms}^2 = \frac{rT}{D}I^2{}_S \tag{2.13}$$

Using (2.9), the rms value of the diode current is calculated as follows

$$I_{D\_rms} = \sqrt{\frac{1}{T}\int_0^T i_D^2 dt} = \sqrt{\frac{1}{T}\int_{DT}^T I_L^2 dt} = I_L\sqrt{1-D} = \frac{I_S\sqrt{1-D}}{D} = \frac{I_D}{\sqrt{1-D}} \tag{2.14}$$

Yielding of its power loss in the diode forward resistance R_F as

$$P_{R_F} = R_F I_{D\_rms}^2 = \frac{R_F}{1-D} I_D^2 \tag{2.15}$$

In addition, a power loss can be dissipated by the diode offset voltage source V_{R_F} and can be expressed as

$$P_{V_{R_F}} = V_{R_F} I_D \tag{2.16}$$

Hence, the nonlinear part of a buck converter can be modeled for a CCM using voltage and current sources based on equations (2.6) and (2.8). When the switch voltage v_s is ignored, the power loss values can be modeled by $\frac{rT}{D}, \frac{R_F}{1-D}$ as depicted in Fig 2.3 [26].

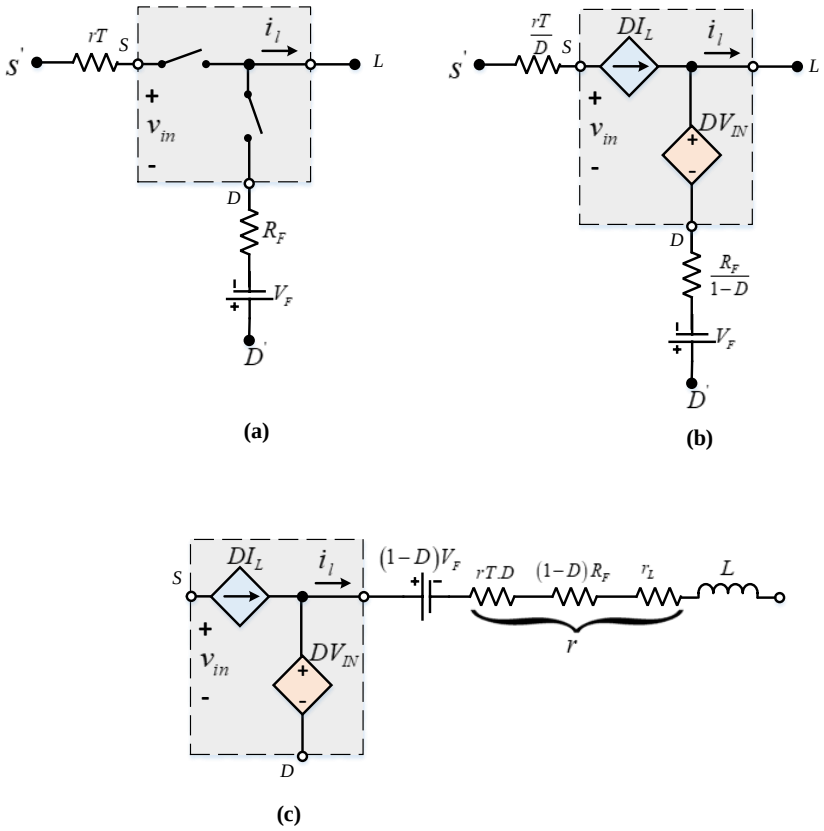


Fig. 2.3 The actual switching network's averaged dc model of the DC-DC Buck converter for CCM

When a DC-DC Buck converter is operated for a CCM and low frequency $f < f_s/2$, and when DC independent external variables, such as the input voltage and duty cycle, are perturbed, then all other variables will oscillate across their relating DC levels at a low frequency f [26]. Hence, the small signal of voltage, current, and duty cycle can be written as a sum of dc and ac low frequency components as

$$v_O = V_O + v_o \tag{2.17}$$

$$i_L = I_L + i_l \tag{2.18}$$

$$d_T = d + D \tag{2.19}$$

$$v_{IN} = V_{IN} + v_{in} \tag{2.20}$$

$$i_D = I_D + i_d \tag{2.21}$$

$$i_{IN} = I_{IN} + i_{in} \tag{2.22}$$

The average model of the DC-DC Buck converter is linearized at a specified operating point by first neglecting the large-signal nonlinear equations into a Taylor series about the set - point and then neglecting the higher-order terms. We can achieve the linear part of a small-signal model of the DC-DC Buck converter, which considers only the first-order terms, by implying small-signal perturbations. Based on the small-signal perturbation, the ac low-frequency components have much lower values than the corresponding dc components [26].

When (2.22), (2.18), and (2.19) are substituted into (2.2), a nonlinear equation is obtained as follows:

$$I_{IN} + i_{in} = (d + D)(I_L + i_l) = DI_L + Di_l + I_L d + i_l d \tag{2.23}$$

Neglecting the products of the small-signal components $i_l d \approx 0$ by assuming $i_l d \ll Di_l$, $i_l d \ll I_l d$ and by achieving the conditions $d \ll D$ and $i_l \ll I_L$

Substituting (2.20), (2.19), and (2.18) in (2.1), a nonlinear equation is obtained as follows:

$$V_O + v_o = (d + D)(V_{IN} + v_{in}) = DV_{IN} + Dv_{in} + V_{IN}d + v_{in}d \tag{2.24}$$

Similarly, with the same conditions, ignoring the products of the small-signal components $v_{in}d$ by assuming $v_{in}d \ll Dv_{in}$, $v_{in}d \ll V_{IN}d$

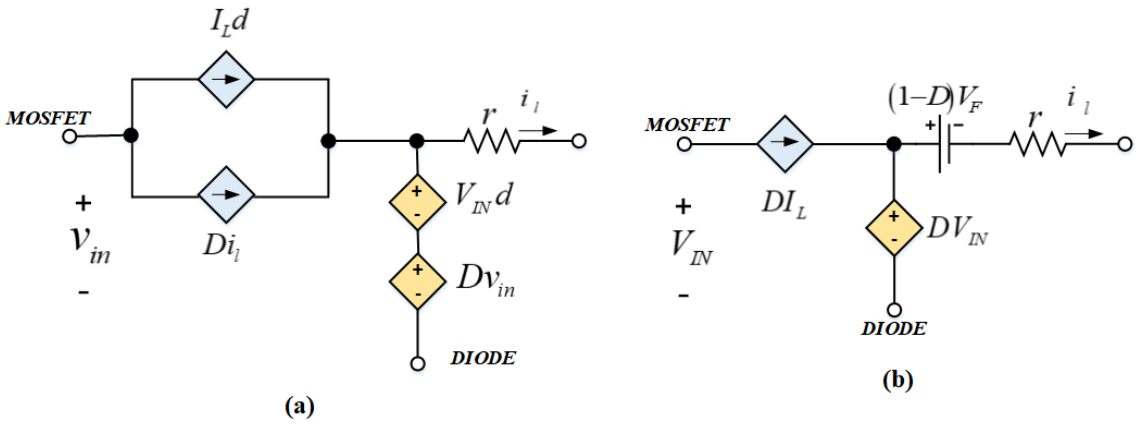


Fig. 2.4 Actual switching network small-signal low frequency and dc linear circuit models for DC-DC Buck converter

The average linear equivalent circuit, shown in Fig. 2.4(b), can be designed by replacing the model of the switching network of the DC-DC Buck converter, as shown in Fig. 2.3(b). As shown in Fig. 2.5(c), the dependent current sources can be divided into two groups: one established in parallel with the input voltage source while the other established in parallel with the dependent voltage source's series connection. The average linear equivalent circuit of the DC-DC buck converter can be simplified by ignoring the parallel dependent current sources, as can be seen in Fig. 2.5 (d) [26].

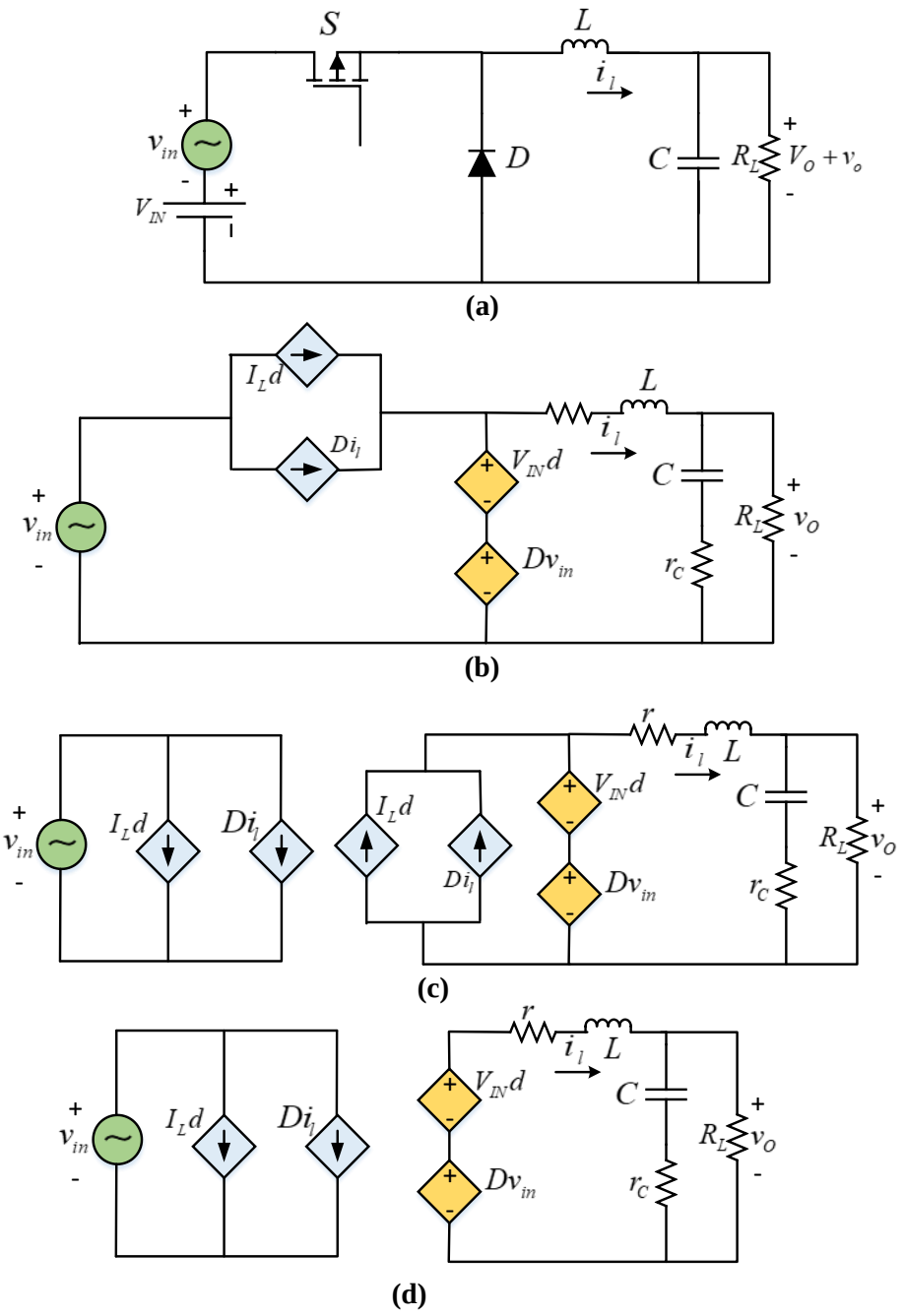


Fig. 2.5 Small-signal circuit block diagram of a DC-DC Buck converter for CCM

2.3. Open-Loop Transfer Functions for a DC-DC Buck converter

Transfer functions can be defined based on the average linear equivalent circuit of a DC-DC buck converter for CCM, as shown in Fig. 2.5(d), in order to design the main controller. As a result, the DC-DC Buck converter is classified as a multi-input single-output (MISO) system. Small-signal input voltage v_{in} and small-signal output current i_0 are considered disturbances for

a DC-DC Buck converter, whereas small-signal duty cycle d is considered a control variable. The transfer functions, which can be defined as the control-to-output transfer function T_p and the input-to-output transfer function M_v, can be obtained from a DC-DC Buck converter operated for CCM. Furthermore, input and output impedances can be characterized as impedance transfer functions (Z_{in}, Z_{out}). Fig. 2.6 shows a block diagram of the open-loop average linear equivalent circuit of a DC-DC buck converter in CCM, which can be seen in Fig. 2.5(a). Based on Fig. 2.6, the output voltage of a Buck converter operating in CCM can be calculated using the superposition law. The total output response produced from each excitation operating alone can be used to calculate the responses from multiple excitations [26]. Therefore, the output voltage of the open-loop DC-DC Buck converter in CCM can be written as

$$v_o = v_o^{'} + v_o^{''} + v_o^{'''} = T_p d + M_v v_i - Z_{out} i_o \tag{2.25}$$

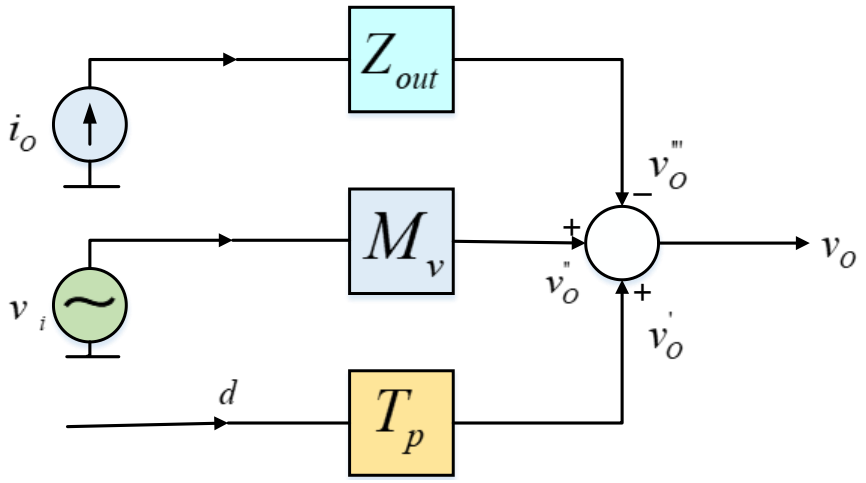


Fig. 2.6. Block diagram of the open-loop average linear equivalent circuit of a DC-DC buck converter in CCM

2.3.1 Open-Loop Control-to-Output Transfer Function

Using the DC-DC Buck converter average linear equivalent circuit shown in Fig. 2.5(d), the Open-Loop Control-to-Output Transfer function can be obtained by lowering the input voltage and the output current turns to zero, as illustrated in Fig. 2.7, which is a single-input single-output (SISO) system. Furthermore, the Open-Loop Control-to-Output Transfer function is commonly referred to as a duty ratio-to-output voltage transfer function [26]. Thus, the output voltage can be calculated as:

$$v_o(s) = V_I d(s) \frac{Z_2(s)}{Z_1(s) + Z_2(s)} \tag{2.26}$$

where

$$Z_1(s) = r + sL \tag{2.27}$$

$$Z_2(s) = \frac{R_L\left(r_C + \frac{1}{sC}\right)}{R_L + r_C + \frac{1}{sC}} \tag{2.28}$$

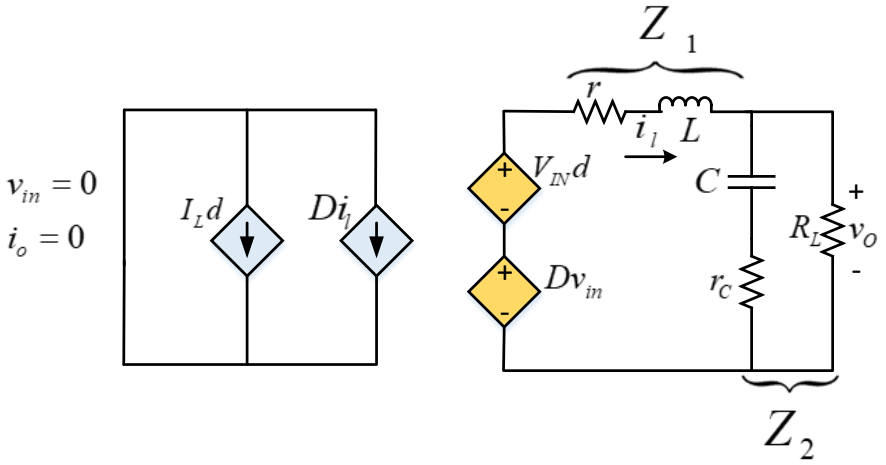


Fig. 2.7. The DC-DC Buck converter's average linear equivalent circuit for calculating the open-loop control-to-output transfer function

By substituting (2.27) and (2.28) in (2.26), the control-to-output transfer function of the DC-DC buck converter operating in CCM is calculated as follows:

$$T_p(s) = \left.\frac{v_o(s)}{d(s)}\right|_{v_i = i_o = 0} = \frac{V_I R_L r_C}{L\left(R_L + r_C\right)} \frac{s + \frac{1}{Cr_C}}{s^2 + s\frac{C\left(R_L r_C + R_L r + r_C r\right) + L}{LC\left(R_L + r_C\right)} + \frac{R_L + r}{LC\left(R_L + r_C\right)}} = T_{po} \frac{1 + \frac{s}{w_z}}{1 + \frac{2\xi s}{w_0} + \frac{s^2}{w_0^2}} \tag{2.29}$$

The low frequency value of T_p is given as

$$T_{po} = T_p(0) = \frac{V_I R_L r_C w_z}{L(R_L + r_C) w_0^2} = \frac{V_I R_L}{R_L + r} \approx V_I \tag{2.30}$$

The angular natural frequency can be calculated as follows:

$$w_0 = \sqrt{\frac{R_L + r}{LC(R_L + r_C)}} \tag{2.31}$$

The damping factor can be written as

$$\xi = \frac{L + C\left[R_L(r_C + r) + r_C r\right]}{2\sqrt{LC\left(R_L + r_C\right)\left(R_L + r_C\right)}} \tag{2.32}$$

The zero's angular frequency is

$$w_z = \frac{1}{Cr_C} \tag{2.33}$$

2.3.2 Open-Loop Input-to-Output Transfer Function

Open-Loop Input-to-Output Transfer Function $M_v(s)$ can be designed using the average linear equivalent circuit depicted in Fig. 2.5(d) of the DC-DC Buck converter depicted in Fig. 2.5(a) by establishing $d = 0$ and $i_o = 0$, which yields a novel model of a DC-DC Buck converter's average linear equivalent circuit, as shown in Fig. 2.8. The obtained transfer function is a single-input single-output (SISO) system. The Open-Loop Input-to-Output Transfer Function is a second-order transfer function having two poles and one zero in LHP. Moreover, the open-loop input-to-output transfer function is also known as the line-to-output voltage transfer function [26]. As a result, the output voltage calculated from Fig. 2.8 is

$$v_o(s) = Dv_i(s)\frac{Z_2(s)}{Z_1(s) + Z_2(s)} \tag{2.34}$$

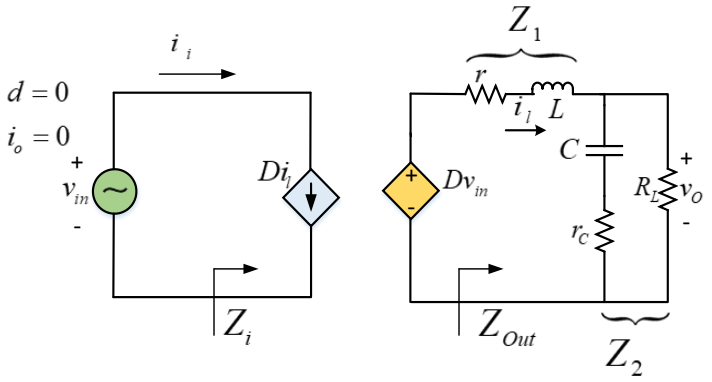


Fig. 2.8. The DC-DC Buck converter's average linear equivalent circuit for calculating the open-loop input-to-output transfer function

Thus, based on (2.29), one gets an open-loop input-to-output transfer function as

$$M_v(s)=\left.\frac{v_o(s)}{v_i(s)}\right|_{d=i_o=0}=\frac{D}{V_I}T_p(s)=\frac{DR_Lr_C}{L\left(R_L+r_C\right)}\frac{s+\frac{1}{Cr_C}}{s^2+s\frac{C\left(R_Lr_C+R_Lr+r_Cr\right)+L}{LC\left(R_L+r_C\right)}+\frac{R_L+r}{LC\left(R_L+r_C\right)}}=M_{vo}\frac{1+\frac{s}{w_z}}{1+\frac{2\xi s}{w_0}+\frac{s^2}{w_0^2}} \quad (2.35)$$

The low frequency value of M_v is provided as follows:

$$M_{vo}=M_v(0)=\frac{DR_L}{R_L+r}\approx D \quad (2.36)$$

2.3.3 Open-Loop Input Impedance Transfer Function

The open-loop input impedance of the DC-DC Buck converter operating in CCM may be calculated using the average linear equivalent circuit shown in Fig. 2.8 [26]. Thus, the current generated by the inductance device may be stated as:

$$i_l=\frac{Dv_i}{Z_1+Z_2} \quad (2.37)$$

As a result of which the input current can be calculated as

$$i_i=Di_l=\frac{D^2v_i}{Z_{out}}=\frac{D^2v_i}{Z_1+Z_2} \quad (2.38)$$

Notice that $Z=Z_1+Z_2$

Therefore, using (2.27) and (2.28), The DC-DC buck converter's open-loop input impedance is obtained as

$$Z_i(s)=\left.\frac{v_i(s)}{i_i(s)}\right|_{d=i_o=0}=\frac{Z}{D^2}=\frac{L}{D^2}\frac{s^2+s\frac{C\left(R_Lr_C+R_Lr+r_Cr\right)+L}{LC\left(R_L+r_C\right)}+\frac{R_L+r}{LC\left(R_L+r_C\right)}}{s+\frac{1}{C(R_L+r_C)}}=Z_{io}\frac{1+\frac{2\xi s}{w_0}+\frac{s^2}{w_0^2}}{1+\frac{s}{w_{cr}}} \quad (2.39)$$

The low frequency value of Z_i is computed as follows

$$Z_{io}=Z_i(0)=\frac{Lw_0^2}{D^2w_{cr}}=\frac{Z(0)}{D^2}=\frac{R_L+r}{D^2} \quad (2.40)$$

The pole's angular frequency is

$$w_{cr} = \frac{1}{C\left(R_L + r_C\right)} \tag{2.41}$$

2.3.4 Open-Loop Output Impedance Transfer Function

Whit $v_i = 0$, $d = 0$, and $i_o = 0$ in the full average linear equivalent circuit of Fig. 2.5(d), one gets the DC-DC buck converter's new derivation average linear equivalent circuit, as shown in Fig. 2.9. A source voltage technique v_t is appropriate across the resistive load to calculate the output impedance transfer function, and then the current i_t provided through the source voltage experiment is calculated. The transfer function of the output impedance is equal to the voltage v_t to current i_t ratio value [26]. As a result, (2.27) and (2.28), may be used to calculate the open-loop output impedance transfer function of the DC-DC Buck converter feeding a resistive load as follows

$$Z_{out} = \left.\frac{v_t(s)}{i_t(s)}\right|_{v_i = d = i_0 = 0} = Z_1 \| Z_2 = \frac{R_L r_C}{R_L + r_C} \frac{\left(s + \frac{1}{Cr_C}\right)\left(s + \frac{r}{L}\right)}{s^2 + s\frac{C\left(R_L r_C + R_L r + r_C r\right) + L}{LC\left(R_L + r_C\right)} + \frac{R_L + r}{LC\left(R_L + r_C\right)}} = Z_{ox} \frac{\left(1 + \frac{s}{w_z}\right)\left(1 + \frac{s}{w_{rl}}\right)}{1 + \frac{2\xi s}{w_0} + \frac{s^2}{w_0^2}} \tag{2.42}$$

where

$$Z_{ox} = \frac{R_L r_C}{R_L + r_C} \tag{2.43}$$

and

$$w_{rl} = \frac{r}{L} \tag{2.44}$$

2.4 Conventional DC-DC power converter controls

Several well-known control approaches are commonly employed in DC-DC power converters to regulate voltage and current, and some have been utilized by industry, airplanes, electric cars, ships, satellites, communications networks, and home loads of AC and DC origin. A DC-DC power converters voltage regulator's purpose is to keep a constant or stable output voltage regardless of variations in load or input voltage. For DC-DC PWM converters, the PI, PID, Integral-Single-Lead Controller (type II), and Integral-double-Lead Controller (type II) are often utilized.

2.4.1 Proportional-Integral Controller

A proportional-integral (PI) controller design and its average linear equivalent circuit are shown in Fig. 2.9 [26]. The transfer function of the amplifier's average linear equivalent circuit, depicted in Fig. 2.9, may be expressed as

$$A_v(s) = \frac{v_c(s)}{v_f(s)} = -\left[\frac{R_2}{R_1 + h_{11}} + \frac{1}{s(R_1 + h_{11})C_1}\right] = -\left(K_P + \frac{K_I}{s}\right) \tag{2.45}$$

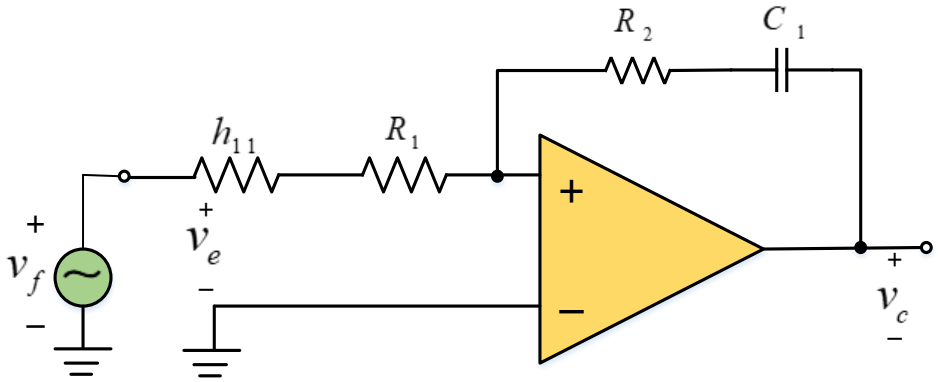


Fig. 2.9. Proportional-integral (PI) controller's average linear equivalent circuit.

where

$$K_P = \frac{R_2}{R_1 + h_{11}} \tag{2.46}$$

and

$$K_I = \frac{1}{(R_1 + h_{11})C_1} \tag{2.47}$$

The PI controller's average linear equivalent circuit can be written as

$$T_c(s) = \frac{v_c(s)}{v_e(s)} = -A_v(s) = \frac{K_P\left(s + \frac{K_I}{K_P}\right)}{s} = \frac{K_P(s + w_z)}{s} \tag{2.48}$$

where

$$w_z = 2\pi f_z = \frac{K_I}{K_P} = \frac{1}{R_2 C_1} \tag{2.49}$$

The PI controller lowers switching fluctuations by acting as a low-pass filter. Nevertheless, it decreases bandwidth, increases rising time, and decreases setup time.

The PI controller's construction method is summed as. The amount of the loop gain at the gain-crossover frequency f_c is calculated as follows

$$\left|T(f_c)\right| = \left|T_k(f_c)\right|\left|T_c(f_c)\right| = \left|T_k(f_c)\right| K_P = 1 \tag{2.50}$$

T_k denotes the uncompensated loop gain.

Resulting in the gain of the controller's K_P section is

$$K_P = \frac{1}{\left|T_k(f_c)\right|} = 20\log\left|T_k(f_c)\right|(dB) = 10^{-\frac{\left|T_k(f_c)\right|}{20}} \tag{2.51}$$

Note that the PI controller's phase lag has no influence on the phase of the compensated loop gain towards the gain-crossover frequency f_c, if and only if $f_z \le f_c/10$. Thus, the zero's angular frequency is

$$w_z = \frac{w_c}{10} = \frac{K_I}{10K_P} \tag{2.52}$$

As a result, the coefficient of the controller's integral part is calculated as

$$K_I = \frac{w_c}{10} K_P = \frac{2\pi f_c}{10} K_P \tag{2.53}$$

2.4.2 Integral-Single-Lead Controller

One sort of lead-type controller is an integral-single lead (or type II) controller, which has a pole at the origin and a single pole–zero pair. As a result, this controller gives a maximum phase boost of 90° with 0% steady-state error and fast transient response. The integral-single-lead controller's main goal is to reduce phase lag and hence obtain a high crossover frequency f_c while keeping a set phase margin *PM*. In this controller, the frequency at which the magnitude of the loop gain $|T|$ crosses 1 or 0 dB is referred to as the crossover frequency f_c. The crossover frequency f_c is typically set at $f_s/5$ [26]. Fig. 2.10 depicts the typical linear equivalent circuit of an integral-single-lead controller. Suppose the operational amplifier, shown in Fig. 2.10 is perfect, with unlimited open-loop dc gain and bandwidth. As a result, the operational amplifier's transfer function may be written as

$$A_{vs}(s)=\frac{v_c(s)}{v_e(s)}=-\frac{1}{C_2\left(R_1+h_{11}\right)}\frac{s+\dfrac{1}{R_2C_1}}{s\left(s+\dfrac{C_1+C_2}{R_2C_1C_2}\right)} \tag{2.54}$$

Based on Fig 2.10, the integral-lead controller's voltage transfer function can be expressed as

$$T_c(s)=\frac{v_c(s)}{v_e(s)}=-A_v(s)=\frac{Bw_{zc}\left(s+w_{zc}\right)}{s\left(s+w_{pc}\right)}=\frac{B\left(1+\dfrac{s}{w_{zc}}\right)}{K^2s\left(1+\dfrac{s}{w_{pc}}\right)} \tag{2.55}$$

where

$$w_{pc}=K^2w_{zc} \tag{2.56}$$

and

$$K=\sqrt{\frac{w_{pc}}{w_{zc}}} \tag{2.57}$$

The magnitude of the integral-lead controller's voltage transfer function is

$$\left|T_c(jw)\right|=\left|\frac{B\left(1+\dfrac{jw}{w_{zc}}\right)}{K^2jw\left(1+\dfrac{jw}{w_{pc}}\right)}\right|=\frac{B}{wK^2}\sqrt{\frac{1+\left(\dfrac{w}{w_{zc}}\right)^2}{1+\left(\dfrac{w}{w_{pc}}\right)^2}} \tag{2.58}$$

The argument is formatted as follows:

$$\phi_{Tc}=-\frac{\pi}{2}+\tan^{-1}\left(\frac{\dfrac{w}{w_{zc}}-\dfrac{w}{w_{pc}}}{1+\dfrac{w^2}{w_{zc}w_{pc}}}\right) \tag{2.59}$$

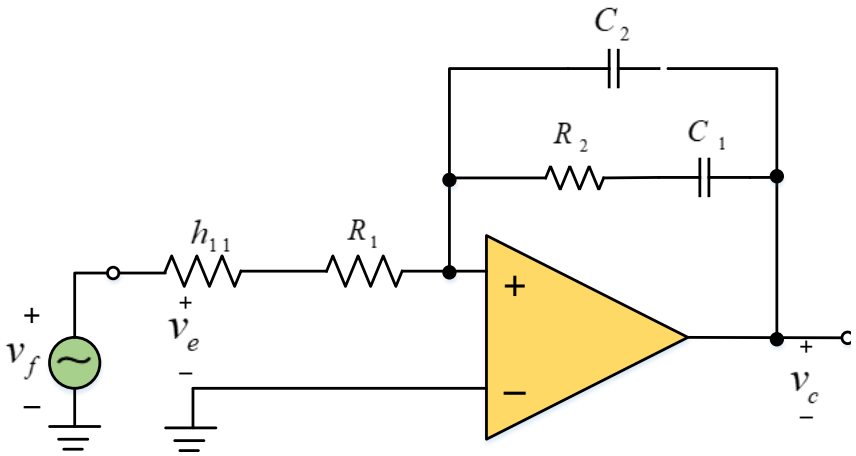


Fig. 2.10. Integral-single-lead controller's average linear equivalent circuit

By setting the derivative of the term in the parentheses of (2.59) to zero and applying (2.57), the frequency at which the largest phase boost ϕ_{Tc} will occur may be calculated as

$$w_m = \sqrt{w_{zc} w_{pc}} = \frac{w_{pc}}{K} = K w_{zc} \tag{2.60}$$

By substituting (2.60) into (2.59), the maximum value of the phase $\phi_{Tc(Max)} = \phi_{Tc}(f_m)$ can be calculated as

$$\phi_{Tc}(f_m) = -\frac{\pi}{2} + \tan^{-1}\left(\frac{K^2 - 1}{2K}\right) = -\frac{\pi}{2} + \sin^{-1}\left(\frac{K^2 - 1}{K^2 + 1}\right) \tag{2.61}$$

As a result, the phase boost's maximum value is

$$\phi_m = \phi_{Tc}(f_m) + \frac{\pi}{2} = \sin^{-1}\left(\frac{K^2 - 1}{K^2 + 1}\right) \tag{2.62}$$

as well as

$$K = \frac{B}{|T_c(f_m) w_m|} = \tan\left(\frac{\phi_m}{2} + 45^o\right) \tag{2.63}$$

To evaluate the overall stability of closed-loop linear systems, the Integral-Single-Lead controller's building technique relies on the gain margin GM and the phase margin PM.

In order to verify the stability of the loop-gain system, the phase margin PM is described as the quantity of loop-gain phase lag at the crossover frequency f_c as follows.

$$PM \equiv 180 + \phi_T(f_c) \tag{2.64}$$

When the loop-gain phase angle hits 180^o, the gain margin GM is calculated as the inverse of the loop-gain magnitude at frequency f_{-180}.

$$GM = \frac{1}{|T(f_{-180})|} = -20\log|T(f_{-180})| \tag{2.65}$$

The gain crossover frequency f_c of an integral-Single Lead controller is normally set to be equal to the frequency f_m. Consequently, we can compute the amount of the loop gain at the crossover frequency as

$$|T(f_c)| = |T_c(f_c)||T_k(f_c)| = |T_c(f_c)||T_{mp}(f_c)|\beta = 1 \tag{2.66}$$

The phase of the loop gain at the crossover frequency fc is obtained by using (2.61) as follows

$$\phi_T(f_c) = \phi_{T_k}(f_c) + \phi_{Tc}(f_c) = \phi_{T_k}(f_c) - 90 + \phi_m \tag{2.67}$$

As a result, the phase margin may be represented as

$$PM = 180^o + \phi_T(f_c) = \phi_{T_k}(f_c) + 90 + \phi_m \tag{2.68}$$

This results in the necessary phase boost as

$$\phi_m = PM - \phi_{T_k}(f_c) - 90^o \tag{2.69}$$

2.4.3 Integral-Double-Lead Controller

The corresponding circuit of the Integral-double-lead controller (also called the type_III controller) amplifier is shown in Fig. 2.11. The Integral-double-lead controller features a pole at the origin as well as two zero-pole pairs. Because the two zeros and two poles are coincident, the phase shift is decreased. This controller's integral part is utilized to create a high low-frequency gain, as a result, at low frequencies, both the dc error and the closed-loop output impedance are minimized. The integral-double-Lead controller's purpose is to keep a defined phase margin *PM* whilst achieving a high crossover frequency f_c of the control-to-output gain [26].

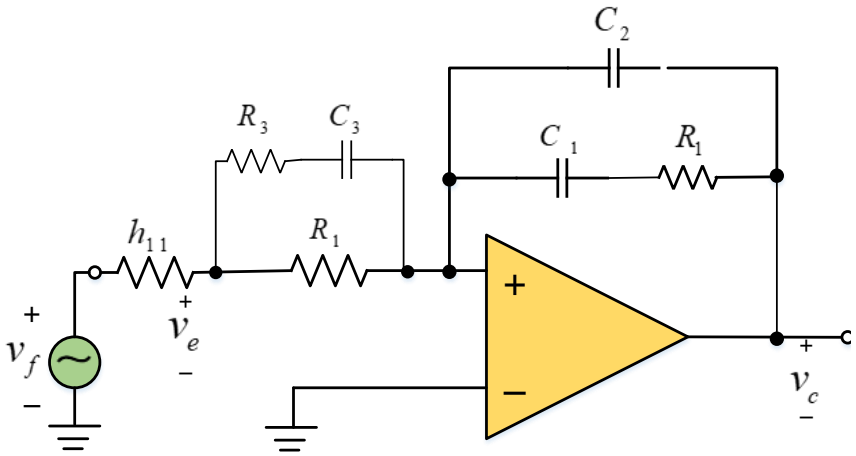


Fig. 2.11. Integral-double-lead controller's equivalent circuit

Suppose that the operational amplifier's open-loop dc gain and bandwidth are both limitless. Thus, the voltage transfer function of the amplifier seen in Fig. 2.11 may be expressed as

$$A_{vD}(s)=\frac{v_c(s)}{v_f(s)}=-\frac{R_1R_3}{C_2\left[R_1R_3+h_{11}\left(R_1+R_3\right)\right]}\frac{\left(s+\dfrac{1}{R_2C_1}\right)\left[s+\dfrac{1}{C_3\left(R_1+R_3\right)}\right]}{s\left(s+\dfrac{C_1+C_2}{R_2C_1C_3}\right)\left(s+\dfrac{R_1+h_{11}}{C_3\left[R_1R_3+h_{11}\left(R_1+R_3\right)\right]}\right)} \tag{2.70}$$

The voltage transfer function (2.70) of the Integral-double-lead controller may be expressed simply as follows.

$$T_c(s)=\frac{v_c(s)}{v_e(s)}=-\frac{v_c(s)}{v_f(s)}=-A_{vD}(s)=\frac{B\left(s+w_{zc1}\right)(s+w_{zc2})}{s(s+w_{pc1})(s+w_{pc2})} \tag{2.71}$$

Suppose $w_{zc1}=w_{zc2}=w_{zc}$ and $w_{pc1}=w_{pc2}=w_{pc}$, (2.71) becomes as

$$T_c(s)=\frac{v_c(s)}{v_e(s)}=\frac{B\left(s+w_{zc}\right)^2}{s(s+w_{pc})^2}=\frac{Bw_{zc}{}^2\left(1+\dfrac{s}{w_{zc}}\right)^2}{w_{pc}{}^2s\left(1+\dfrac{s}{w_{pc}}\right)^2}=\frac{B\left(1+\dfrac{s}{w_{zc}}\right)^2}{K^2s\left(1+\dfrac{s}{w_{pc}}\right)^2} \tag{2.72}$$

where

$$K=\frac{w_{pc1}}{w_{zc1}}=\frac{w_{pc2}}{w_{zc2}}=\frac{w_{pc}}{w_{zc}} \tag{2.73}$$

The magnitude of T_c can be expressed as

$$|T_c(w)| = \frac{B\left[1+\left(\frac{w}{w_{zc}}\right)^2\right]}{K^2 w\left[1+\left(\frac{w}{w_{pc}}\right)^2\right]} \tag{2.74}$$

The phase shift of T_c is computed as

$$\phi_{Tc}(w) = -\frac{\pi}{2} + 2\arctan\left(\frac{w}{w_{zc}}\right) - 2\arctan\left(\frac{w}{w_{pc}}\right) \tag{2.75}$$

The geometric average value of the zero frequency and the pole frequency produces the highest value of phase, and is calculated as

$$w_m = w_c = \sqrt{w_{zc} w_{pc}} = w_{zc}\sqrt{K} = \frac{w_{pc}}{\sqrt{K}} \tag{2.76}$$

The phase shift when $f = f_m$ is obtained by substituting (2.76) into (2.75) as follows

$$\phi_{Tc}(f_m) = -\frac{\pi}{2} + 2\arctan\left(\frac{K-1}{2\sqrt{K}}\right) = -\frac{\pi}{2} + 2\arcsin\left(\frac{K-1}{K+1}\right) \tag{2.77}$$

As a result, based on (2.77), the greatest phase shift decrease is

$$\phi_m = \phi_{Tc}(f_m) + \frac{\pi}{2} = 2\arctan\left(\frac{K-1}{2\sqrt{K}}\right) = 2\arcsin\left(\frac{K-1}{K+1}\right) \tag{2.78}$$

Thus, based on (2.78), the controller's *K* factor may be calculated as

$$K = \frac{1+\sin\left(\frac{\phi_m}{2}\right)}{1-\sin\left(\frac{\phi_m}{2}\right)} = \tan^2\left(\frac{\phi_m}{4} + \frac{\pi}{4}\right) \tag{2.79}$$

As a result, the greatest phase shift ϕ_m may be calculated by using (2.79) as

$$\phi_m = -\pi + 4\arctan\sqrt{K} \tag{2.80}$$

When (2.76) is substituted for (2.74), the magnitude of the Integral-double-lead controller voltage transfer function at frequency $f = f_m$ is obtained as

$$|T_c(f_m)| = \frac{B}{w_m K} \tag{2.81}$$

At the crossover frequency $f = f_m$, the magnitude of the loop gain is computed as

$$|T(f_c)| = |T_c(f_c)||T_k(f_c)| = |T_c(f_c)||T_{mp}(f_c)|\beta = 1 \tag{2.82}$$

At the crossover frequency f_c, one obtains the phase shift of the loop gain as follows.

$$\phi_T(f_c) = \phi_{T_k}(f_c) + \phi_{Tc}(f_c) \tag{2.83}$$

The phase boost is

$$\phi_m = 90^o + \phi_{Tc}(f_c) \tag{2.84}$$

By using (2.77), one obtains the phase margin as

$$PM = 180^o + \phi_{Tk}(f_c) = 180^o + \phi_{Tk}(f_c) + \phi_{Tc}(f_c) = 180^o + \phi_{Tk}(f_c) + \phi_m - 90 = 90^o + \phi_{Tk}(f_c) + \phi_m \tag{2.85}$$

As a result, the needed phase boost is calculated as

$$\phi_m = PM - 90^o - \phi_{Tk}(f_c) \tag{2.86}$$

2.5 Cascade control of DC-DC Buck converter

A cascade controller is used in DC Microgrid systems to meet the increasing requirement for good load and supply-voltage regulation of DC/DC converters in continuous conduction mode (CCM). Cascade control is utilized when there are several measurements but only one control signal. To improve control performance, the cascade controller contains two cascaded control loops: internal current control and outer voltage control. Each external voltage control and internal current control loop has its own feedback controller [39], [27]. The cascade controller is built on DC-DC buck converter parameters, with the internal current control loop's dynamics significantly quicker than the outside voltage control loop's. The main benefit of using cascade control in DC Microgrid systems is that the internal current controller resolves disturbances inside the internal current loop before they affect the value of the outside voltage-controlled. Following that, a Proportional-Integral (PI) controller is utilized to follow the required reference input and reduce load disturbances. Fig. 2.12 depicts a cascade controller used for a DC-DC Buck converter in CCM.

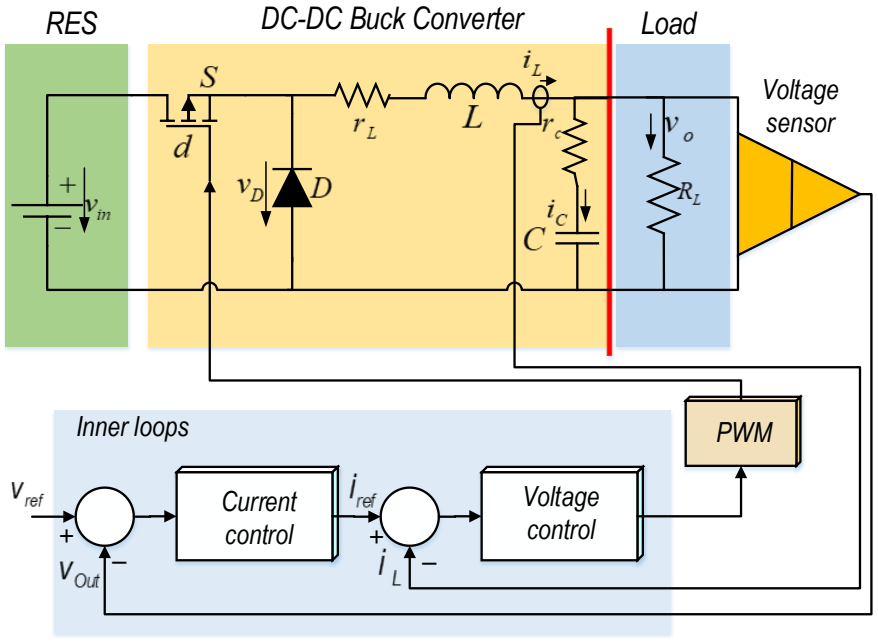


Fig. 2.12. The DC-DC Buck converter cascade controller operates in CCM

To provide the highest dynamic performances, the cascade controller uses a serial PI controller for both in the outer loop voltage and in the inner loop current of the DC-DC Buck converter. Fig. 2.13 depicts a simplified block diagram of the DC-DC Buck converter with serial PI controller. According to Fig. 2.12, the PI controllers are designed utilizing the current and voltage transfer function.

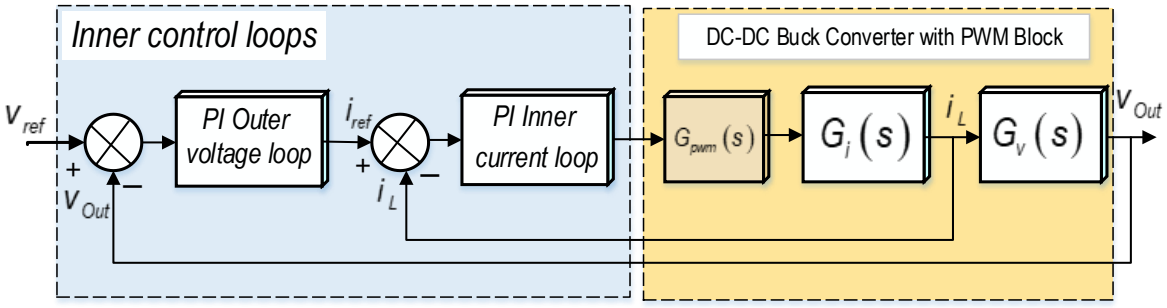


Fig. 2.13. DC-DC Buck converter simplified block diagram with serial PI controller.

where

$G_v(s)$: transfer function of the voltage loop

$G_i(s)$: transfer function of the current loop

$G_{pwm}(s)$: transfer function of the PWM

Using Fig. 2.12 and (2.1), (2.2), one can calculate the voltage surrounding a DC-DC Buck converter supplying a resistive load as follows.

$$v_{out} - v_{in} = L\frac{di}{dt} + r_L i_L \tag{2.87}$$

Using the linearization approach and (2.87), the current transfer function of a DC-DC Buck converter feeding a resistive load is obtained as follows:

$$G_i(s) = \frac{i_L(s)}{d(s)} = \frac{V_{in}}{V_m\left(r_L + Ls\right)} \tag{2.88}$$

where r_L is the inductance's resistive parasites. V_{in} is the input voltage's nominal value. V_m is nominal value from peak to peak.

Current flows through the capacitance may be calculated using Kirchhoff's principles on the DC-DC Buck converter feeding a resistive load as

$$i_c = i_L - i_{out} = C\frac{dV_c}{dt} + \frac{V_c}{r_c} \tag{2.89}$$

The voltage transfer function of the DC-DC Buck converter feeding a resistive load may be calculated using (2.1), (2.2), and (2.89) as follows

$$G_v(s) = \frac{v_{out}(s)}{i_L(s)} = \frac{R_{load}(Cr_c s + 1)}{Cs(R_{load} + r_c) + 1} \tag{2.90}$$

Where R_{load} is the resistive load. r_c is the capacitance's resistive parasites. C is the nominal value of the capacitance.

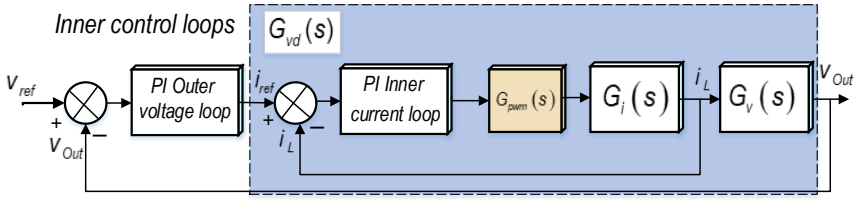
The transfer function $G_{vd}(s)$, as shown in Fig. 2.14, is a series combination of the closed current loop transfer function with the PI inner controller and the voltage loop transfer function. This transfer function is required in order to compute the PI outer voltage controller. By using (2.88), (2.90), and the transfer function of the PI inner current controller, one obtains the transfer function of $G_{vd}(s)$ as follows

$$G_{vd} = \frac{\omega s^2 + (\mu + \delta)s + \lambda}{\alpha T s^3 + (\alpha\beta + T)s^2 + (\alpha\gamma + \beta)s + \gamma} \tag{2.91}$$

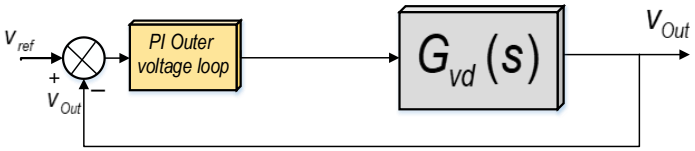
where

$$\alpha = CR_{load} + Cr_c, \beta = 1 + \frac{V_{in}k_{p\_c}}{r_L V_m}, \gamma = \frac{k_{i\_c}V_{in}}{r_L V_m}, \; T = \frac{L}{r_L}, \mu = \frac{R_{load}k_{i\_c}Cr_cV_{in}}{r_L V_{in}}, \lambda = \frac{R_{load}k_{i\_c}V_{in}}{r_L V_{in}},$$

$$\omega = \frac{R_{load}k_{p\_c}Cr_cV_{in}}{r_L V_{in}}, \delta = \frac{R_{load}k_{p\_c}V_{in}}{r_L V_{in}}$$



(a)



(b)

Fig. 2.14. Simplified block diagram of the DC-DC Buck converter with G_{vd} transfer function

2.6 Local control configuration of a DC Microgrid system

As stated in Chapter I, DC Microgrid has three control levels: primary control, secondary control, and tertiary control. This section delves into the primary control level (also known as the local control level) [3], [17], [27]. The DC-DC PWM converters, being the backbone of DC Microgrid systems, play a vital role in the whole system's efficient and dependable functioning. Adjustable local current and voltage control, as well as precise power sharing among parallel linked DC-DC PWM converters, should be used to provide not only appropriate local functioning, but also synchronized connections across different components in a DC Microgrid systems. Fig. 2.15 depicts the primary control level schematic for a DC-DC Buck converter in DC MGs, which normally includes current and voltage controllers as well as a droop control loop. Proportional-integral (PI) controllers are frequently used in DC Microgrid systems to ensure effective regulation of the output voltage and output current of the DC-DC converters.

The PI controller's main advantages include 0% steady-state error, ease of tuning, and high robustness. Droop control is frequently built on top of inner loops (current control and voltage control), particularly for the purpose of current sharing [39-44]. Fig. 2.15 shows that in droop

control, the feedback signal might be either output power or output current. The output power of a DC Microgrid with a power-type load can be utilized as droop control, as shown in Fig. 2.16 (a). Based on Fig. 2.16 (a), the reference for voltage controller in a power-type load may be calculated as follows:

$$v^{*}_{DCi} = v^{*}_{DC} - m_p.P_{oi} \tag{2.92}$$

Where v^{*}_{DCi} is the reference value of the DC-DC PWM converter's DC output voltage; v^{*}_{DC} is the value of output voltage; m_p is the droop coefficient in power-based droop controllers; P_{oi} is the output voltage of each DC-DC PWM converter.

When the current signal type is employed, however, as illustrated in Fig. 2.16 (b), the droop control coefficient m_c can be viewed as a virtual internal resistance. Based on Fig. 2.16 (b), the reference for voltage controller in a current-type load may be determined as follows:

$$v^{*}_{DCi} = v^{*}_{DC} - m_c.\mathrm{I}_{oi} \tag{2.93}$$

Where I_{oi} is the output current of each DC-DC PWM converters; m_c is the droop coefficient in current-based droop controller.

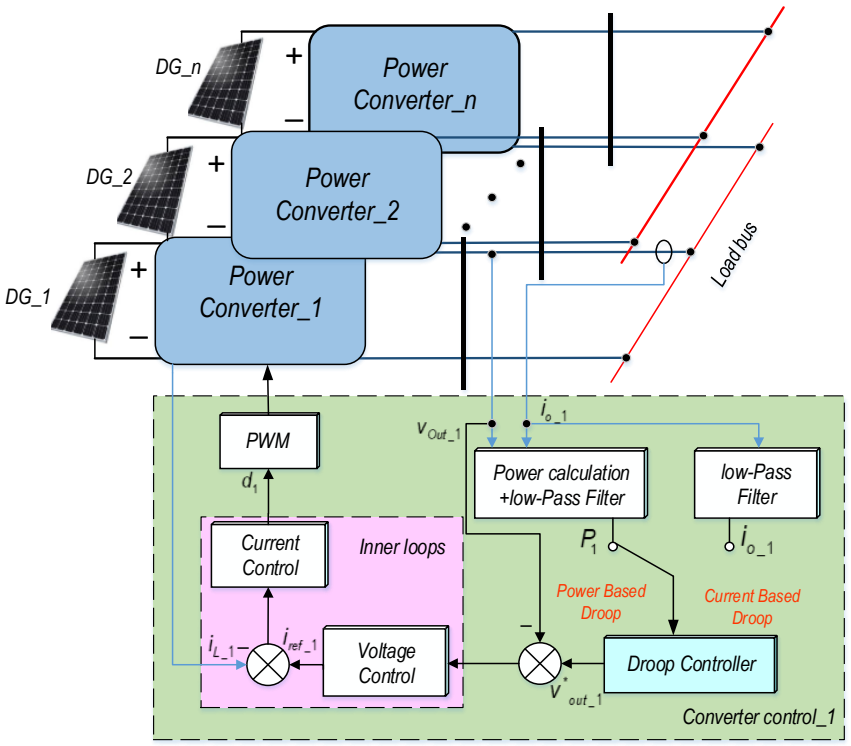


Fig. 2.15. Primary control level control schematic for a DC-DC Buck converter in DC MGs

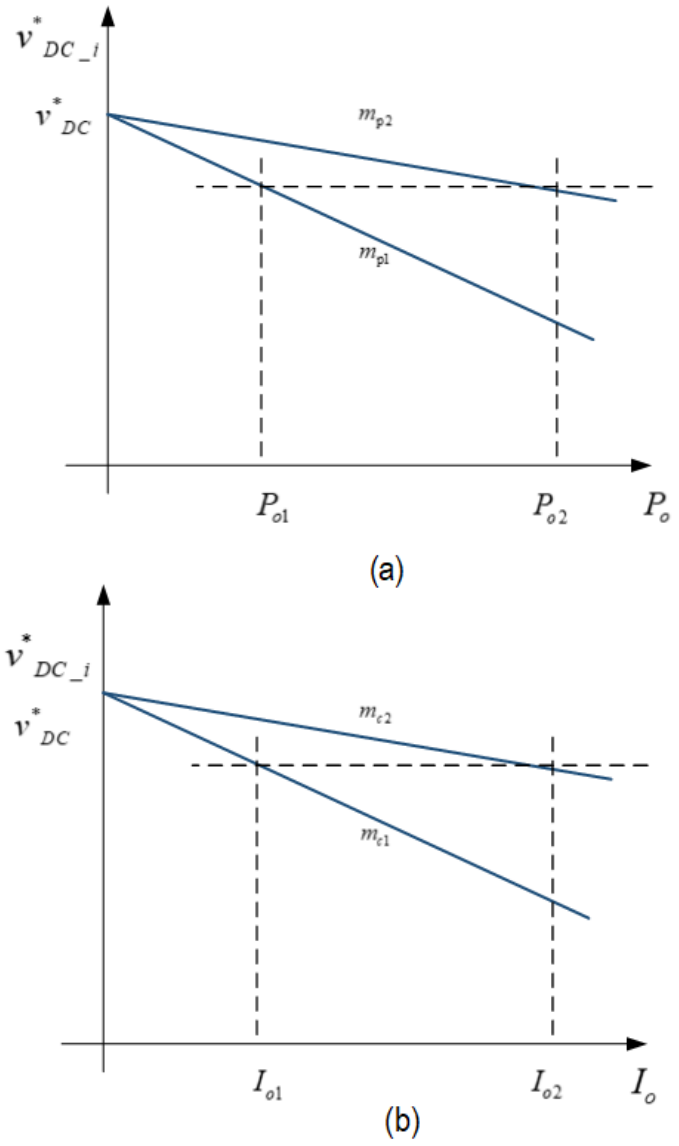
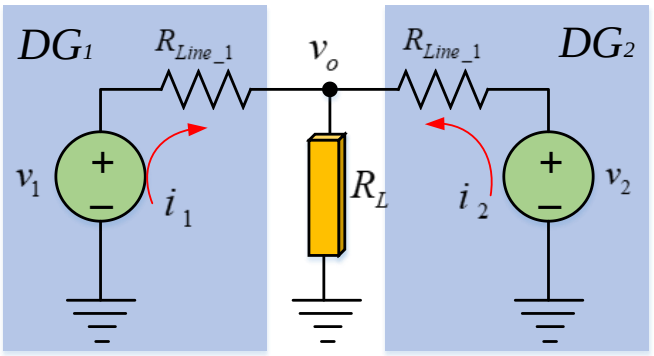


Fig. 2.16. Droop characteristic of DC Microgrid. (a) Power-Based Droop. (b) Current-Based Droop

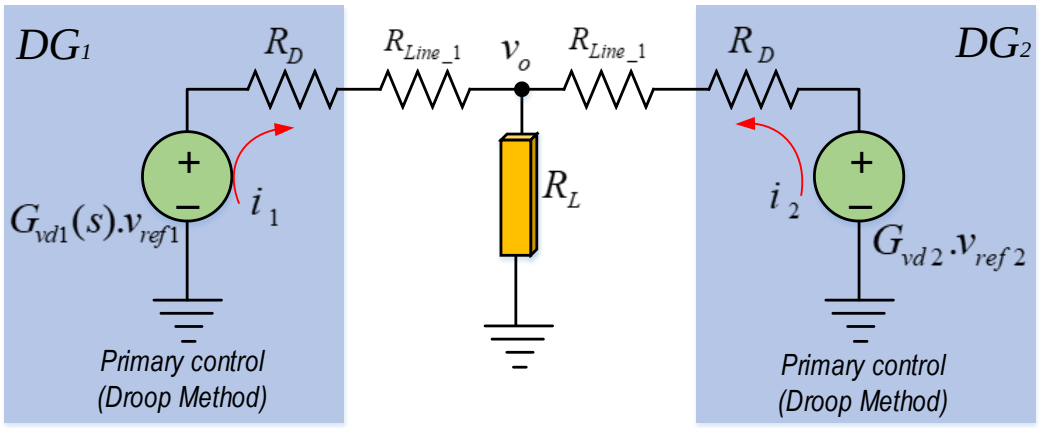
2.7 Droop control loop

Droop control is commonly used in the primary control level to minimize current circulation caused by the interconnection of parallel DC-DC PWM converters [3], [27]. It may incorporate a virtual impedance control loop to simulate the DC-DC PWM converter's physical output impedance. The equivalent circuit of two paralleled DC-DC PWM converters sharing a common load via resistive output impedances, as depicted in Fig. 2.17. According to Fig. 2.17 (a), when there is a voltage difference between the DC source suppliers, a current circulation between both DC source suppliers occurs. Using the primary control level of a DC Microgrid system and the characteristic *V-I* or *V-P* shown in Fig 2.16, current circulation may be prevented

by adding virtual output impedances, as depicted in Fig. 2.17 (b). In order to maintain the power consumption of each DC-DC Buck converter, virtual resistance is manufactured instead of real resistance using the outer control loop with a droop gain added to the DC-DC Buck converter control loop. This control level, as shown in Fig. 2.15, modifies the voltage reference provided to the inner current and voltage control loops of the DC-DC PWM converters, as well as the virtual output impedance loop.



(a)



(b)

Fig. 2.17. Two DC-DC PWM converters' Thevenin equivalent circuit. (a) Equivalent circuit of two parallel-connected DC-DC PWM converters. (b) Two DC-DC PWM converters linked in parallel with the primary control level

According to Fig 2.15, the output voltage can be expressed as

$$v_{oi} = v_{ref\_i} - R_D.i_{oi} \tag{2.94}$$

Where i_{oi} is the output current of the DC-DC converter i; R_D is the value of the virtual output impedance; v_{ref_i} is the reference voltage for the output voltage of the DC-DC converter i.

If ε_v is the maximum allowable voltage variation, R_D and v_{ref_i} must be built as

$$v_{ref\_i} = v_{n\_i} - \varepsilon_v / 2 \tag{2.95}$$

$$R_D = \varepsilon_v / i_{\max\_i} \tag{2.96}$$

Where v_{n_i} denotes the nominal output voltage of the DC-DC PWM converter *i*; and $i_{\max\_i}$ is the maximum output current of the DC-DC PWM converter *i*.

Droop control loop, in general, consists of increasing series resistance in each branch carrying the DC-DC Buck converter to achieve the same voltage level at the point of connection as shown in Fig. 2.17 (b). The droop control loop, as illustrated in Fig. 2.16 (b), supplies a resistive output impedance to the DC-DC PWM converters to compensate for the voltage reference discrepancy. $\Delta v_{oi} = v_{o1} - v_{o2}$. As a result, the current sharing between the two DC-DC PWM converters $\Delta i_{oi} = i_{o1} - i_{o2}$, which can be obtained as

$$\Delta i_{oi} = \Delta v_{oi}^{*} / R_D \tag{2.97}$$

The droop control loop not only enables parallel functioning of the DC-DC PWM converters, but it also enhances the output voltage's dynamic performance. It does, however, have an intrinsic load-dependent voltage deviation.

2.8 Modeling of the parallel connecting of two DC-DC Buck converters

The parallel interconnection of two DC-DC Buck converters, constituting the DC MG, is provided to demonstrate the practicality of the suggested primary control level (droop control method) [27]. Fig. 2.18 depicts a block diagram of two DC-DC Buck converters that comprise a DC Microgrid system and feed the same resistive load. A mismatch in cable resistance connecting the output of each DC-DC buck converter to the DC bus might produce an inaccuracy in current load sharing among the converters. The primary control level of the DC Microgrid system is obtained by first calculating the inner loop controllers of the current and voltage loops, as illustrated in Fig. 2.19. The parallel connector equivalent circuit of two DC-DC Buck converters operating in CCM with their inner loop controllers and the droop control loops, as depicted in Fig. 2.19. The main reason for using the droop control loop is to share the same power between the parallel connections of the DC-DC Buck converter.

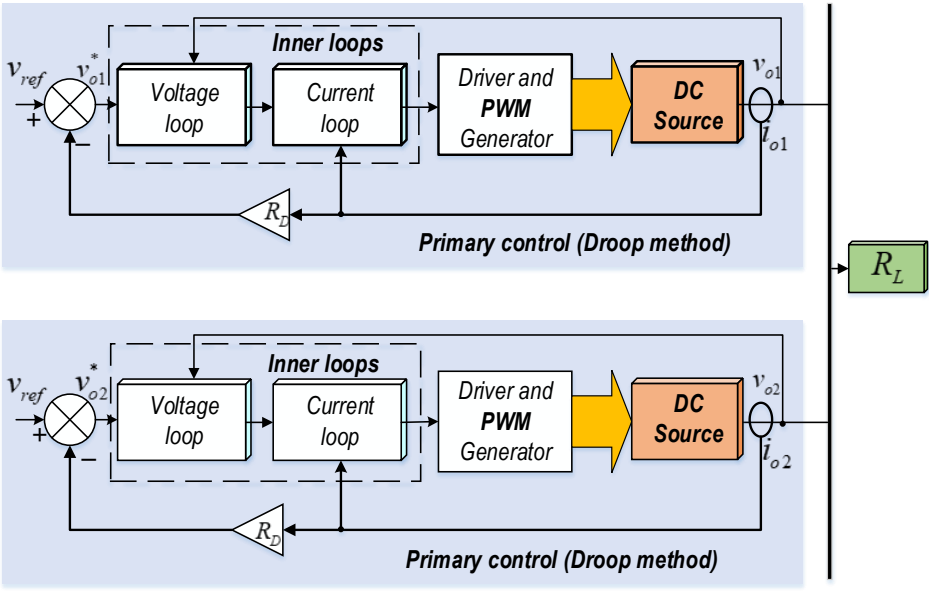


Fig. 2.18. Primary control level of a DC Microgrid

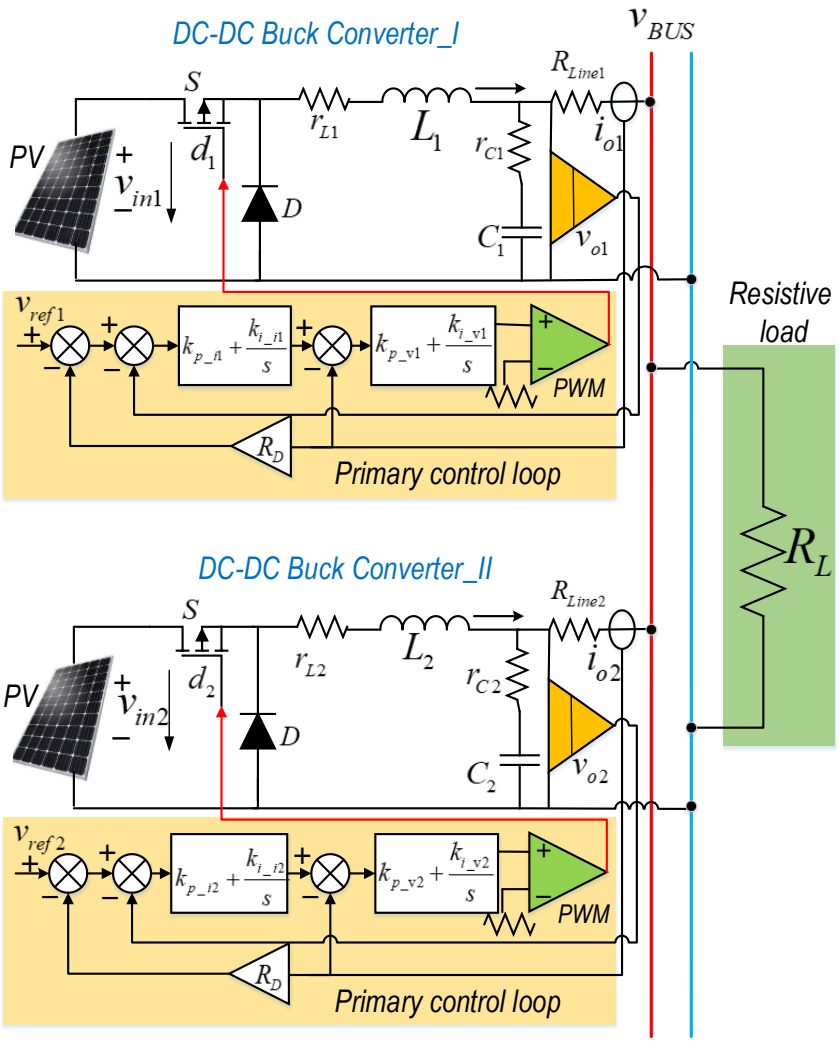


Fig. 2.19. Equivalent electrical circuit of a DC Microgrid system's primary control level

As a result, for our simulation, we suppose that the cable resistance of the DC-DC Buck converter 1 is twice that of the DC-DC Buck converter 2. Furthermore, we will consider the DC-DC Buck converters, which do not have the same dynamic properties. Their input voltage v_{in} and pick _to pick value V_m are both fixed at $28V$ and $10V$, respectively. The dynamic parameters for each DC-DC Buck converter are shown in Tables 2.1 and 2.2.

Tab 2.1. Dynamic parameters of DC-DC Buck converter I

Variables	Descriptions	value
L_1	Nominal inductance	*6 mH*
r_{L1}	the inductance's resistive parasites	*0.8 mH*
C_1	Nominal capacitance	$470\mu F$
r_{C1}	the capacitance's resistive parasites	$0.001\mu F$
v_{out}	Output voltage	$14V$
f_{sw}	Switching frequency	$25kHz$

Tab 2.2. Dynamic parameters of DC-DC Buck converter II

Variables	Descriptions	value
L_2	Nominal inductance	*2.7 mH*
r_{L2}	the inductance's resistive parasites	*3.3 mH*
C_2	Nominal capacitance	$220\mu F$
r_{C2}	the capacitance's resistive parasites	$0.001\mu F$
v_{out}	Output voltage	$14V$
f_{sw}	Switching frequency	$25kHz$

The DC Microgrid controller loops depicted in Fig. 2.19 are calculated using a PI controller. Using (2.51) and (2.53), the parameters of the PI compensator for each DC-DC Buck converter

can be designed based on Fig. 2.14 and the transfer functions explained in (2.88) and (2.90). The PI compensator design process can be structured as follows:

At the desired crossover frequency, the magnitude of the current loop transfer function is calculated as:

$$\left|\mathrm{G}_i(f_{c\_d})\right| = \frac{v_{inp}}{V_m\sqrt{r_L^2 + (L2\pi f_{c\_d})^2}} \tag{2.98}$$

hence

$$\left|\mathrm{G}_i(f_{c\_d})\right| k_{p\_c} = 1 \tag{2.99}$$

Resulting in the gain of the inner loop current controller's k_{p_c} section is

$$k_{p\_c} = \frac{1}{\left|\mathrm{G}_i(f_{c\_d})\right|} = \frac{V_m\sqrt{r_L^2 + (L2\pi f_{c\_d})^2}}{v_{in}} \tag{2.100}$$

As a result, the coefficient of the inner loop current controller's integral part k_{i_c} is calculated as

$$k_{i\_c} = \frac{2\pi f_{c\_d}}{10} k_{p\_c} = \frac{2\pi f_{c\_d} V_m\sqrt{r_L^2 + (L2\pi f_{c\_d})^2}}{10 v_{in}} \tag{2.101}$$

By using (2.90), (2.100), and (2.101), ones can calculate the proportional part of the outer loop transfer function (2.91) as follows

$$k_{p\_v} = \frac{1}{\left|\mathrm{G}_{vd}(f_{cv\_d})\right|} \tag{2.102}$$

At the desired crossover frequency f_{cv_d}, the magnitude of the outer loop transfer function G_{vd} is calculated as:

$$\left|G_{vd}(f_{cv\_d})\right| = \frac{G_{vdo}\sqrt{G_1 G_2}}{\sqrt{G_3 + G_4}} \tag{2.103}$$

where

$$G_1 = k_{i\_c}^2 + \left(\frac{v_{in} 2\pi f_{cv\_d}}{V_m r_L} \right)^2 \tag{2.104}$$

$$G_2 = \left(C r_c 2\pi f_{cv\_d} \right)^2 + 1 \tag{2.105}$$

$$G_3 = \left(\left[C(R_L + r_c) 2\pi f_{cv\_d} \right]^2 + 1 \right) \left[\left(1 + \frac{v_{in} k_{p\_c}}{V_m r_L} \right) 2\pi f_{cv\_d} \right]^2 \tag{2.106}$$

$$G_4 = \left(\frac{L}{r_L} \left(2\pi f_{cv\_d} \right)^2 \right)^2 \tag{2.107}$$

$$G_{vdo} = \frac{R_L v_{in}}{V_m r_L} \tag{2.108}$$

Thus, the coefficient of the outer loop controller's integral part k_{i_v} can be designed as

$$k_{i\_v} = \frac{2\pi f_{cv\_d}}{10} k_{p\_v} = \frac{2\pi f_{cv\_d}}{10 \left| \mathrm{G}_{vd}(f_{cv\_d}) \right|} \tag{2.109}$$

For the inner loops strategy, the outer loop controller has a faster settling time response than the inner loop controller.

The voltage and current loops transfer function are calculated using Tabs 2.1 and 2.2 and based on (88), (90) as follows:

1. For the DC-DC Buck converter I:

$$\begin{cases} G_{i\_I}(s) = \dfrac{2.8}{0.006s + 0.8} \\ G_{v\_I}(s) = \dfrac{4.7e-06+10}{0.0047s+1} \end{cases} \tag{2.110}$$

2. For the DC-DC Buck converter II:

$$\begin{cases} G_{i\_II}(s) = \dfrac{2.8}{0.0027s + 3.3} \\ G_{v\_II}(s) = \dfrac{2.2e-06+10}{0.0022s+1} \end{cases} \tag{2.111}$$

The PI parameters for the inner and outer loops can be calculated using (2.100), (2.101), and (2.102), (2.109), respectively, by setting $f_{c\_d} = 1e3$ and $f_{cv\_d} = 0.1e3$.

1. The inner and outer loop controllers of the DC-DC Buck converter I

$$\begin{cases} G_{PI\_c} = \dfrac{13.47s + 8462}{s} \\ G_{PI\_v} = \dfrac{0.3097s + 19.46}{s} \end{cases} \tag{2.112}$$

2. The inner and outer loop controllers of the DC-DC Buck converter II

$$\begin{cases} G_{PI\_c} = \dfrac{6.172s + 3878}{s} \\ G_{PI\_v} = \dfrac{0.202s + 12.69}{s} \end{cases} \tag{2.113}$$

2.9 Simulation results

PSIM software is used for simulation to verify the theoretical primary control approach. The simulation comprises a DC-Microgrid feeding a resistive load configured in the same way as shown in Fig. 2.19 and functioning under the suggested primary control technique. Two DC-DC buck converters working in CCM and coupled in parallel to feed a resistive load comprise the DC Microgrid utilized. In this simulation, the DC-DC buck converters get their input voltages from DC sources, which may be seen as an analogous depiction of RESs. The specifications for DC-DC buck converters are the same as those given in Tabs 2.1 and 2.2. In this simulation, the virtual output resistance was set at $R_D = 2\Omega$. Fig. 2.25 shows the PSIM simulation of a DC Microgrid system with the proposed primary control.

Fig. 2.20 depicts the dynamic behavior of the output voltage and current for both DC-DC Buck converters when the suggested primary controller is used. According to Fig. 2.20, the proposed main control (droop control) is successful in avoiding the current circulation problem and sharing the same power between the DC-DC Buck converters. Furthermore, the DC-DC Buck converters' output voltages v_{o_1}, v_{o_2} are controlled to their intended values in a short time response, with no overshoot observed.

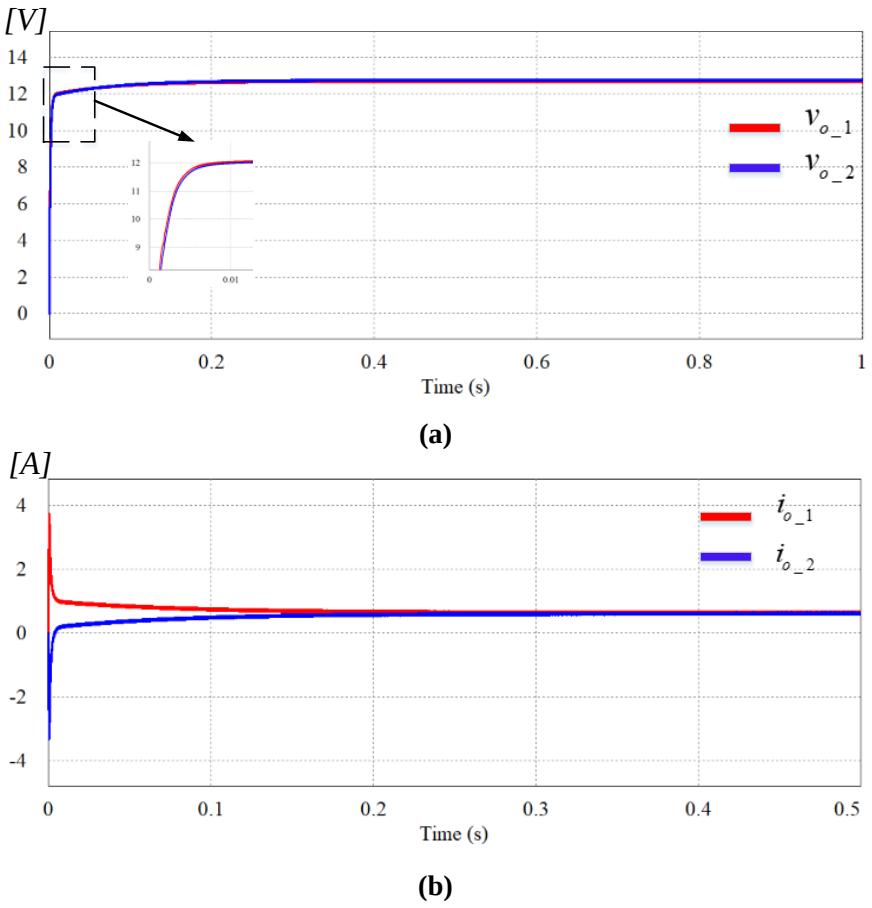


Fig. 2.20. The dynamic behavior of the DC-DC Microgrid utilizing the primary control suggested. (a) Output voltage. (b) Output current

In order to validate the proposed primary control, three scenarios are performed in this simulation. The first scenario is used to test the efficacy of the proposed primary control against sudden fluctuations in the DC-DC Buck converters' input voltage. This scenario is implemented as follows: both input voltages of the DC-DC Buck converters experience sudden fluctuations. As shown in Fig. 2.21(a), the DC-DC Buck converters' input voltages v_{in_1}, v_{in_2} are changed from $28V$ to $13V$ and then returned to $28V$. In this scenario, the resistive load remains constant. Figs. 2.21(b) and 2.21(c) show the simulation results of the output voltage and output current of the DC-DC Buck converters under this scenario.

One of the most important power quality challenges is input voltage fluctuation, which may damage electronic equipment and cause substantial systemic difficulties. Furthermore, fluctuations in input voltage degrade the quality of electronic equipment and cause internal voltages and currents to fluctuate.

Based on the simulation results, it is clear that the behavior of the output voltage and current stays unchanged, and no substantial fluctuation is noticed despite the variation in the input voltage of the DC-DC Buck converters. The proposed primary controller rejects all input voltage variations induced by the DC-DC Buck converters. The influence of variable input voltage on the output voltage and current of DC-DC Buck converters is essentially non-existent.

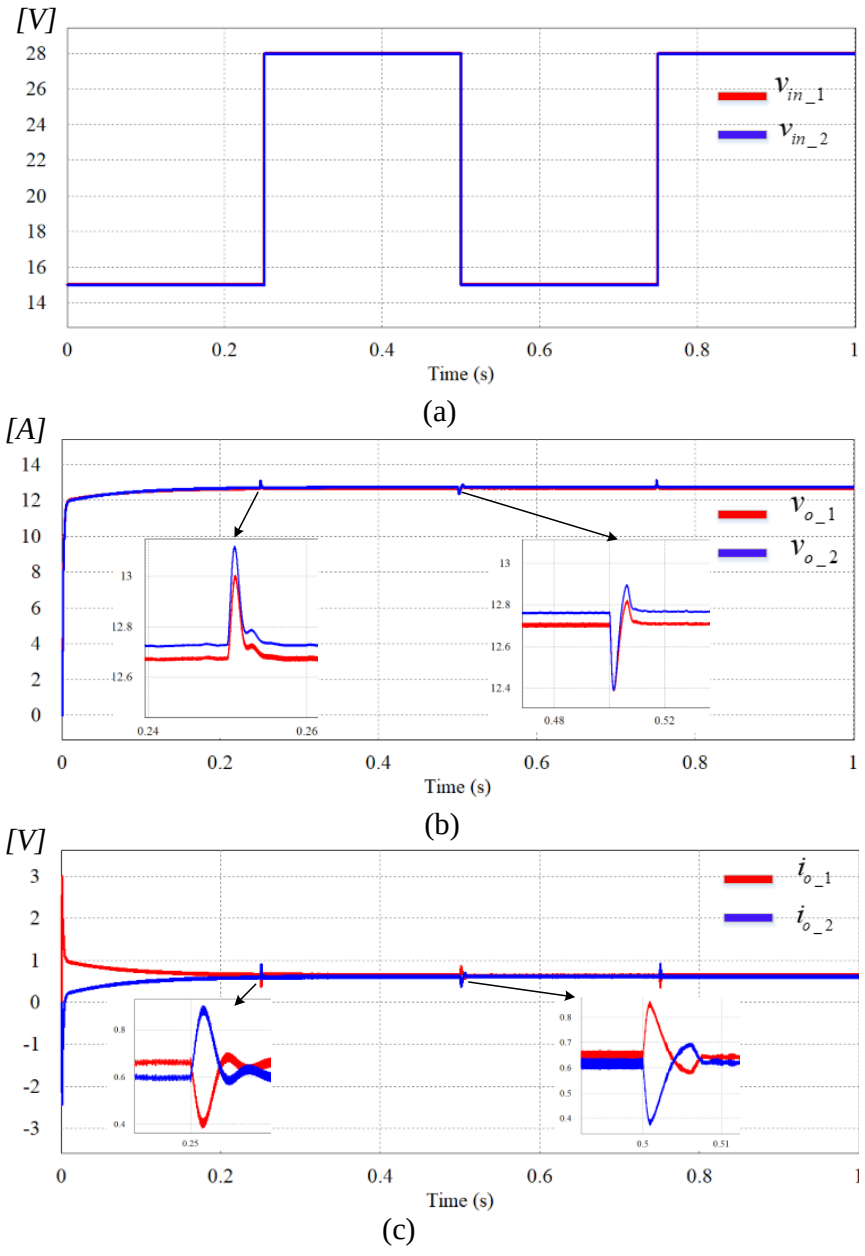
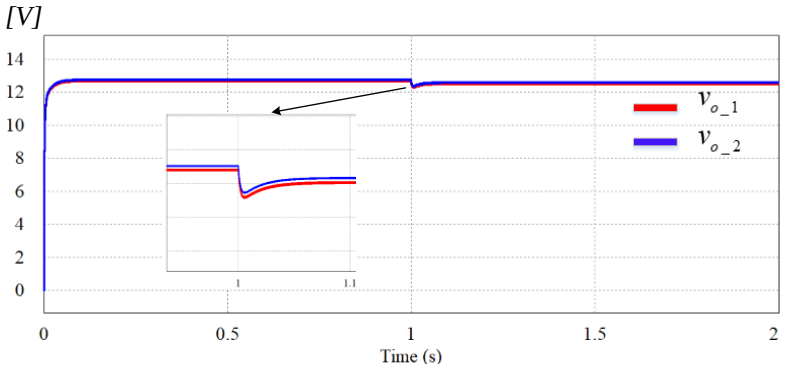


Fig. 2.21.The DC Microgrid's behavior in the presence of an input voltage fluctuation scenario. (a) Scenario of input voltage fluctuation. (b) Output voltages of the DC-DC Buck converter. (c) Output currents of the DC-DC Buck converter.

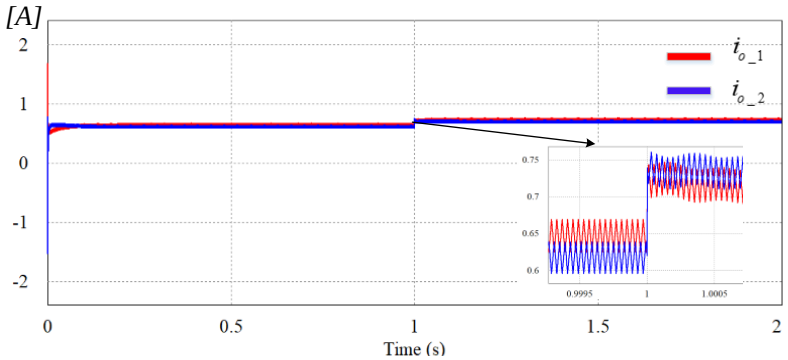
The second scenario is used to evaluate the efficacy of the suggested primary control against disturbances produced by the variations of resistive load R_L . The second scenario is carried out as

follows: the resistive load is maintained at the nominal value $R_L = 10\Omega$ from 0s to 1s. After that, the resistive load suddenly increases to $R_L = 15\Omega$ at 1s. Fig. 2.22 depicts the simulation results for this scenario.

The resistance value has been adjusted in this scenario to test the performance of the proposed primary control of the DC Microgrid. Normally, sudden increases in the resistive load cause a drop in the output voltage, which causes a quick increase in heat, which might burn the insulation of the overall system. The output voltages of the DC-DC Buck converters v_{o_1}, v_{o_2} have a short settling time with a quick rise time, as shown by the simulation results in Fig. 2.22 (a), and no overshoot is detected. By changing the resistive load value R_L, it was observed that the suggested primary control rejected the sudden fluctuation with no change noticed in the output voltages of the DC-DC Buck converter. The power sharing between the DC-DC Buck converters was maintained by employing the suggested primary controller, despite a significant fluctuation in the resistive load with a short time response and with no overshoot, as seen in Fig. 2.22 (b).



(a)

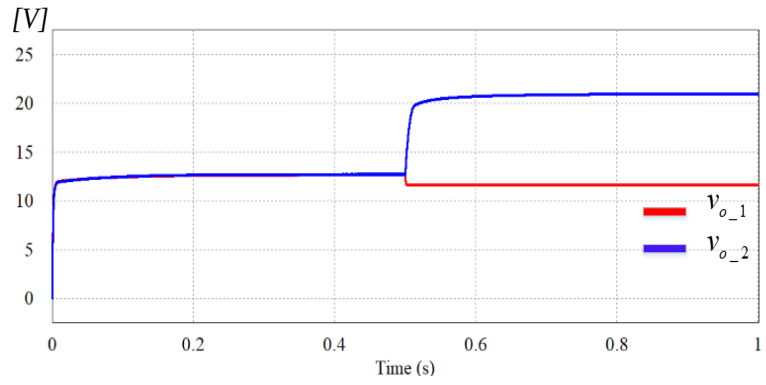


(b)

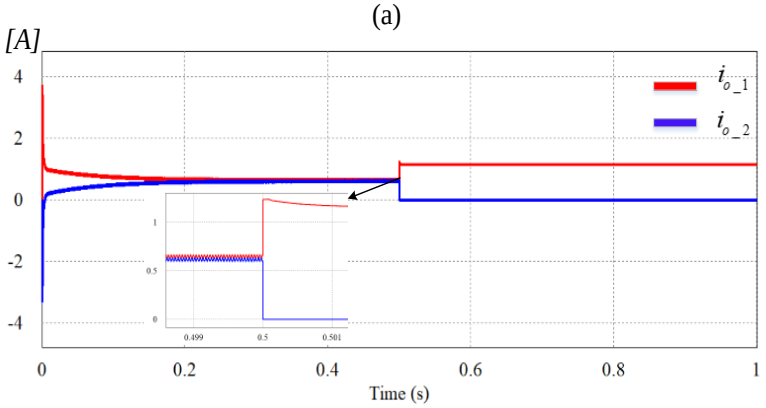
Fig. 2.22.The behavior of a DC microgrid in the presence of resistive load variation. (a) The DC-DC Buck converters' output voltage behavior. (b) The DC-DC Buck converters' output current behavior

The third scenario is performed to validate the efficiency of the suggested primary control in minimizing disruptions caused by connecting or removing one DC-DC buck converter from the DC Microgrid's common DC bus. This scenario is carried out in the following manner: In Case 1, the second DC-DC Buck converter is unplugged from the DC Microgrid's common DC Bus after 0.5s. In Case 2, the same DC-DC Buck converter is linked to the DC Microgrid's common DC Bus at 0.5s. Figs .2.23 and 2.24 illustrate the simulation results for this scenario.

Considering the DC Microgrid response in Case 1, as shown in Fig. 2.23, the proposed primary control has been to control the output voltage of the DC-DC Buck converter I, despite the removal of the second DC-DC Buck converter of the DC Microgrid. The suggested primary control compensated for the power losses caused by the removal of the DC Microgrid's second DC-DC Buck converter. In Case 2, as shown in Fig. 2.24, the proposed primary control shared the same power after connecting the second DC-DC Buck converter to the DC Microgrid's common DC Bus, with a short response time and no overshoot. Furthermore, after connecting the second DC-DC Buck converter to the DC Microgrid's common DC Bus, the output voltages were effectively maintained at their appropriate levels.

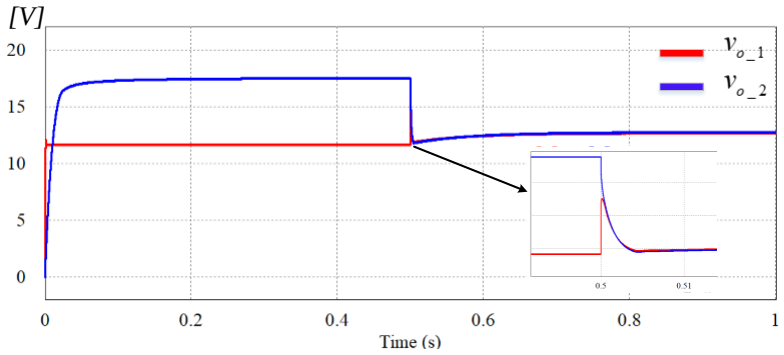


(a)

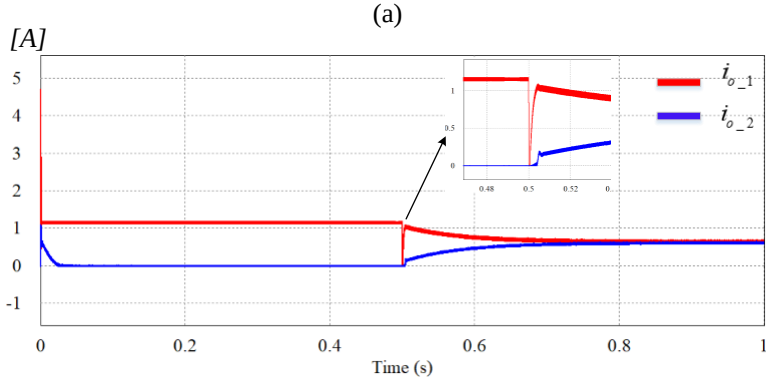


(b)

Fig. 2.23.The behavior of a DC microgrid after unplugging the second DC-DC Buck converter. (a) Output voltages. (b) Output currents



(a)



(b)

Fig. 2.24.The behavior of a DC microgrid after plugging in the second DC-DC Buck converter. (a) Output voltages (b) Output currents

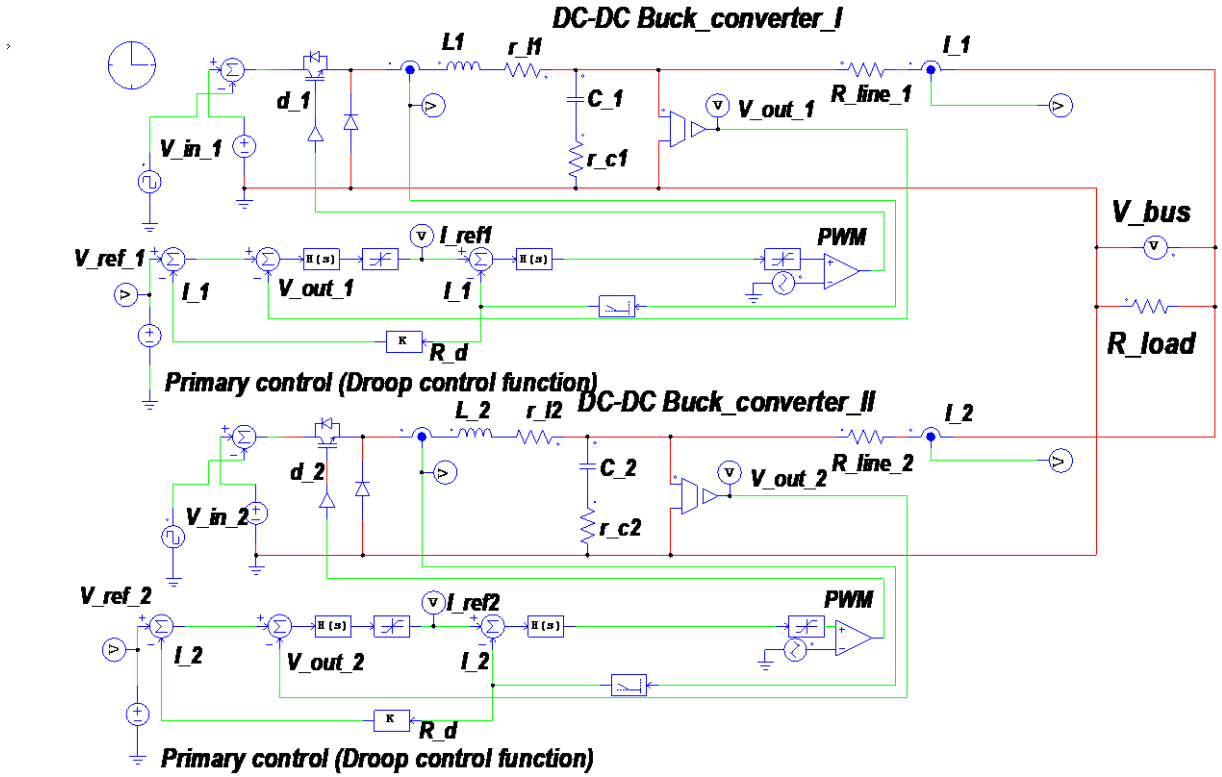


Fig. 2.25. DC Microgrid system with the proposed primary control stimulated by the PSIM software

2.10 Conclusion

The results of the simulation research shown in this chapter demonstrate that the proposed strategy improved the robustness of the primary control against the current circulation problem and disturbances. The suggested primary control enables improved regulation of the output voltages and currents of the DC-DC buck converters that comprise the DC Microgrid. The suggested primary control assures power sharing between the DC-DC Buck converters used to construct the DC Microgrid and the power flow required to supply the resistive load.

This chapter also covers the design of the single double lead controller (Type II), the integral double lead controller (Type III), the PI controller, and a cascade controller, all of which are required to regulate the DC-DC Buck converter that comprises the DC Microgrid.

The voltage deviation caused by the primary control, on the other hand, needs rectification by a secondary controller. As a result, a higher control level might transmit all references to each DC-DC Buck converter that makes up the DC Microgrid in order to restore the amplitude of output voltages and the DC Bus.

Chapter 3: Robust Non-Singular Terminal Sliding Mode Control of DC-DC Buck Converter Feeding Constant Power Load

3.1. Introduction

This chapter discusses and simulates the buck converter supplying a constant power load (CPL) using PSIM software. For a Buck converter that feeds a tight voltage regulated DC-DC Boost converter , which acting as a CPL, two nonlinear controllers, a sliding mode controller (SMC) and a nonsingular terminal sliding mode controller (NTSMC), are used. PSIM software is used for the simulation study. It is made up of two scenarios that were operate to verify the theoretical nonlinear approaches.

The first scenario addresses issues related to fluctuations in the CPL of the DC-DC Buck converter that forms the DC-Microgrid. The second scenario, on the other hand, deals with problems related to the input voltage variation of the DC-DC Buck converter that keeps feeding a CPL. As such, a stability analysis of the DC-DC Buck converter is required to ensure the system's stable operation using the proposed nonlinear approaches. Let us first define the problem that arises from a Buck converter feeding a CPL.

3.2. Problem definition

Certain power systems, known as multi converter power systems, require serially connected DC-DC converters to offer a variety of power and voltage types to the system [5, 6], [45]. This type of system includes a large number of DC-DC converters configured in parallel, cascade, stacking, and splitting topologies for loads and sources to ensure optimal operation. Serially connected DC-DC converters, as shown in Fig. 3.1, are one sort of multi converter power electronic systems. This system comprises of an upstream DC-DC converter that supplies the required power to the system and a DC-DC converter (load converter) that transforms the output voltage to the right value for each load, implying that the output voltage must be tightly controlled [46-48].

When control is performed tightly, the load DC-DC converter (second stage of serially connected DC-DC converters) tends to exhibit the characteristic of a constant power load (CPL), which implies the DC-DC converter has a rapid response and minimal output ripple. As a result, the DC-DC converter acts similarly to the CPL in terms of control bandwidth. In CPLs, the output power of the load DC-DC converter is constant, i.e., the output voltage lowers with small fluctuations in the output current quantity (increasing output current), implying that the output power and input power of the DC-DC converter are identical when the wasted power into the whole system is ignored [49-51].

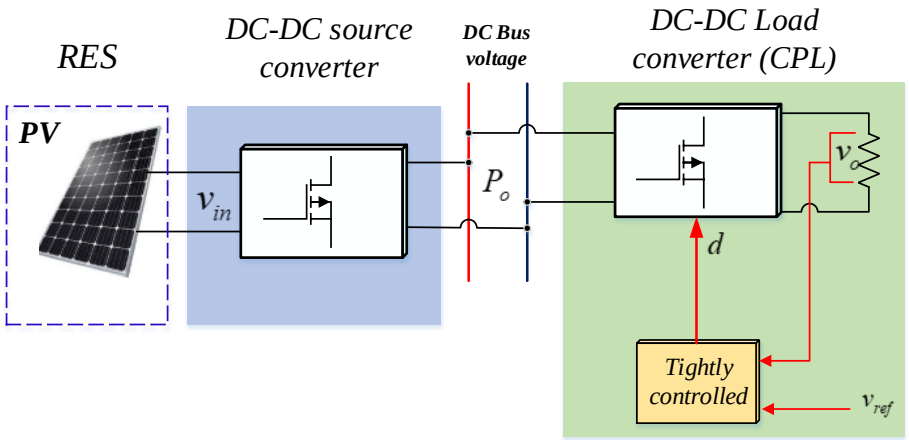


Fig. 3.1. Serially connected DC-DC converters with the second converter tightly regulated

DC-DC converters frequently exhibit the CPL characteristic when their output voltage exceeds the voltage reference V_c , as depicted in Fig. 3.2 [49-51]. Furthermore, the DC-DC converters can behave as a passive load at startup but as a CPL when the reference voltage V_c is exceeded.

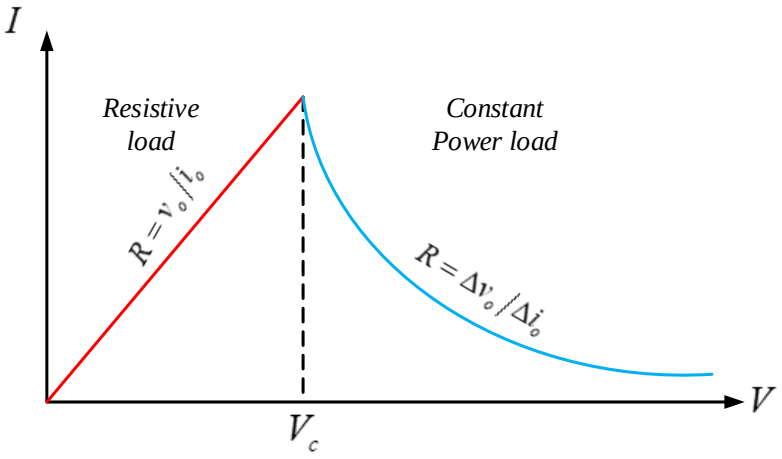


Fig. 3.2.V-I curve of a DC-DC load converter

Fig. 3.2 shows that the load DC-DC converter (CPL) has a negative incremental impedance, which means that the average difference between the output voltage and current $dv/di < 0$ is negative. The steady state point in serially connected DC-DC converters, as shown in Fig. 3.1, is attained when the CPL voltage equals the voltage source. By adding minor disturbances to the system, the steady state point can be explained if the load voltage is smaller than the voltage value of the stationary state. As a result, the load's output current will be greater than the CPL's output current, culminating in the discharge of the filter capacitor. This variation in current and voltage causes the power to remain constant by raising the current amount of the load while reducing the voltage amount of the load. The output current reaches infinity and the output voltage converges to zero as a result of this approach

[52-55]. Fig. 3.3 depicts the above-mentioned maintenance achieved by connecting a CPL and a capacitor filter in parallel.

One may get the state equation that depicts the circuit from Fig. 3.3 [4], which given as

$$\begin{cases} v_c = \dfrac{P}{i} \\ -i = C\dfrac{dv_c}{dt} \end{cases} \tag{3.1}$$

The solutions of the above maintained are provided as

$$\begin{cases} v_c^2 = V_c^2 - 2\dfrac{P}{C}t \\ i = \dfrac{P}{\sqrt{V_c^2 - 2\dfrac{P}{C}t}} \end{cases} \tag{3.2}$$

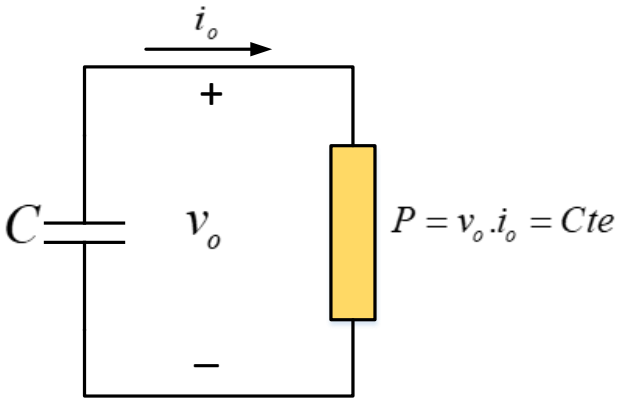


Fig. 3.3. A CPL connected in parallel with a capacitor filter

According to the above-mentioned equations in (3.2), at $t = V_c^2 C/2P$, the output voltage is 0, while the current is infinite. Hence, the circuit represented in Fig. 3.3, which includes a parallel CPL and capacitor filter, is unsteady. In this case, the system is unstable because, on the one hand, the impact of INR induced by the CPL, and on the other hand, because the output voltage drops to 0 as the current approaches infinity and conversely. The circuit's equilibrium point, depicted in Fig. 3.3, occurs when the voltage of CPL equals the source voltage [4-6], [45].

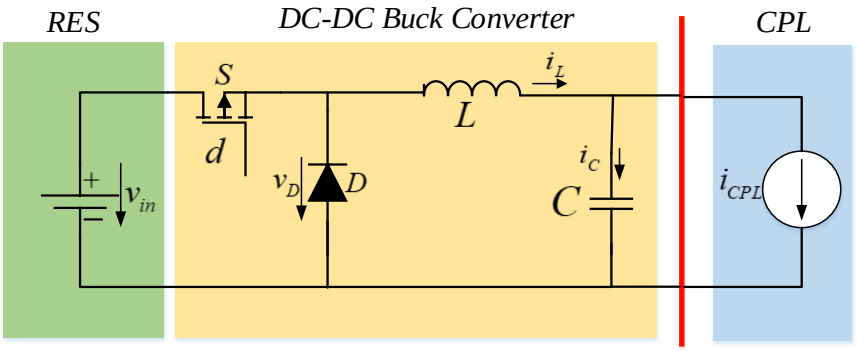


Fig. 3.4. A DC-DC buck converter equivalent circuit model providing a CPL

Fig. 3.4 depicts the equivalent model of the examined system, as depicted in Fig. 3.1, with the load DC-DC converter (CPL) represented by a controlled current source and the DC source representing the RES. Where v_{in} is the input voltage. *C* and *L* represent the DC-DC Buck converter's capacitor and inductor, respectively. *d* is the duty cycle value. i_L is the inductor current of the DC-DC buck converter. v_o denotes the output voltage of the buck converter.

While operating in continuous condition mode (CCM), the DC-DC Load converter (a Boost converter) can operate as a CPL if and only if its output voltage is closely regulated. The frequency of a CPL is less than the DC-DC Buck converter's voltage loop cut-off frequency, implying that the input impedance is equivalent to a negative resistance. The input impedance is equal to an inductance when the frequency outset the cut off frequency of the system [4-6], [45].

Across the controller bandwidth, the power consumed by a CPL stays unchanged, and its relationship is represented as

$$P_{CPL} = v \ .i = Cte \tag{3.4}$$

where

P_{CPL}: CPL power demanded

v: CPL's input voltage

i: CPL's consumed current

The equation for a CPL's incremental negative impedance is obtained by calculating its current in relation to its voltage and inverting the result, which expressed as:

$$\frac{dv}{di} = -\frac{v}{i} = -\frac{P_{CPL}}{i^2} = -\frac{v^2}{P_{CPL}} \tag{3.5}$$

resulting in

$$\frac{dv}{di} = -R_{CPL} < 0 \tag{3.6}$$

Equation (3.6) shows that CPLs induce the incremental negative resistance (INR), as shown in Fig. 3.5, which represents the CPL characteristic in the context of a *V-I* graph of the load converter. The CPL has a -180° phase on the Bode diagram because to its negative incremental resistance. As a result, if the source DC-DC converter's output impedance module crosses with the CPL's input impedance module when the source DC-DC converter's cut-off frequency is smaller than the CPL's, instability occurs. Furthermore, the INI characteristic (or called the incremental negative impedance (INI)) has an impact on system performances and the quality of the power. Thus, while CPL has a substantial influence on the stability of a DC-DC Buck converter, a tight load control may make a significant contribution if done correctly[4-6], [45].

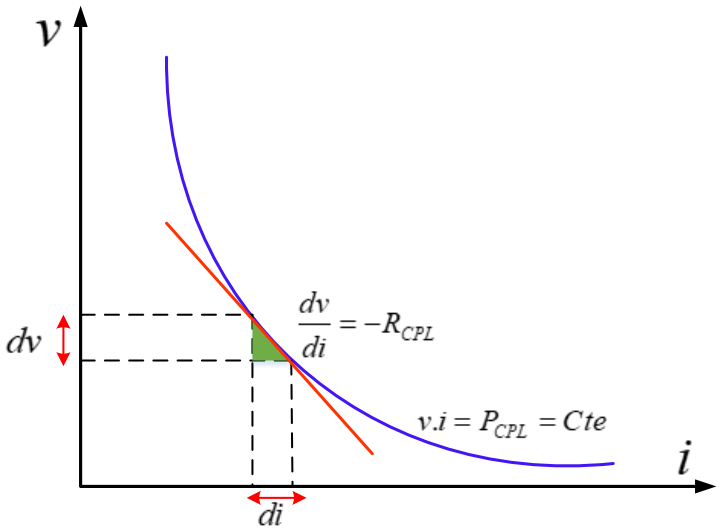


Fig. 3.5.Characteristic of constant power load (DC-DC load converter)

Figs. 3.6 and 3.7 illustrate the simulation of an open loop DC-DC Buck converter operating in CCM and feeding a load requesting a fixed voltage when the frequency is lower than the converter's voltage loop's cut-off frequency. The parameters utilized in this simulation's results are listed as follows: $v_{in} = 28V, C = 220uF, L = 2.7mH, P_{CPL} = 20W, d = 0.5$.

The open loop characteristic of a DC-DC Buck converter feeding a CPL causes significant changes in the output voltage and current, meaning that instability may arise, resulting in system damage (see Figs. 3.6 and 3.7).

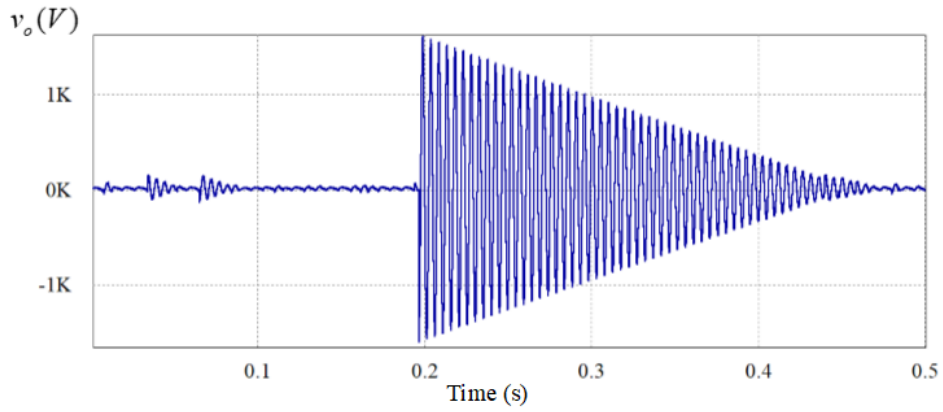


Fig. 3.6. The output voltage response of a DC Buck converter feeding a CPL

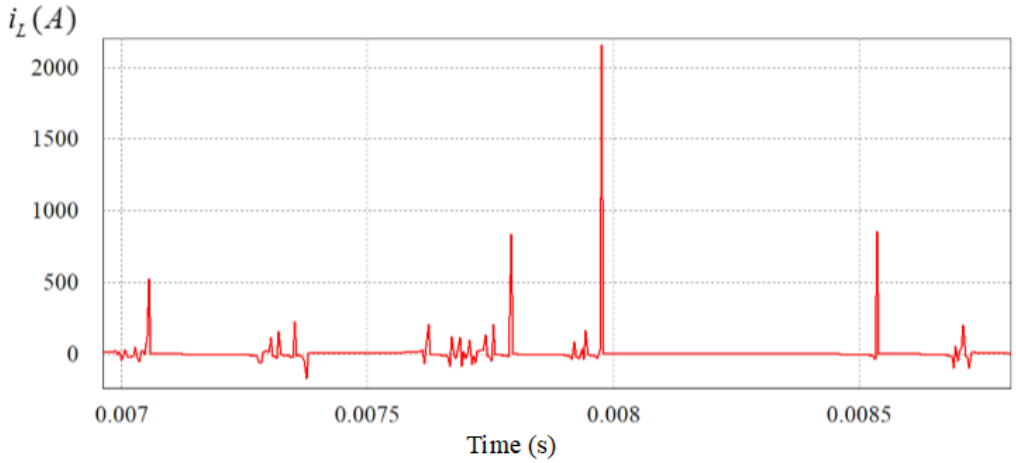
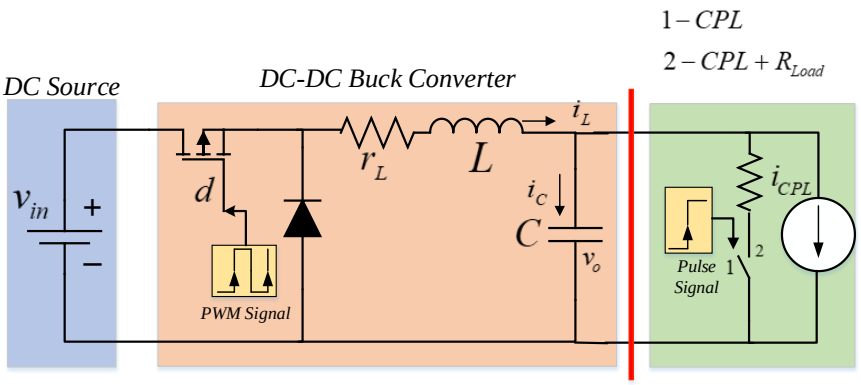


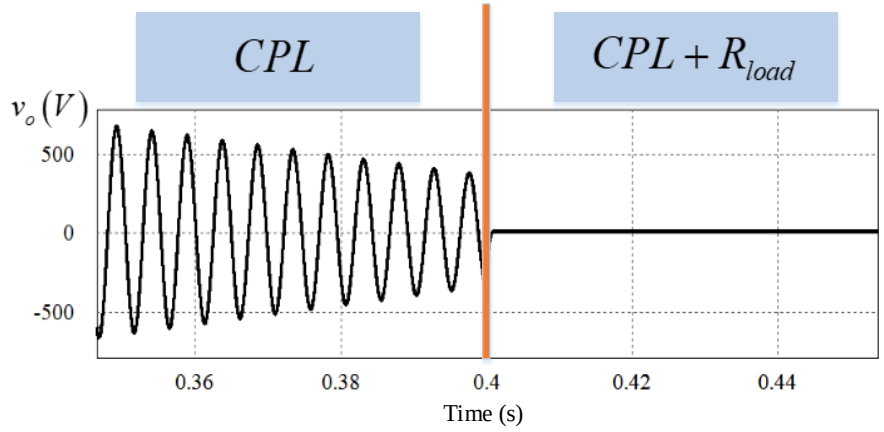
Fig. 3.7. The output current response of a DC Buck converter feeding a CPL

Many studies have offered various solutions to address the aforementioned difficulty, for example, introducing resistive loads in parallel to the CPL to reduce the INI feature, which means increasing the damping factor. Unfortunately, the main drawback of the proposed technique is lower power quality.

An open loop simulation result of a DC-DC Buck converter operating in CCM, whose feeds, in case 1: CPL and in case 2: (CPL + R), was used to study the impact of passive loads on the damping factor of the system. The behavior of a DC-DC Buck converter feeding a parallel resistive load and the CPL is seen in Fig. 3.8.



(a)



(b)

Fig. 3.8 .The effect of passive loads on the oscillations in output voltage generated by the CPL. (a)-a DC-DC buck converter feeding two types of loads, (1) with a CPL. (2) With (CPL+R), (b)-simulation result

To prevent the INI characteristic and enhance the damping factor without introducing a resistive load, a suitable technique is necessary. Furthermore, the proposed control must regulate the whole system verses the variations in input voltage and power demanded. A recommended solution, which is presented and detailed below, needs modeling the DC-DC buck converter feeding a voltage-regulated DC-DC boost converter to achieve this purpose (functioning as CPL).

3.3. Modeling of a DC-DC Buck converter feeding a CPL

This section considers the modeling of a DC-DC Buck converter with a CPL, as shown in Fig. 3.4. With CPL consideration, the DC-DC Buck converter operates with a switching period *T* and a duty cycle *d*.

When the switch is turned ON, $0 < t < dT$, during CCM operation, the state space equations are provided by:

$$\begin{cases} \dfrac{di_L}{dt} = \dfrac{1}{L}(v_{in} - v_o) \\ \dfrac{dv_o}{dt} = \dfrac{1}{C}(i_L - \dfrac{P}{v_o}) \end{cases} \tag{3.7}$$

And when the switch is turned OFF, $dT < t < T$, are represented as:

$$\begin{cases} \dfrac{di_L}{dt} = \dfrac{1}{L}(-v_o) \\ \dfrac{dv_o}{dt} = \dfrac{1}{C}(i_L - \dfrac{P}{v_o}) \end{cases} \tag{3.8}$$

These sets of equations may be shown using the state space averaging approach as follows:

$$\begin{cases} \dfrac{di_L}{dt} = \dfrac{1}{L}(dv_{in} - v_o) \\ \dfrac{dv_o}{dt} = \dfrac{1}{C}(i_L - \dfrac{P}{v_o}) \end{cases} \tag{3.9}$$

Equations (3.9) are nonlinear. Small perturbations in the state variables owing to small disturbances in the input voltage and duty cycle are considered for analyzing the small signal stability of the DC-DC Buck converter shown in Fig. 3.4. $\tilde{v}_{in}$ and $\tilde{d}$ are the small-signal variations of the inputs, $\tilde{v}_o$ and i_L are the small-signal variation of the state variables of small-signal model of the DC-DC Buck converter. The transfer functions and pole positions of this small-signal model can be used to assess its stability.

The transfer function of the output voltage with a small perturbation in inputs (v_{in}, d) may be described using the average small-signal technique as

$$\tilde{v}_o(s) = H_1(s).\tilde{d}(s) + H_2(s).\tilde{v}_{in}(s) \tag{3.10}$$

where

$$H_1(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{\dfrac{V_{in}}{LC}}{s^2 - \left(\dfrac{P}{CV_o^2}\right)s + \left(\dfrac{1}{LC}\right)} \tag{3.11}$$

and

$$H_2(s) = \frac{\tilde{v}_o(s)}{\tilde{v}_{in}(s)} = \frac{\frac{D}{LC}}{s^2 - \left(\frac{P}{CV_o^2}\right)s + \left(\frac{1}{LC}\right)} \tag{3.12}$$

According to (3.11) and (3.12), the poles of the transfer functions $H_1(s)$ and $H_2(s)$ have positive real parts. As a result of the influence of CPL, the system is unstable.

A transformation approach is used to reduce the number of sensors employed in the system under study. To do this, the output voltage and its derivative of the DC-DC Buck converter that feeds a CPL are chosen as the overall system's state variables as follows:

$$\begin{cases} x_1 = v_o \\ x_2 = \dfrac{dv_o}{dt} \end{cases} \tag{3.13}$$

By inserting the chosen state variables (3.13) in (3.9), one may construct the following new state-space model defining the analyzed system:

$$\begin{cases} \dot{x}_1 = x_2 \\ \dot{x}_2 = \dfrac{v_{in}}{CL}d - \dfrac{x_1}{CL} - \dfrac{Px_2}{Cx_1^2} \end{cases} \tag{3.14}$$

Where x_1 is the output voltage, and x_2 its derivative. C and L are the values of the DC-DC Buck converter's capacitor and inductance. v_{in} is the input voltage of the DC-DC Buck converter. P represents the constant power required by the DC-DC Buck converter.

In order to control the DC-DC Buck converter with a CPL, which is a nonlinear system, a nonlinear native control approach is required in this study. Let us first look at some suggested strategies for controlling the DC-DC Buck converter feeding a CPL.

3.4. Strategies for controlling a DC-DC Buck converter supplying a CPL

The majority of techniques for dealing with the CPL problem are based on nonlinear control [56-71]. The DC-DC Buck converter in our study must operate with abrupt changes in power demand and a varied range of input voltage. These disturbances will induce fluctuations in both the CPL and the duty cycle. As a result, linear controllers are inefficient, necessitating the usage of nonlinear controllers. The suggested control solutions, on the other hand, have either low

efficiency because of the additional passive elements or a large computational burden due to algorithm complexity. This section will go through two types of nonlinear controllers: sliding mode control (SMC) and Non-Singular Terminal Sliding Mode Control (NSTMC). The DC-DC buck converter control is accomplished in both cases under CPL and input voltage variations.

3.4.1 Sliding mode control for a DC-DC Buck converter feeding a CPL

The robustness of variable structure systems (VSS) to system parameter alterations and dynamic characteristics is well recognized [72-75], [82]. VSS are widely utilized in a variety of applications, including robotics, airplanes, DC and AC motors, power systems, and process control. The sliding mode control (SMC), which is meant to drive and restrict system states to reside within a neighborhood of the defined switching topologies that display desirable dynamics, is a particularly interesting feature of VSS. Furthermore, when SMC is used, the closed-loop response of the system studied becomes completely insensitive to both internal parameter uncertainty and external disturbances. The convergence of the system states to the equilibrium point is frequently asymptotical in conventional VSS due to the asymptotical convergence of the linear switching topologies that are typically used.

Several studies have employed a sliding mode controller (SMC) to alleviate the effect of INI generated by CPLs. The goal of this approach is to regulate the voltage or power of the Buck converter that provides a CPL by establishing a desire value and comparing it to the measured value of the DC-DC Buck converter. A suggested SMC offers a duty ratio that is utilized to create PWM generates signals for the Buck converter. Despite CPL fluctuations and high input voltage variation, this controller enhances the stability of the DC-DC Buck converter.

3.4.1.1 Mathematical Model of an SMC for a DC-DC Buck Converter feeding a CPL

According to the equivalent circuit model of the DC-DC buck converter supplying a CPL depicted in Fig. 3.4 and its built-in design (3.14), a SMC surface is given as.

The nonlinear surface of the SMC is then selected as follows:

$$S(x;t)=\left(\frac{d}{dt}+\lambda\right)^{n-1}\tilde{x} \tag{3.15}$$

where $\tilde{x}$ is the tracking error. The constant $\lambda>0$ uses to adjusting the convergence speed. *n*th-order S_function.

With *n=1* and according to (3.14) and (3.15), the surface function *S* may be expressed as

$$S = \dot{\tilde{x}} + \lambda \tilde{x} \tag{3.16}$$

where $\tilde{x}$ is defined as

$$\tilde{x} = x_1 - v_{ref} \tag{3.17}$$

and

$$\dot{\tilde{x}} = x_2 - \dot{v}_{ref} \tag{3.18}$$

By inserting (3.16) and (3.17) in (3.16), one may derive the surface function that characterizes the system as follows:

$$S = \left(x_2 - \dot{v}_{ref}\right) + \lambda\left(x_1 - \dot{v}_{ref}\right) \tag{3.19}$$

Switching control law is used to acquire the appropriate approach law *u(t)* of the SMC, which is defined as

$$u_{sw} = \dot{S} = -ksign(S) - QS = \begin{cases} \dot{S} > 0 \_ if \_ S < 0 \\ \dot{S} < 0 \_ if \_ S > 0 \end{cases} \tag{3.20}$$

Where *k* and *q* are both bigger than zero

To verify the presence of the sliding mode, a derivative of the function *S* is necessary to confirm the function stated in (3.20). Based on (3.19), the time derivative of S is given as

$$\dot{S} = (\dot{x}_2 - \ddot{v}_{ref}) + \lambda(\dot{x}_1 - \dot{v}_{ref}) \tag{3.21}$$

By using (3.14), x_1 and x_2 are obtained as

$$\dot{x}_1 = x_2 \tag{3.22}$$

and

$$\dot{x}_2 = \frac{v_{in}}{CL} d - \frac{x_1}{CL} - \frac{P_{CPL} x_2}{C x_1^2} - \ddot{v}_{ref} \tag{3.23}$$

By substituting (3.22) and (3.23) in (3.21), one may derive the derivative of *S* as

$$\dot{S} = \frac{v_{in}}{CL} d - \frac{x_1}{CL} - \frac{P_{CPL} x_2}{C x_1^2} - \ddot{v}_{ref} + \lambda x_2 - \lambda \dot{v}_{ref} \tag{3.24}$$

To ensure the convergence condition of the variable states to reach to required surface, a Lyapunov Function is defined as follows:

$$V(S)=\frac{1}{2}S^2 \tag{3.25}$$

As a result, the switching control (3.20) should ensure that the derivative of $V(S)$ when $S\neq 0$ remains smaller than zero, as shown below:

$$\dot{V}(S)=S.\dot{S}<0 \tag{3.26}$$

By employing (3.26), one may derive two conditions by substituting (3.20) in (3.24), emphasizing $S.\dot{S}<0$. The tow conditions are defined as:

1. If $S>0$ should be $\dot{S}<0$ .Then, the control law equal to 1,which can be written as:

$$\dot{S}=\frac{v_{in}}{CL}d-\frac{x_1}{CL}-\frac{P_{CPL}x_2}{Cx_1^2}-\ddot{v}_{ref}+\lambda x_2-\lambda\dot{v}_{ref}<0 \tag{3.27}$$

2. If $S<0$ should be $\dot{S}>0$ .Then, the control law equal to 0,which can be written as:

$$\dot{S}=\frac{v_{in}}{CL}d-\frac{x_1}{CL}-\frac{P_{CPL}x_2}{Cx_1^2}-\ddot{v}_{ref}+\lambda x_2-\lambda\dot{v}_{ref}>0 \tag{3.28}$$

3.4.1.2 Control Design and Stability Analysis of the proposed SMC

The control law *u* is divided into two parts: the first includes the equivalent control u_{eq} used to keep *s* equal to zero, and the second part includes the discontinuous control u_{sw}, which is defined as shown below.

$$u=u_{eq}+u_{sw} \tag{3.29}$$

The time derivative of (3.25) is given as:

$$\dot{V}=S.\dot{S}=S.\left(\frac{v_{in}}{CL}d-\frac{x_1}{CL}-\frac{P_{CPL}x_2}{Cx_1^2}-\ddot{v}_{ref}+\lambda x_2-\lambda\dot{v}_{ref}\right) \tag{3.30}$$

According to (44), ones can derive the control input *d* as follows:

$$d=\frac{CL}{v_{in}}\left(\frac{x_1}{CL}+\frac{P_{CPL}x_2}{Cx_1^2}+\ddot{v}_{ref}-\lambda x_2+\lambda\dot{v}_{ref}\right)+\frac{CL}{v_{in}}\left(ksign(S)+QS\right) \tag{3.31}$$

where

$$u_{eq} = \frac{CL}{v_{in}}\left(\frac{x_1}{CL} + \frac{P_{CPL}x_2}{Cx_1^2} + \ddot{v}_{ref} - \lambda x_2 + \lambda \dot{v}_{ref}\right) \tag{3.31-a}$$

and

$$u_{sw} = \frac{CL}{v_{in}}\left(ksign(S) + QS\right) \tag{3.31-b}$$

Substituting (3.31) into (3.30) yields:

$$\dot{V} = S.\dot{S} = -S(ksign(S) + QS) \tag{3.32}$$

resulting in

$$\dot{V} < -S(ksign(S) + QS) < 0 \tag{3.33}$$

As a result of the mathematical conclusions, the Lyapunov condition has been satisfied.

Fig. 3.9 depicts the phase portrait of the Buck converter feeding CPL with the suggested SMC based on the mathematical discussion offered in this section. In this dynamic analysis, we will determine the matching phase portrait for the overall system under the proposed controller and track the evolution of the system's state variables. As can be seen, the phase portrait is structurally stable, and the system behavior approaches the required equilibrium position with a brief restricted period of convergence and a reduced energy cost.

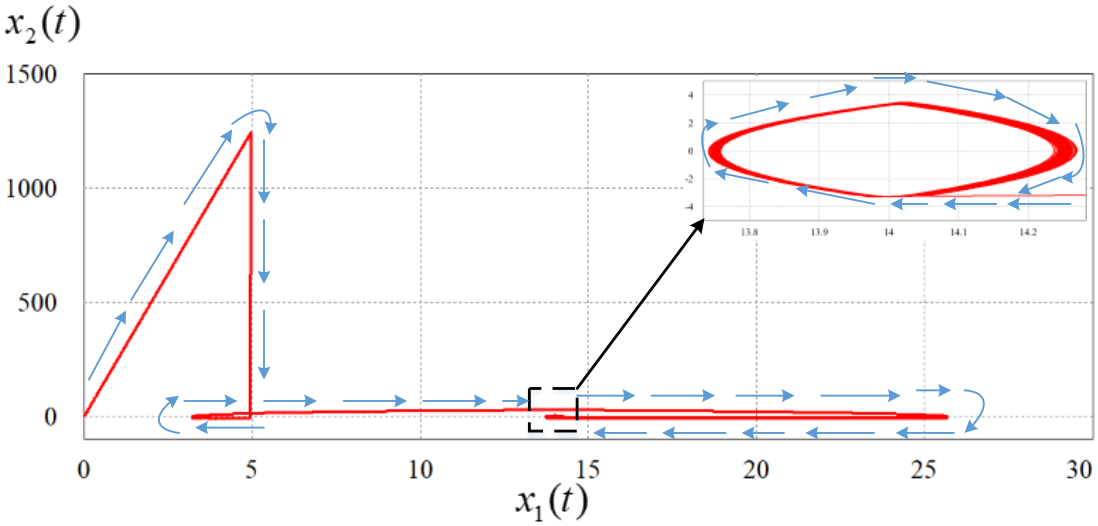


Fig. 3.9. Phase portrait of the DC-DC Buck converter feeding a CPL under the suggested SMC

3.4.1.3 Implementation of the Proposed SMC

Fig. 3.10 is a suggested SMC diagram configuration for a Buck converter supplying a CPL. One may implement the suggested SMC by utilizing (3.13), (3.14), and (3.19).

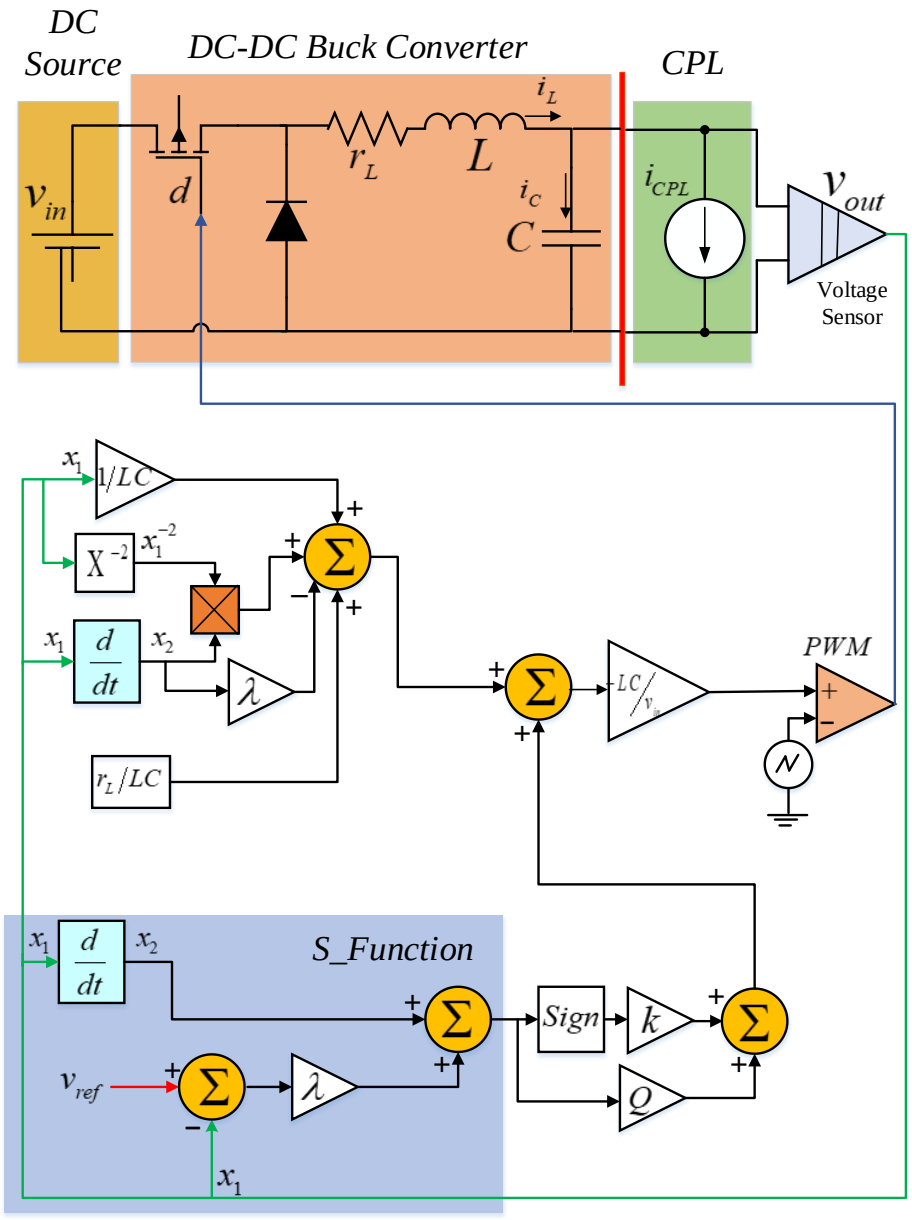


Fig. 3.10. Block diagram configuration of the proposed SMC for a DC-DC Buck converter supplying a CPL

3.4.1.4 Simulation study

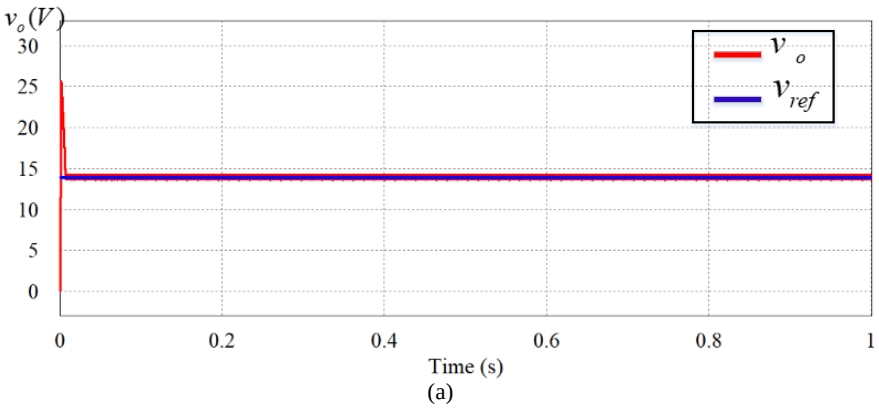
In order to verify the effectiveness of the proposed SMC against CPL effect and disturbances caused in input voltage and power load demanded, a simulation investigation was carried out using PSIM software, as shown in Fig. 3.15. The simulation includes a Buck converter that feeds

a tightly regulated DC-DC Boost converter that acts as a CPL. A DC-DC buck converter get their input voltage from a DC source, which may be viewed as a comparable representation of RES. Table 3.1 shows the parameters of the DC-DC Buck converter utilized in this simulation. The PSIM simulation results of a Buck converter feeding a tightly controlled Boost converter with the suggested SMC are shown in Fig. 3.11. In this simulation, the power load demand (CPL) is set at 10 W (Table. A2 in the Appendix section shows the control parameters).

Tab 3.1- DC-DC Buck converter parameters for the proposed SMC

Variables	Descriptions	Value
v_{in}	Input voltage	*28V*
v_o	Voltage Reference	*14V*
L	Nominal inductance	*2.7mH*
C	Nominal capacitance	$220\mu F$
f_{sw}	Switching frequency	*25KHz*
P_{CPL}	Power of CPL	*10W*
D	Duty cycle	*0.5*

Fig. 3.11 shows that the suggested SMC is successful in avoiding the influence of the CPL, which the output voltage approaches the reference value with a quick time response.



(a)

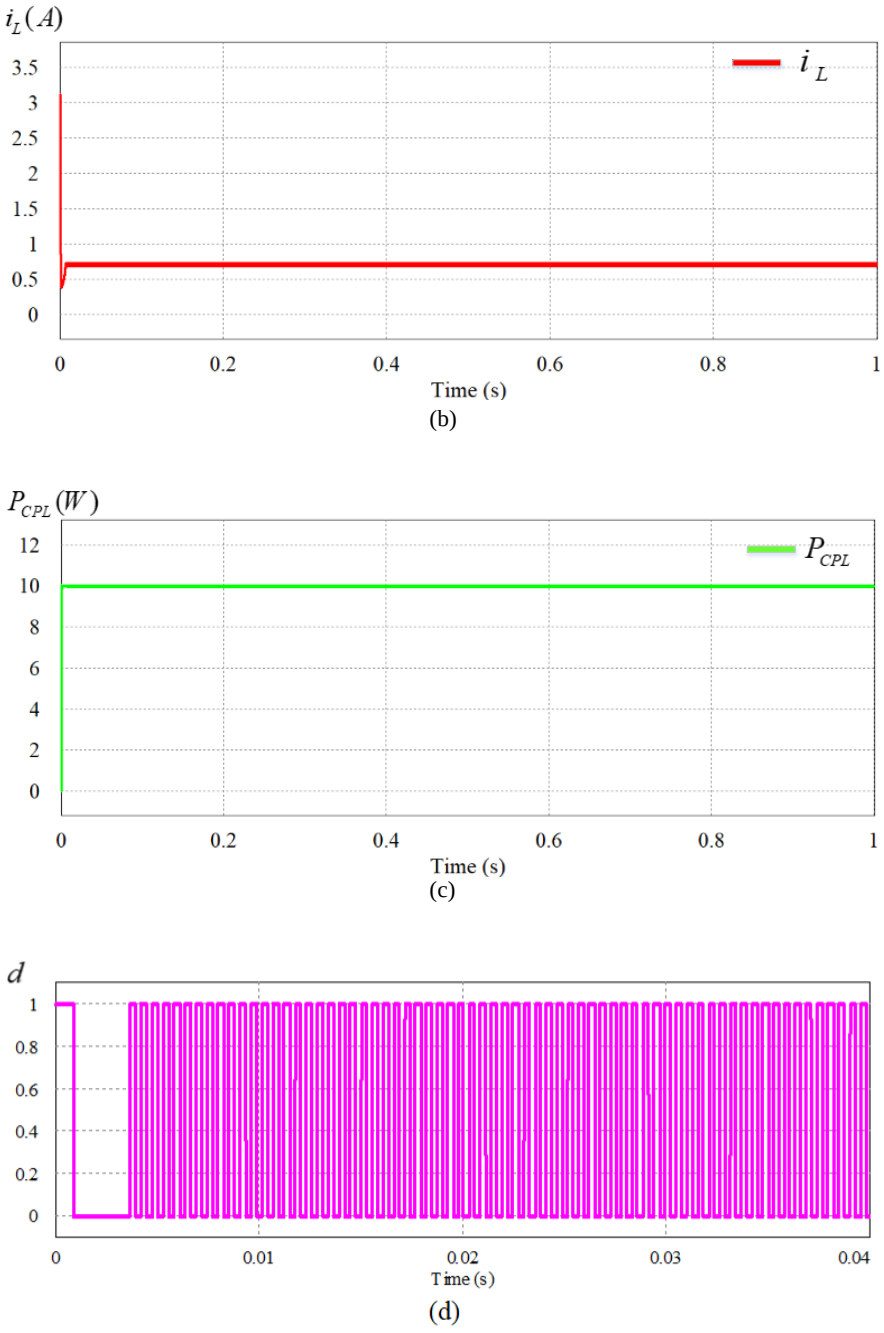


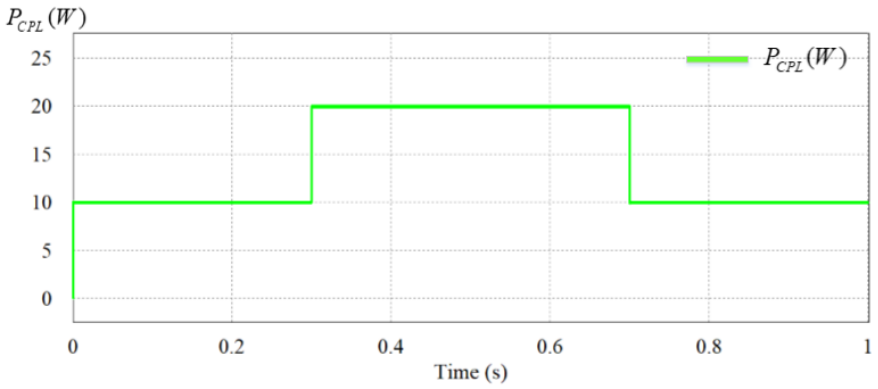
Fig. 3.11.The DC-DC Buck converter's dynamic behavior feeds a CPL through the proposed SMC. (a) Output voltage. (b) Output current. (c) CPL value. (d) Duty cycle

The simulation study includes two scenarios: CPL fluctuation and input voltage variation. The first scenario is used to evaluate the efficiency of the proposed SMC in preserving the stability of the DC-DC buck converter supplying the CPL. a regulated current source is used to simulate the CPL. As a result, it enables changing the power requested by the CPL of the DC-DC Buck converter, as shown in Fig. 3.12. This method allows testing the suggested SMC's capacity to maintain DC-DC buck converter stability at various levels of power and reduce disturbances

caused by fluctuations in load current. v_{in} is held at 28 V in this scenario, while the voltage reference v_{ref} is 14V.

The scenario of CPL experiment was carried out as: the system consumes 10w from 0s to 0.3s. We performed a sudden increase in power consumption by the DC-DC Buck converter of 20w from 0.3s to 0.7s. Then, as indicated in Fig. 3.12 a, we executed a sudden decrease of 10w (original value) in the time remaining.

Fig. 3.12 shows that the output voltage response approaches the appropriate reference with a shot settling time of 0.01s. According to the simulation results, the output voltage behavior remains stable, and no significant fluctuation is seen despite the scenario of the sequential variation in the power load demanded (CPL) of the DC-DC Buck converter. All variations in the CPL of the DC-DC Buck converter are rejected by the suggested SMC. The effect of consecutive CPL on the output voltage of the DC-DC Buck converter is minimal and ignored. The stability of a DC-DC Buck converter feeding a CPL has been demonstrated while taking these disturbances on the CPL into consideration.



(a)

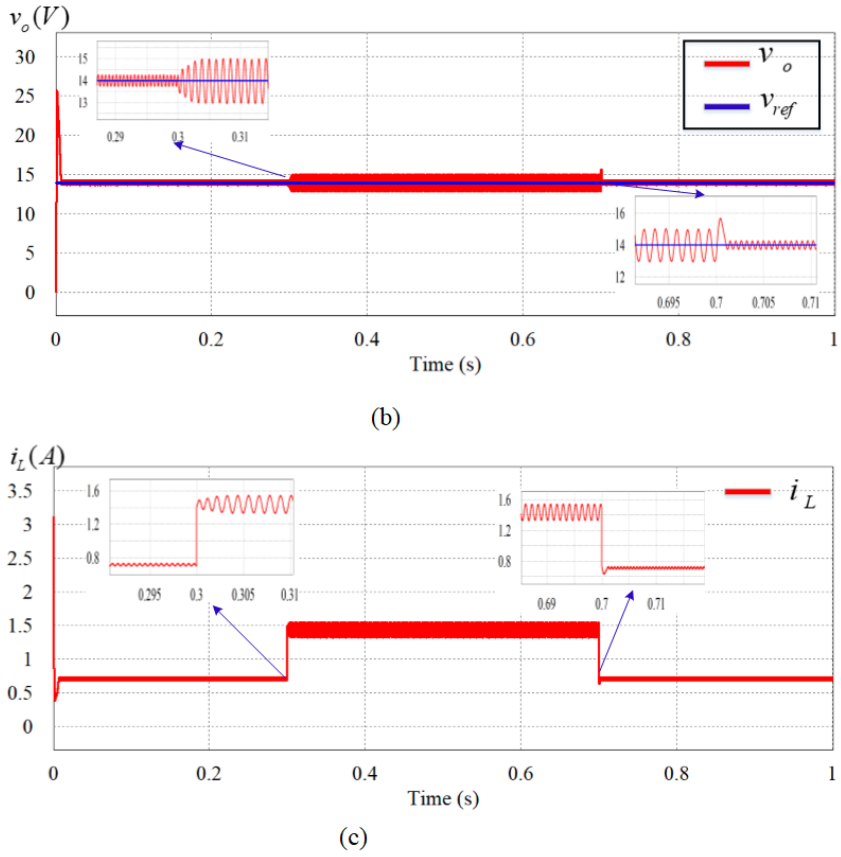


Fig. 3.12. A dynamic behavior of the DC-DC Buck converter feeding CPL resulted from the first scenario :(a) CPL value. (b) Output voltage. (c) Output current.

The second scenario is intended to evaluate the proposed SMC's robustness to sudden changes in the input voltage of the DC-DC Buck converter feeding a CPL. Indeed; the purpose of this scenario is to model the effect of RES fluctuation on the DC-DC Buck converter supplying a CPL, where the fluctuations are caused by natural element intermittency. This scenario is established as follows: As shown in Fig. 3.13 (a), the input voltage began with a 30% decrease and was then restored to the usual value 28V, which was done four times. The power load demand (CPL) in this scenario remains constant at 10W. Figs. 3.13 and 3.14 depict the behavior of a DC-DC Buck converter feeding a CPL in the presence of input voltage fluctuation.

One of the most important power quality challenges is input voltage fluctuation, which can damage electrical equipment and cause substantial systemic difficulties. Moreover, changes in input voltage reduce the electronic quality of the devices and create oscillations in internal voltages and currents.

According to Figs. 3.13 and 3.14, the disruption caused by the abrupt sequential fluctuation of v_{in} has no influence when the suggested SMC is used. As shown in Fig. 3.14, the abrupt variation

in input voltage creates a tiny divergence when the input voltage is reduced by 30% or recovered to its usual value. Depending on the simulation results, it is obvious that the values of output voltage and current remain constant, and no significant variation is observed despite fluctuations in input voltage (RES fluctuation). Thus, in this scenario, the suggested SMC can reduce the changes caused by the input voltage within a short time response.

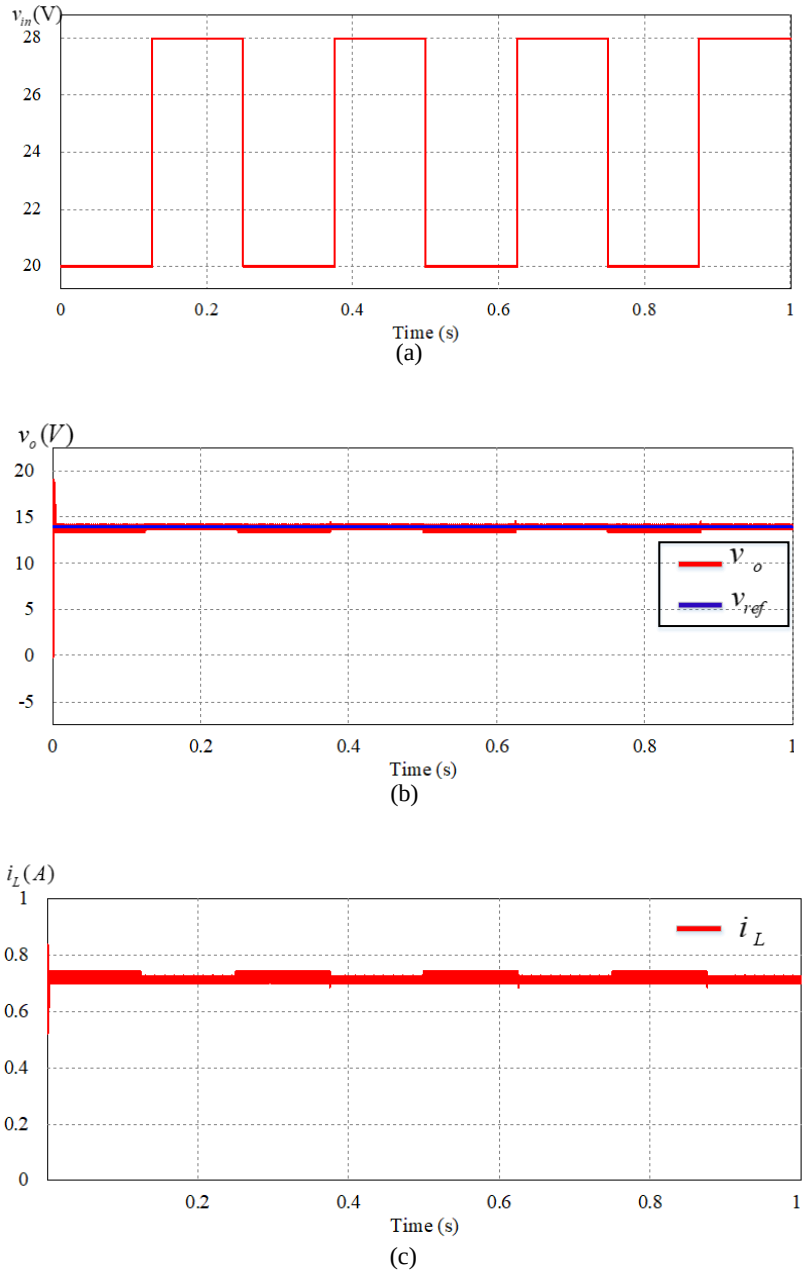


Fig. 3.13. The system behavior in the presence of an input voltage fluctuation scenario. (a) Scenario of input voltage fluctuation. (b) Output voltage. (c) Output current

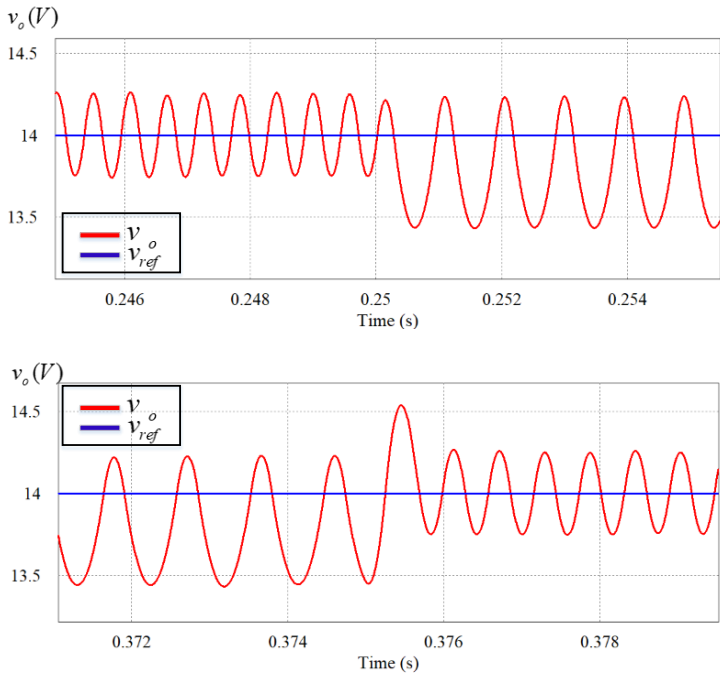


Fig. 3.14. Output voltage behavior in the second scenario: (a) decrease in input voltage (b) return to normal input voltage value

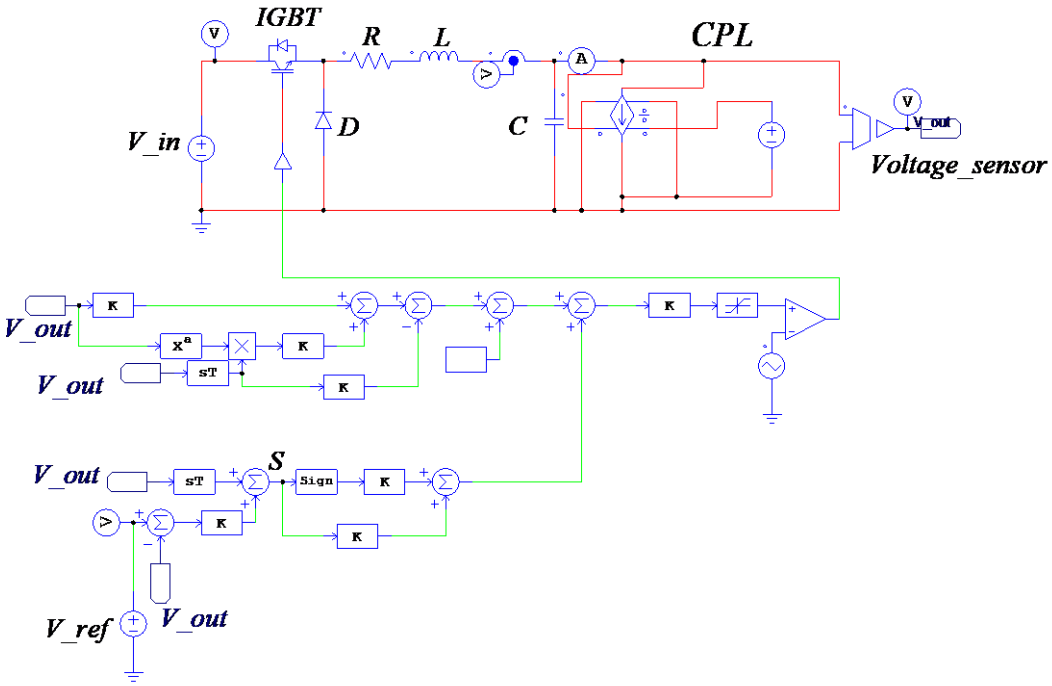


Fig. 3.15. PSIM software simulation of a DC-DC Buck converter using the recommended SMC

3.4.2 Nonsingular terminal sliding mode controller for a DC-DC Buck converter supplying a CPL

Terminal sliding mode controllers (TSMC) were designed to control industrial applications such as rigid manipulators and power electrical equipment [76-81]. When compared to linear hyperplane-based sliding modes, TSMC has various advantages, such as quick, finite-time convergence. Because it accelerates the rate of convergence at an equilibrium point desired, this controller is very suitable for high precision control. However, the present TSMC design methodologies continue to suffer from a singularity issue. The non-singular terminal sliding mode (NTSMC) is introduced in this section for a type of nonlinear dynamical systems with parameter uncertainty and external disturbances. To solve the singularity problem created by TSMC, a novel NTSMC manifold is presented. The suggested TSMC is used to regulate a Buck converter that feeds a DC-DC Boost converter with a tight voltage regulation (acting as a CPL). In addition, an overview of TSMC systems was provided.

A second-order uncertain nonlinear system is provided in order to express the TSMC, which is given as

$$\begin{aligned} \dot{x}_1 &= x_2 \\ \dot{x}_2 &= f(x) + b(x)u + g(x) \end{aligned} \tag{3.34}$$

Where $x = [x_1\ x_2]^T$ are the system states variables. The smooth nonlinear equations reliant on *x* are denoted by $f(x)$ and $b(x)\,.\,g(x)$ describes the total system's uncertainty, including disturbances, where $\|g(x)\| \le I_g$ and $I_g > 0$. u represents the examined system's control law..

The conventional TSM controller has a first-order sliding mode surface, written as

$$s_1 = x_2 + \beta x_1^{\frac{q}{p}} \tag{3.35}$$

In this equation, $\beta > 0$ is a constant. *p* and *q* are odd numbers greater than zero that solve the following equation:

$$p > q \tag{3.36}$$

The time derivative of (3.35) is calculated as follows:

$$\dot{s}_1 = f(x) + b(x)u + g(x) + \beta \frac{q}{p} x_2\ x_1^{\frac{q}{p}-1} \tag{3.37}$$

Let define the following Lyapunov function as follows:

$$V_1 = \frac{1}{2} s_1^2 \tag{3.38}$$

The time derivative of (3.38) is given by:

$$\dot{V}_1 = s_1 \dot{s}_1 \tag{3.39}$$

According to (3.37) and (3.39), one can obtain the control law *u* as follows:

$$u = -b^{-1}(x)\left[f(x) + \beta \frac{q}{p} x_1^{\frac{q}{p}-1} x_2 + I_g + \eta \,\mathrm{sgn}(s_1) \right] \tag{3.40}$$

Where $\eta > 0$ denotes a design constant.

When $s_1(0) \neq 0$, the dynamic system states obviously track the sliding mode surface at $s_1 = 0$ for a limited and calculable time t_r, which is met by the following condition.

$$t_r \leq \frac{|s_1(0)|}{\eta} \tag{3.41}$$

In addition, when the sliding mode approaches $s_1 = 0$, the dynamic design is determined by solving the nonlinear differential equation:

$$x_2 + \beta x_1^{\frac{q}{p}} = \dot{x}_1 + \beta x_1^{\frac{q}{p}} = 0 \tag{3.42}$$

Where x_1 is the system's terminal attractor of equation (3.42).

The time necessary to go from $x_1(t_r) \neq 0$ to $x_1(t_s + t_r) = 0$ can be given as

$$t_s = \frac{p}{\beta(p-q)} \left| x_1(t_r) \right|^{1-\frac{q}{p}} \tag{3.43}$$

According to (3.43), the state variables (x_1, x_2) that describe the TSM manifold (3.42) converge to zero after a certain amount of time.

According to (3.40), if $x_2 \neq 0$ while $x_1 = 0$, the second section involving $x_1^{\frac{q}{p}-1} x_2$ may result in a singularity problem.

Proof:

When $s_1 = 0$, one can obtain the following equation, written as

$$x_2 = -\beta x_1^{\frac{q}{p}} \tag{3.44}$$

By substituting (3.44) into (3.40), the control law *u* may be rewritten as follows:

$$u = -b^{-1}(x)\left[f(x) - \beta^2 \frac{q}{p} x_1^{(2q-p/p)} + I_g + \eta \,\mathrm{sgn}(s_1) \right] \tag{3.45}$$

Therefore hence as long as $q < p < 2q$, i.e. $1 < \frac{p}{q} < 2$, the term $x_1^{\frac{q}{p}-1} x_2$ completely equal to $x_1^{(2q-p/p)}$, which implies that is nonsingular, this scenario does not arise in the ideal sliding mode.

When there is inadequate control to guarantee that $x_2 \neq 0$ while $x_1 = 0$, the singularity problem can appear during the reaching phase.

For the case of $x_2 \neq 0$ when $x_1 = 0$ before the system states reach $s_1 = 0$, the TSM controller (3.40) cannot guarantee a limited control signal. Besides that, even after the sliding mode $s_1 = 0$ has arrived, the singularity problem may arise, due to the system states cannot be assured to always continue to stay in the sliding mode, including around the equilibrium position $(x_1 = 0, x_2 = 0)$, as well as the situation of $(x_2 \neq 0, x_1 = 0)$ can arise at any time because of the calculation faults and unpredictable conditions. This underscores the need of addressing the singularity problem produced by traditional TSM systems.

Several solutions have been developed to solve the singularity problem in traditional TSM systems. One method is to alternate between TSM and linear hyperplane-based sliding modes. Another technique is to move the trajectory to a pre-specified open zone where TSM control is not singular. In order to avoid the singularity, these strategies take indirect approaches. This section proposes a Nonsingular terminal sliding mode controller (NTSMC) for a Buck converter feeding a tightly voltage-controlled DC-DC Boost converter that can totally avoid the singularity problem. With the presence of external disturbances, the suggested controller avoid the CPL effect and the singularity problem. This approach has achieved asymptotic stability with less steady-state error, faster finite-time convergence, and a low control energy cost.

The suggested surface for describing the NTSM model is given as:

$$s_2 = x_1 + \frac{1}{\beta} x_2^{\,p/q} \tag{3.46}$$

where β , p and q are discussed in (3.35).

When $s_2 = 0$, the surface equation of NTSM (3.46) is easily observed to be identical to (3.35), implying that the period necessary to achieve the balancing point $x_1 = 0$ in the sliding mode is the same as in (3.43). It is vital to notice that the derivative of s_2 with respect to time does not create negative fractional terms when (3.46) is used. The following theorem expands on the NTSM control.

Theorem. Based on (3.34) and the NTSM surface equation (3.46), the following control law may be obtained:

$$u = -b^{-1}(x)\left\{ f(x) + \beta \frac{q}{p} x_2^{\,2-p/q} + I_g + \eta \,\mathrm{sgn}(s_2) \right\} \tag{3.47}$$

Where $1 < p/q < 2, \eta < 0$.

As a result, the NTSM surface equation (3.46) will approach a limited duration. Moreover, x_1 and x_2 will ultimately reach zero.

Proof. The derivative of s_2 with respect to time t may be calculated using (3.34), as follows:

$$\dot{s}_2 = x_2 + \frac{1}{\beta}\frac{p}{q} x_2^{\,p/q-1}\left(f(x) + g(x) + b(x)u \right) \tag{3.48}$$

The candidate Lyapunov function is defined as follows:

$$V_2 = \frac{1}{2} s_2^{\,2} \tag{3.49}$$

In terms of time, the derivative of (3.49) is given as:

$$\dot{V}_2 = s_2 \dot{s}_2 \tag{3.50}$$

Resulting in

$$\dot{V}_2 = s_2 \left(x_2 + \frac{1}{\beta}\frac{p}{q} x_2^{\,p/q-1}\left(f(x) + g(x) + b(x)u \right) \right) \tag{3.51}$$

The control law u (3.47) given above is constructed using (3.51) and (3.48).

By substituting (3.47) into (3.51), one can obtain the following equation:

$$\dot{V}_2 = s_2\dot{s}_2 = s_2\left(-\frac{1}{\beta}\frac{p}{q}x_2^{\,p/q-1}\eta\,\mathrm{sgn}(s_2)\right) \tag{3.52}$$

resulting in

$$\dot{V}_2 < 0 \tag{3.53}$$

Since p and q signify odd number integers greater than zero, and $1 < p/q < 2$, and we have $x_2^{\,p/q-1} > 0$. Thus, let us assume that $\rho(x_2) = (1/\beta)(p/q)\eta x_2^{\,p/q-1}$.

Also there's $\dot{V}_2 \le -\rho(x_2)\mathrm{sgn}(s_2)$ for $x_2 \neq 0$ and $\rho(x_2) > 0$

As a result, when $x_2 \neq 0$, the Lyapunov stability condition is achieved. A system states can link the sliding mode $s_2 = 0$ in a finite amount of time. This may be simply proven by citing the following arguments: The consequence of substituting the control law (3.47) for the system dynamic (3.35).

$$\dot{x}_2 = -\beta\frac{q}{p}x_2^{\,2-p/q} - \eta\,\mathrm{sgn}(s_2) \tag{3.54}$$

For $x_2 = 0$, (3.54), it is as follows:

$$\dot{x}_2 = -\eta\,\mathrm{sgn}(s_2) \tag{3.55}$$

In the case of two conditions, $s_2 > 0$ and $s_2 < 0$, $\dot{x}_2 \le -\eta$ and $\dot{x}_2 \ge -\eta$, are achieved, which indicating that $x_2 = 0$ it is not a source of attraction. In addition implies that there is a region near $x_2 = 0$ such that $\delta > 0$, where $|x_2| < \delta$, there seem to be $\dot{x}_2 \le -\eta$ during $s_2 > 0$ and $\dot{x}_2 \ge \eta$ during $s_2 < 0$, respectively. As a result, the passage of the trajectory of the proximity's end from $x_2 = \delta$ to $x_2 = -\delta$ during $s_2 > 0$, and from $x_2 = -\delta$ to $x_2 = \delta$ during $s_2 < 0$ arises in a short period of time. Furthermore, to different areas wherever $|x_2| > \delta$, that can be surely concluded from (3.54) that the switching surface $s_2 = 0$ can be achieved transformed within a finite period of time because we have $\dot{x}_2 \le -\eta$ during $s_2 > 0$ and $\dot{x}_2 \ge -\eta$ during $s_2 < 0$. Fig. 3.16 depicts the system's phase plane plot. As a result, even under the most severe disturbances, the sliding mode $s_2 = 0$ can be achieved in finite period of time from anywhere in the phase plane. Based on what has been

explained, we can confidently conclude that NTSM (3.46) is similar to TSM (3.35), which means that the time required to transfer into the balance position $x_1 = 0$ is the same in (3.43).

Therefore, the NTSM manifold (3.46) can be transferred in a limited time, implying that the system states will transfer into zero in a limited time.

Remark 1. It is possible to observe non-singular phenomena within the state space in NTSM Controller.

Remark 2. To reduce chattering, the function "sat" can be used to replace the "sgn" equation.

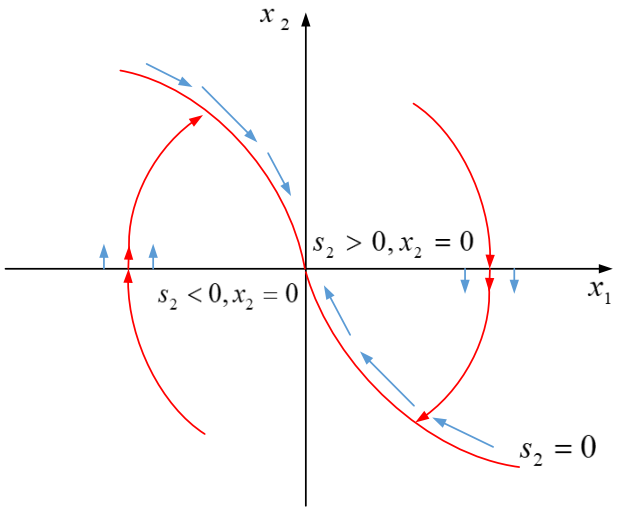


Fig. 3.16. The phase plot of the system with NTSM controller

3.4.2.1 Mathematical Model of a NTSM controller For a DC-DC Buck Converter supplying a CPL

The first step in developing the NTSM controller for a DC-DC buck converter feeding a CPL is to create a stable surface. This surface is based on the equivalent of the DC-DC buck converter illustrated in Fig. 3.4 and its design model (3.14).

Assuming that the desired reference of the Buck converter output voltage supplying a CPL is x_{1r}, the tracking error of the output voltage and its derivative is stated as follows: $e = x_1 - x_{1r}, \dot{e} = x_2 - \dot{x}_{1r}$.

Thus, the NTSM controller's non-linear surface is chosen as follows:

$$s_3 = e + \frac{1}{\beta}\dot{e}^{\frac{p}{q}} = \left(x_1 - x_{1r}\right) + \frac{1}{\beta}\left(x_2 - \dot{x}_{1r}\right)^{\frac{p}{q}} \tag{3.56}$$

Where $\beta > 0$, p and q signify odd number integers greater than zero that perform the subsequent conditions: $p = 2m+1, m = 1,2,.....$, and it must be $1 < p/q < 2$.

Assume that the time between $s_3(0) \neq 0$ and $s_3 = 0$ is t_r, and that the period between t_r and when the tracking error is zero is t_s.As a result, when the system approaches it, there is a sliding surface, which is expressed as

$$s_3 = e + \frac{1}{\beta}\dot{e}^{\frac{p}{q}} = 0 \tag{3.57}$$

Converting (3.57) may find the equation described above as follows:

$$\dot{e} = -\beta^{\frac{q}{p}} e^{\frac{q}{p}} \tag{3.58}$$

Then, by solving the differential equation (3.58), one can obtain ts as follows:

$$t_s = \frac{p}{\beta^{\frac{q}{p}}\left(p-q\right)}\left|e(t_r)\right|^{1-\frac{q}{p}} \tag{3.59}$$

By adjusting β, p, and q, the system can reach steady state in t_s.

The switching control law of SMC is defined in order to acquire the requisite control law *u(t)* of the NTSM controller, written as

$$u_{sw} = -Qs_3 - ksign(s_3) = \begin{cases} \dot{s}_3 > 0\_if\_s_3 < 0 \\ \dot{s}_3 < 0\_if\_s_3 > 0 \end{cases} \tag{3.60}$$

To verify the presence of the sliding mode, a derivative of the function s_3 is necessary to validate the function stated in (3.60). The time derivative of s_3 is determined as follows according to (3.56), written as

$$\dot{s}_3 = \dot{e} + \frac{p}{\beta q}\dot{e}^{\frac{p}{q}-1}\left(\ddot{e}\right) \tag{3.61}$$

resulting in

$$\dot{s}_3 = \left(\dot{x}_1 - \dot{x}_{1r}\right) + \frac{p}{\beta q}\left(\dot{x}_1 - \dot{x}_{1r}\right)^{\frac{p}{q}-1}\left(\ddot{x}_1 - \ddot{x}_{1r}\right) \tag{3.62}$$

The primary and secondary time derivative tracking errors for the output voltage of the DC-DC Buck converter feeding a CPL may be obtained using the dynamic design in (3.14), which are defined as

$$\dot{e} = \dot{v}_o - \dot{x}_{1r} \tag{3.63}$$

and

$$\ddot{e} = \frac{v_{in}}{CL}d - \frac{x_1}{CL} - \frac{Px_2}{Cx_1^2} - \ddot{x}_{1r} \tag{3.64}$$

The derivative of s_3 can be obtained by combining (3.63) and (3.64) in (3.62), written as follows:

$$\dot{s}_3 = \left(\dot{x}_1 - \dot{x}_{1r}\right) + \frac{p}{\beta q}\left(\dot{x}_1 - \dot{x}_{1r}\right)^{\frac{p}{q}-1}\left(\frac{v_{in}}{CL}d - \frac{x_1}{CL} - \frac{Px_2}{Cx_1^2} - \ddot{x}_{1r}\right) \tag{3.65}$$

To guarantee the stability analysis and convergence condition of the reaches of phase space trajectory into the desired sliding surface, a Lyapunov Function is defined as:

$$V_3 = \frac{1}{2}s_3^{\,2} \tag{3.66}$$

The switching control (3.60) should therefore ensure that the derivative of $V_3\left(s_3\right)$ while $s_3 \neq 0$ remains less than zero, as follows:

$$\dot{V}_3(s_3) = s_3\dot{s}_3 < 0 \tag{3.67}$$

Therefore, two conditions are obtained by substituting (3.60) in (3.65), highlighting $s_3\dot{s}_3 < 0$

1) If $s_3 > 0$, must be $\dot{s}_3$ is smaller than 0,which yields:

$$\dot{s}_3 = \left(\dot{x}_1 - \dot{x}_{1r}\right) + \frac{p}{\beta q}\left(\dot{x}_1 - \dot{x}_{1r}\right)^{\frac{p}{q}-1}\left(\frac{v_{in}}{CL}d - \frac{x_1}{CL} - \frac{Px_2}{Cx_1^2} - \ddot{x}_{1r}\right) < 0 \tag{3.68}$$

2) If $s_3 > 0$, must be $\dot{s}_3$ is greater than 0,which yields:

$$\dot{s}_3 = \left(\dot{x}_1 - \dot{x}_{1r}\right) + \frac{p}{\beta q}\left(\dot{x}_1 - \dot{x}_{1r}\right)^{\frac{p}{q}-1}\left(\frac{v_{in}}{CL}d - \frac{x_1}{CL} - \frac{Px_2}{Cx_1^2} - \ddot{x}_{1r}\right) > 0 \tag{3.69}$$

3.4.2.2 Control Design and Stability Analysis of TSM controller

The control law $u(t)$ includes two parts: the primary term $u_{eq}(t)$ reflects the equivalent control to maintain $\dot{s}_3 = 0$, and the second portion $u_{sw}(t)$ represents the discontinuous control, written as

$$u = u_{eq} + u_{sw} \tag{3.70}$$

The time derivative of (3.67) is given as:

$$\dot{V}_3 = s_3\dot{s}_3 = s_3\left[\left(\dot{x}_1 - \dot{x}_{1r}\right) + \frac{p}{\beta q}\left(\dot{x}_1 - \dot{x}_{1r}\right)^{\frac{p}{q}-1}\left(\frac{v_{in}}{CL}d - \frac{x_1}{CL} - \frac{Px_2}{Cx_1^2} - \ddot{x}_{1r}\right)\right] \tag{3.71}$$

According to (3.71), one can derive the control input d characterized NTSM controller that applied for a DC-DC Buck converter feeding a CPL, designed as

$$d = -\frac{LC}{v_{in}}\left(-\frac{x_1}{CL} - \frac{Px_2}{Cx_1^2} - \ddot{x}_{1r} + \beta\frac{p}{q}\left(x_2 - \dot{x}_{1r}\right)^{2-\frac{p}{q}} + ksign(s_3) + Qs_3\right) \tag{3.72}$$

where

$$u_{eq} = -\frac{LC}{v_{in}}\left(-\frac{x_1}{CL} - \frac{Px_2}{Cx_1^2} - \ddot{x}_{1r} + \beta\frac{p}{q}\left(x_2 - \dot{x}_{1r}\right)^{2-\frac{p}{q}}\right) \tag{3.72-a}$$

and

$$u_{sw} = -\frac{LC}{v_{in}}(ksign(s_3) + Qs_3) \tag{3.73-b}$$

Substituting (3.72) into (3.71) yields:

$$\dot{V}_3 = s_3\dot{s}_3 = -s_3\left(\frac{p}{\beta q}\left(x_2 - \dot{x}_{1r}\right)^{\frac{p}{q}-1}\left(Qs_3 + ksign(s_3)\right)\right) \tag{3.73}$$

because

$$1 < \frac{p}{q} < 2 \tag{3.74}$$

so

$$0 < \frac{p}{q} - 1 < 1 \tag{3.75}$$

When $\left(x_2 - \dot{x}_{1r}\right) \neq 0$, and x_{1r} is defined as a constant, p and q denote odd number integers greater than zero, indicating that

$$\left(x_2 - \dot{x}_{1r}\right)^{\frac{p}{q}-1} > 0 \tag{3.76}$$

This means

$$\dot{V}_3 < -s_3\left(\frac{p}{\beta q}\left(x_2 - \dot{x}_{1r}\right)^{\frac{p}{q}-1}\left(Qs_3 + ksign(s_3)\right)\right) \tag{3.77}$$

By simplifying (3.77), yields

$$\dot{V}_3 \le -s_3\left[\varepsilon\left(Qs_3 + ksign\left(s_3\right)\right)\right] < 0 \tag{3.78}$$

Where

$$\varepsilon = \frac{p}{\beta q}\left(x_2 - \dot{x}_{1r}\right)^{\frac{p}{q}-1} > 0 \tag{3.79}$$

As a result of the mathematical conclusions, the Lyapunov condition has been achieved.

Fig. 3.17 depicts the asymptotic stability of a DC-DC Buck converter feeding a CPL loaded by the recommended NTSM controller. Based on our findings, we can infer that the system behavior achieves the ideal equilibrium position with a quick settling time, a brief restricted period of convergence, and a low control energy cost.

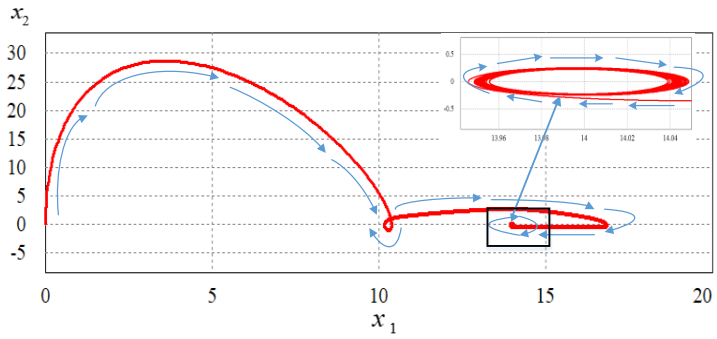


Fig. 3.17. The phase plot of a DC-DC Buck converter feeding a CPL controlled by an NTSM

3.4.2.3 Implementation of the Proposed NTSM controller

PSIM software is used to implement the suggested robust nonsingular terminal sliding mode controller (NTSMC). The proposed NTSM controller for a DC-DC Buck converter feeding a tightly voltage regulated DC-DC Boost converter (functioning as a CPL) may be reduced by a block diagram using the transformation approach indicated in equations (3.13) and (3.14), as illustrated in Fig. 3.18.

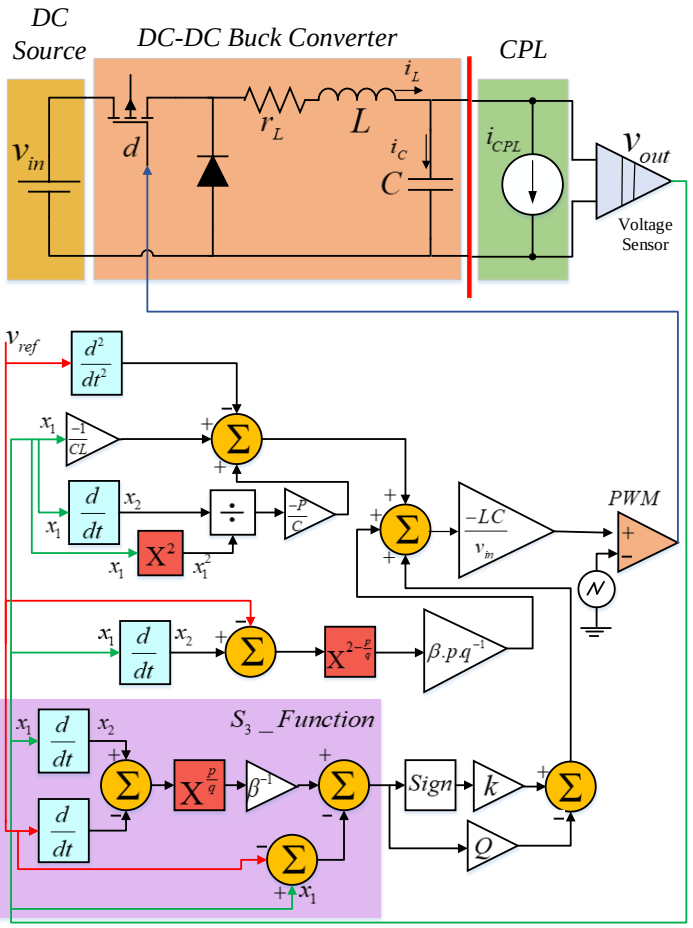


Fig. 3.18. NTSM controller block diagram configuration for a DC-DC Buck converter supplying a CPL

The design process of the robust NTSM controller used for a DC-DC Buck converter feeding a CPL can be characterized as follows (see Fig. 3.19):

- Step 1: Providing the studied system's state variables v_o, i_L
- Step 2: Selecting new state variables x_1, x_2
- Step 3: Performing the new model design by using (x_1, x_2)
- Step 4: Constructing NTSM control with the new model design
- Step 5: Satisfying the Lyapunov condition in order to ensure stability

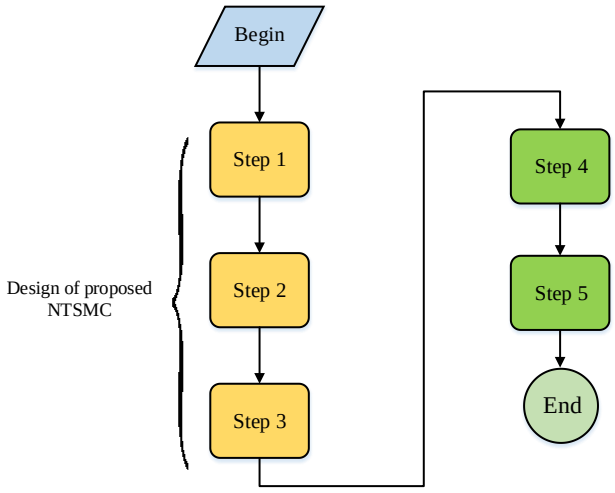


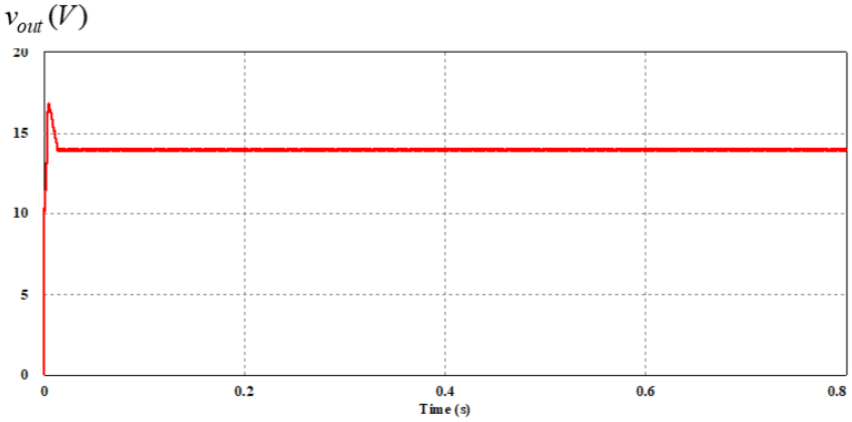
Fig. 3.19. NTSM controller flowchart

3.4.2.4 Simulation results

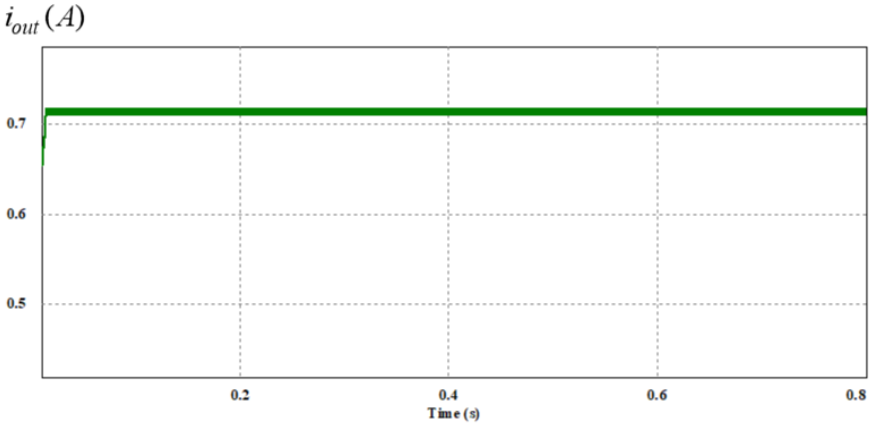
External disturbances in input voltage and power load demanded (CPL) are utilized to test the efficacy of the proposed NTSM controller applied to a DC-DC Buck converter feeding a CPL. Furthermore, the singularity problem associated with traditional TSM control is eliminated. A DC-DC Buck converter feeds a closely regulated DC-DC boost converter that works as a CPL in the simulation. The DC-DC buck converter gets its input voltage from a DC source, which may be seen of as a similar depiction of RES. PSIM software was used to do this simulation, as indicated in Fig. 3.23. Table 3.2 summarizes the general parameters utilized in this simulation. We conducted two scenarios that were properly employed for this goal in order to verify the ability to deal with abrupt disturbances.1) - To test the efficacy and resilience of the recommended controller, a sudden change in the power utilized by the CPL has been performed. 2) - A perturbation was performed against the input voltage of the DC-DC buck converter feeding a CPL. Fig. 3.20 illustrates that the proposed NTSM controller, when applied to a DC-DC buck converter powering a CPL, was effective in avoiding the detrimental effects of the CPL as well as the singularity problem generated by TSM systems. With a rapid time response and a low control energy cost, the output voltage provided by the suggested controller approaches the intended reference voltage value of the DC-DC Buck converter (The control parameters utilized in this simulation are listed in Table. A2 in the Appendix).

Tab 3.2- DC-DC Buck converter parameters values with the introduced NTSM controller

Variables	*Descriptions*	*Value*
v_{in}	Input voltage	*28V*
v_o	Voltage Reference	*14V*
L	Nominal inductance	*6mH*
C	Nominal capacitance	$470\mu F$
f_{sw}	Switching frequency	*25KHz*
P_{CPL}	Power of CPL	*10W*
D	Duty cycle	*0.5*



(a)



(b)

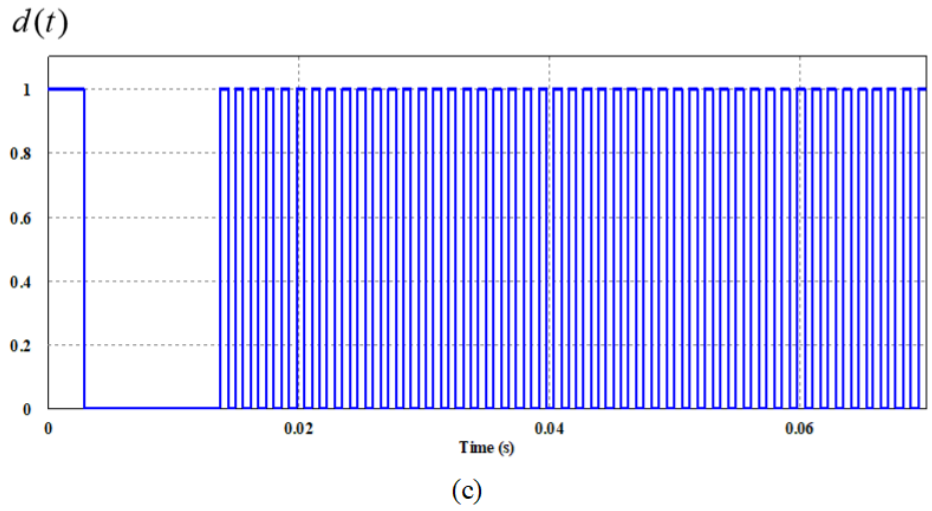
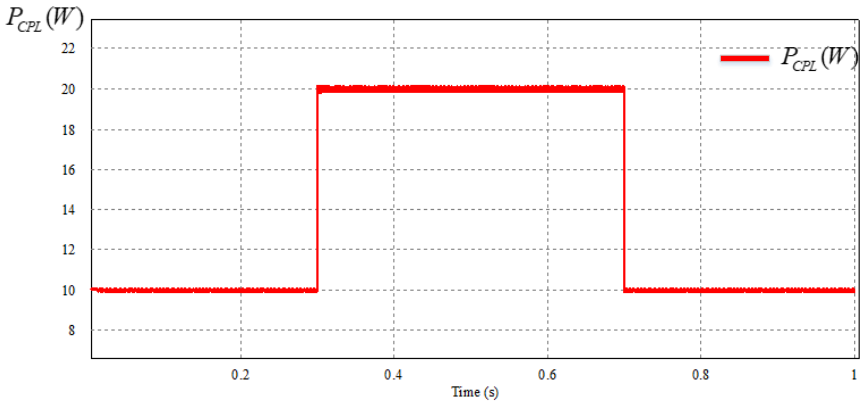


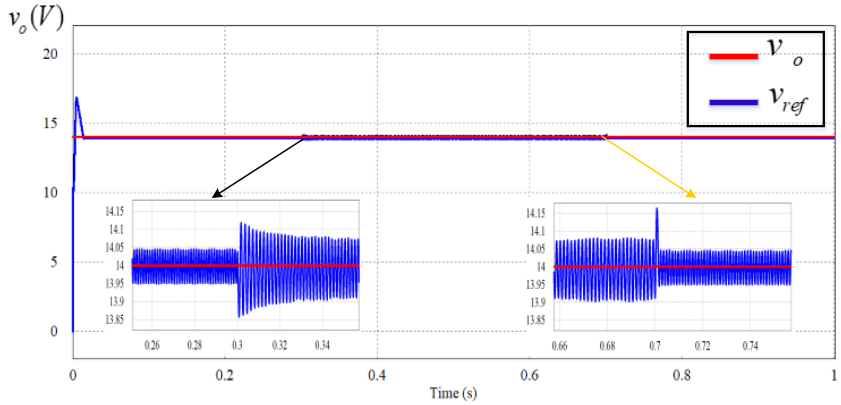
Fig. 3.20. The dynamic behavior of the DC-DC Buck converter feeds a CPL via the suggested NTSM controller. (a) Voltage. (b) Current. (c) Duty cycle

External fluctuations were performed at the power load demanded of the CPL of the DC-DC Buck converter to assess the efficacy of the proposed NTSM controller. The CPL experiment was carried out as follows: the total system utilizes 10w from 0s to 0.3s. We performed a dramatic rise in the power requested by the CPL of 20w from 0.3s to 0.7s. Then, as indicated in Fig. 3.21(a), we executed a dramatic drop of 10w (original value) in the time remaining. As shown in Fig. 3.21, the simulation results of this experiment are achieved for the DC-DC Buck power converter exposed to a dramatic change in CPL for both step-up fluctuation and step-down fluctuation.

When compared to previous techniques, the proposed NTSM controller delivers better anti-disturbance rejection and the fastest recovery performance for both step-up and step-down fluctuations. Furthermore, the proposed NTSM controller has a short settling time of 0.01s, a small overshoot, and imposes on the DC-DC Buck converter output voltage to precisely reach the desired reference value.



(a)



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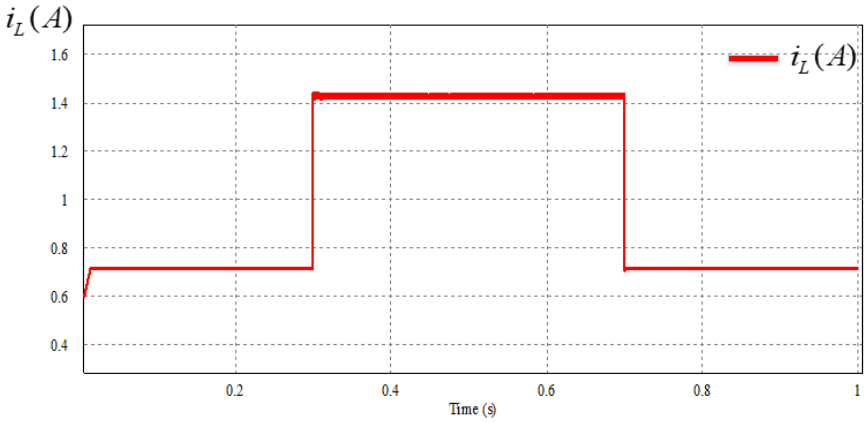
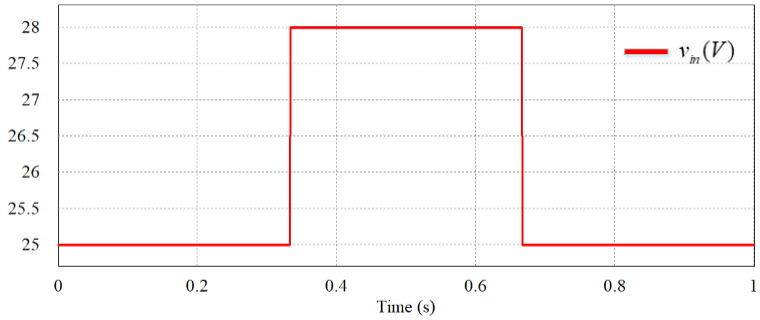


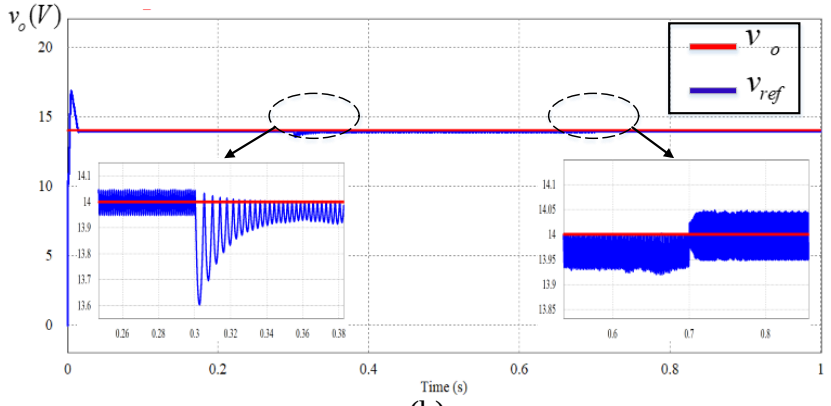
(c)

Fig. 3.21. The simulation results scenario of changing the power consumption of the DC-DC Buck converter, which includes: (a). CPL variation scenario, (b). output voltage behavior. (c). output current behavior

For the input voltage variation test, there is no significant variation observed in the behavior of the output voltage of the DC-DC Buck converter feeds a CPL, as illustrated in Fig. 3.22. As shown in Fig. 3.22(a), The DC-DC Buck converter's input voltage changes from 28 volts to 23 volts before returning to the nominal value. In this scenario, the power load demanded of the DC-DC Buck converter (CPL) is kept constant at 10 W. Based on the results, it is possible to conclude that the output voltage is maintained consistent and well controlled at 14V, with a very fast response throughout input voltage fluctuation.



(a)



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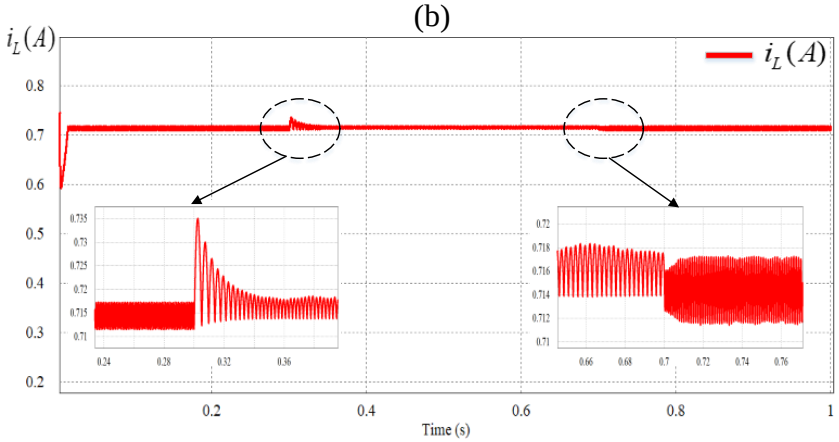

(c)

Fig. 3.22.The dynamic behavior of the DC-DC Buck converter during an input voltage variation test, which includes: (a). an input voltage variation scenario, (b). output voltage behavior, (c). output current behavior.

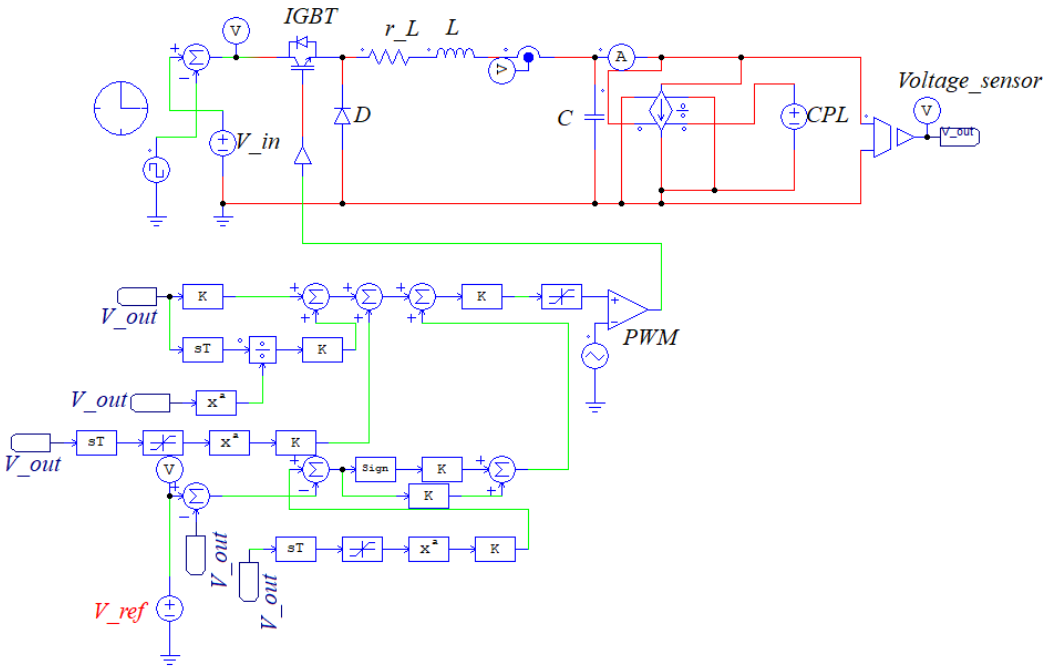

Fig. 3.23. PSIM software simulation of a DC-DC Buck converter feeding a CPL via the proposed NTSM controller

3.5 Conclusion

This chapter detailed the CPL effect produced by a DC-DC Buck converter feeding a tight voltage-controlled DC-DC Boost converter. To address the CPL effect in DC MGs and eliminate the singularity problem induced by the conventional terminal sliding mode controller, two types of nonlinear controllers are considered: SMC and NTSM controller. The proposed nonlinear controllers can mitigate the negative effects of CPLs while maintaining their efficiency. Theoretical development of SMC and NTSMC has demonstrated the stability of the DC-DC Buck converter feeding CPLs without the addition of virtual damping. Furthermore, the proposed NTSM controller and SMC proved fast response and fast-finite time convergence, as well as low control energy in the face of abrupt changes in CPL and input voltage fluctuations.

Chapter 4: Experimental validation

4.1. Introduction :

The DC microgrid and its primary control level are proven experimentally in this chapter using an experimental setup consisting of two DC-DC Buck converters connected in parallel and feeding a single resistive load. The proposed primary control is experimentally tested using two disturbances: plugging in/out the converters from the DC Bus and a sudden change in a resistive load of the DC Microgrid. The robustness and efficacy of the proposed primary controller are attained in this experimental validation.

In this chapter, on the other hand, the suggested NTSM controller and SMC are validated in a real-time experiment based on a prototype that contains a buck converter feeding a tightly voltage-regulated DC-DC boost converter that works as a CPL. Two examples are explored in this experimental validation to evaluate the efficacy of the suggested controllers: NTSM compensator and SMC: one with a fluctuate in power required (CPL) and the other with a fluctuate in the input voltage of the DC-DC Buck converter.

4.2. Experimental validation of the primary control level

The experimental setup depicted in Fig. 4.5 is constructed in the laboratory to verify the effectiveness and robustness of the proposed primary control of a DC Microgrid system comprised of two DC sources, two DC-DC Buck converters, and a resistive load. Thus, in this section, the proposed controller, which is based on the DSP TMS320F28035 C2000 microcontroller, has been tested on real hardware. This hardware is made up of two parallel DC-DC Buck converters that feed the same resistive load. Tables 2.1 and 2.2 show the parameters used in the experiment for the two DC-DC Buck power converters, which comprise the DC MG. Fig. 4.5 depicts the experimental setup of a DC Microgrid system loaded with a resistive load. For this experiment, the input and output voltages are set to 12V and 5V, respectively. The virtual resistances of the proposed primary controller (Droop control) are chosen to be $R_{d1} = R_{d2} = 2\Omega$. $R_{Line\_1} = 1.8\Omega$ and $R_{Line\_2} = 2\Omega$ are the selected line resistances.

The output voltage and inductor current of the DC-DC Buck converters were measured with a current sensor LV25-P (714227) and a voltage sensor LA25-NP (717087). The proposed primary controller experiment included two types of tests: The first was a plug in/out of one of the Buck converters in the DC MG system. A PSIM simulation of a DC MG in discrete-time mode is controlled by the recommended primary regulator based on the DSP TMS320F28035 C2000 microcontroller, as illustrated in Fig. 4.4. Using the proposed primary controller

algorithm described in Chapter 2, the outer and inner controllers of the two DC-DC Buck converters of the DC Microgrid were designed and converted to discrete-time as follows:

For converter 1, the controllers are obtained as

$$\begin{cases} G_{PI\_v-c1}(z) = \dfrac{0.4456594z - 0.4445406}{z-1} \\ G_{PI\_i\_c1}(z) = \dfrac{4.309186z - 4.276814}{z-1} \end{cases} \tag{4.1}$$

For converter 2, the controllers are obtained as

$$\begin{cases} G_{PI\_v\_c2}(z) = \dfrac{9.85502z - 9.78098}{z-1} \\ G_{PI\_i\_c2}(z) = \dfrac{1.3627104z - 1.3592826}{z-1} \end{cases} \tag{4.2}$$

Fig. 4.1 illustrates the dynamic behavior of the output currents i_{o_1}, i_{o_2} of the buck converters that comprise the DC Microgrid with the proposed primary controller during the plug-in/out experiment. In this experiment, the resistive load is fixed at $R_{Load} = 33\Omega$ and the input voltage of each buck converter is kept at $v_{in} = 12V$ .Based on the results, the output current of the DC-DC buck converters share the same value at $i_o \approx 0.43A$ with a very fast response. In addition, the suggested controller maintained the same power demanded by the resistive load of the DC MG during the disconnect of converter II from the moment 2s to 3.2s. With a very fast time response, the current values are recovered to 0.43A $i_o \approx 0.43A$ after moment 3.2 s.

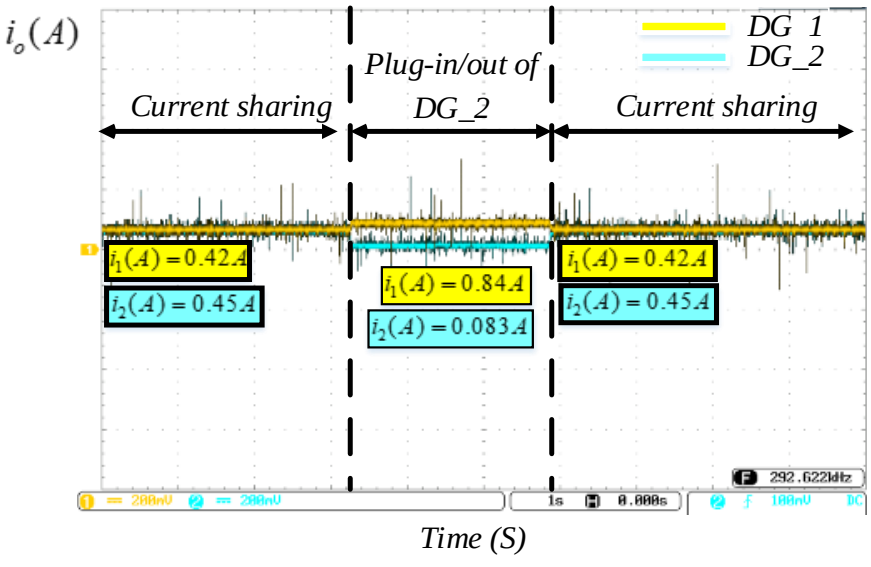

Fig. 4.1.Dynamic response of the DC-DC Buck converter output currents forming the DC Microgrid during the Plug-in/out scenario

Fig. 4.2 depicts the experimental result of the DC Bus of the DC Microgrid system during the disconnection and reconnecting of converter 2. At t=2 s, the DC-DC buck converter II is disconnected from the DC Bus, and at t=3.2 s, it is reconnected to the DC Bus voltage.

It can be shown that the suggested primary controller delivers a robust control and steady operating performance for the DC Bus voltage of the DC MG system when the buck converter II is unplugged and attached, respectively. The voltage deviation caused by the primary control, on the other hand, need restoration by using a secondary controller.

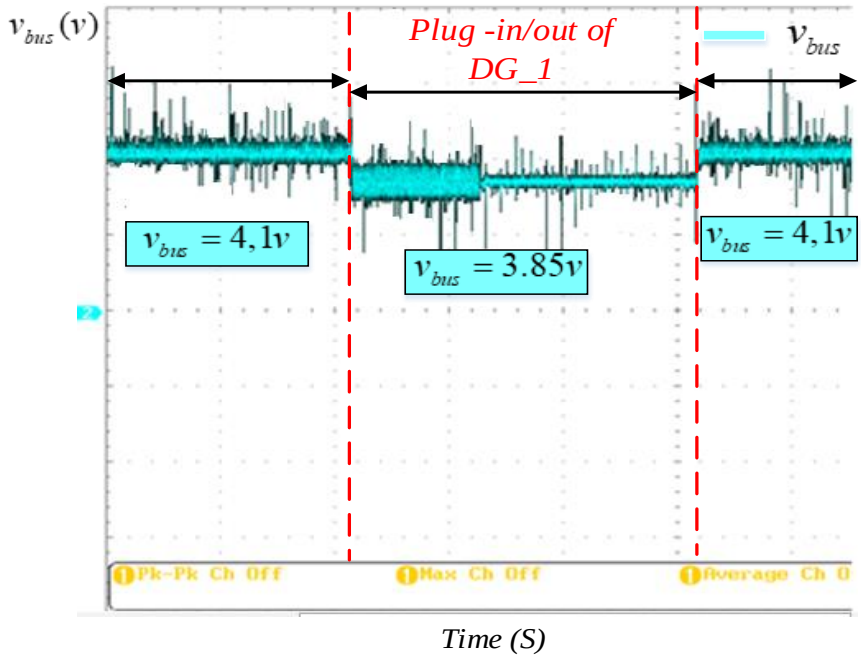

Fig. 4.2.The DC Microgrid's DC Bus Voltage during the plug-in/out scenario

In the second scenario, the test of the sudden fluctuation of the resistive load, the value of the DC Microgrid's resistive load varied from 33Ω to 16.5Ω at 5.8s. In this case, the input voltage of the DC-DC Buck converters, forming the DC Microgrid system, is kept fixed at 12v.

Based on the experimental results shown in Fig. 4.3, it is clear that the proposed primary controller (Droop control) offers robust control and stable operation behavior of the output currents of the DC-DC Buck converters that comprise the DC Microgrid during sudden fluctuation in the DC Microgrid's resistive load.

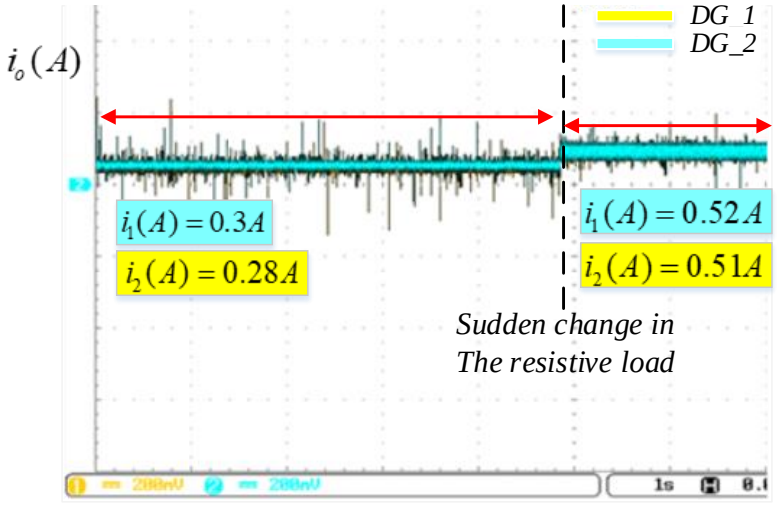

Fig. 4.3. Dynamic response of the DC-DC Buck converter output currents forming the DC Microgrid during a resistive load fluctuation scenario

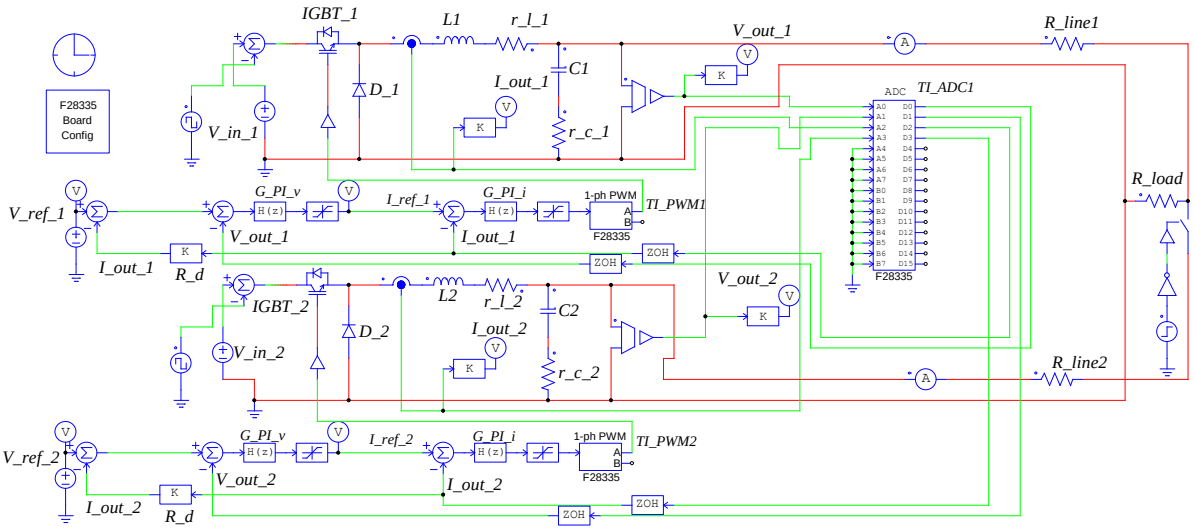

Fig. 4.4. Psim simulation of a DC Microgrid feeding a resistive load using the suggested primary control in discrete-time mode

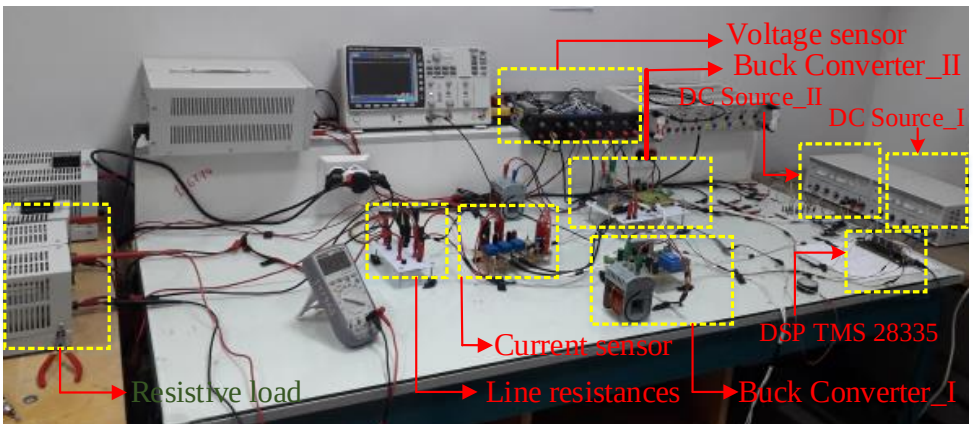

Fig. 4.5. An illustration of the experimental setup of a DC Microgrid feeding a resistive load.

4.3. Experimental validation of a robust SMC loaded for a DC-DC Buck converter feeding a CPL

This Subsection tries to demonstrate the efficacy of the suggested SMC for a DC-DC Buck converter feeding a CPL based on experimental validation. Fig. 4.6 depicts the equivalent experimental platform. The suggested SMC is developed in real time with the help of a DSP TMS320F28035 C2000 microcontroller. As depicted in Fig. 4.19, the experimental test platform includes a digital oscilloscope, a DC power supply, a DC-DC buck converter, a voltage sensor LA25-NP (717087), a DC-DC boost converter, and a TMS320F28035 C2000 microcontroller. The CPL is represented as a DC-DC boost converter with a tightly regulated output voltage. In this experiment, the DC-DC boost converter is controlled by an integral-double-lead controller (type III) as described in Chapter 2. Table 3.1 lists the specifications value of the DC-DC Buck converter. The specification values of the boost converter are shown in Table 4.1. PSIM discrete-time simulation of a DC-DC Buck converter supplying a boost converter whose output voltage is tightly controlled as illustrated in Fig. 4.10.

The type III controller's discrete-time for the DC-DC Boost converter is stated as follows:

$$G_b(z) = \frac{0.14166101z^3 - 0.13646717z^2 - 0.14166101z + 0.13651566}{z^3 - 2.4715066z^2 + 2.0128468z - 0.54134021} \tag{4.3}$$

Tab 4.1- DC-DC Boost converter experimental parameters

Variables	*Descriptions*	*Value*
v_{in_Boost}	*Input voltage*	*14V*
v_{o_Boost}	*Voltage Reference*	*20V*
L_{Boost}	*Nominal inductance*	*0.52mH*
C_{Boost}	*Nominal capacitance*	$470\mu F$
f_{sw}	*Switching frequency*	*25KHz*
R	*Resistive load*	30Ω
D	*Duty cycle*	*0.5*

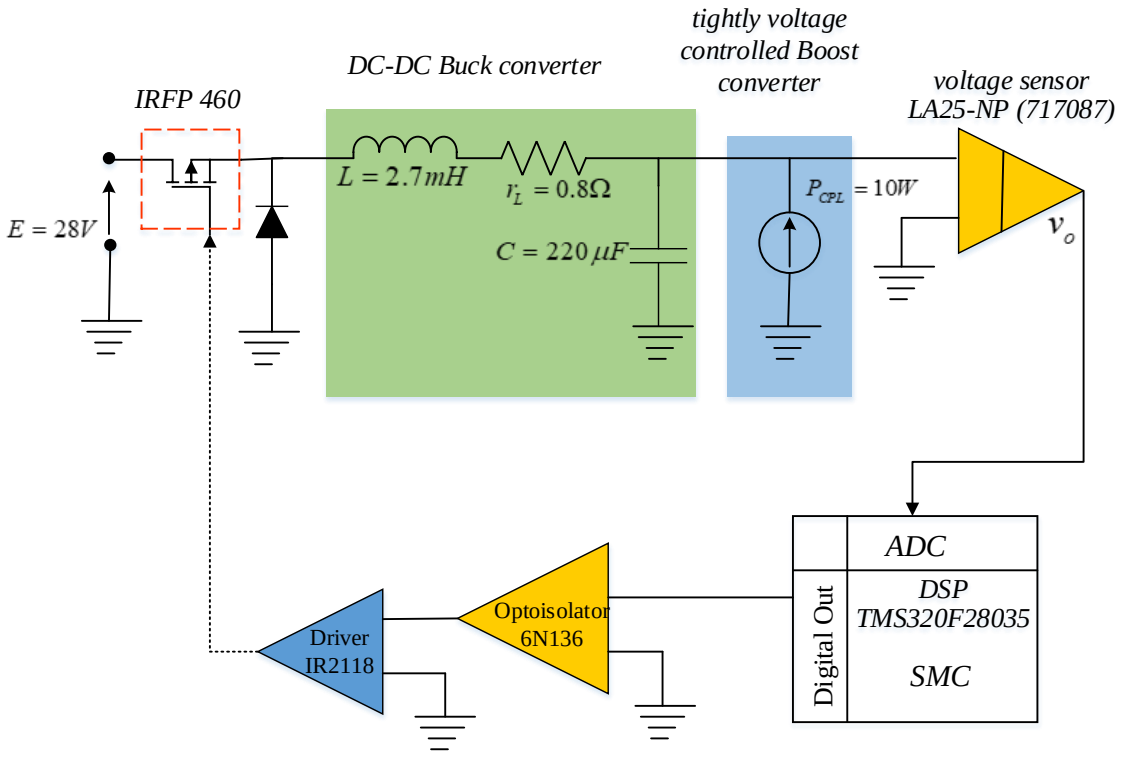

Fig. 4.6. The similar experimental setup comprising a DC-DC Buck converter feeding a CPL

External disturbances in the power load demand and input voltage of the DC-DC boost converter are real-time tests used to validate the effectiveness and robustness of the proposed SMC. To test the proposed SMC against CPL variations, we vary the resistive load of the boost converter to change the power load requested by the DC-DC buck converter. The CPL fluctuation scenario is carried out by gradually raising the power requirement from 10W to 20W, and ultimately to 30W. Following that, we reduced the power demanded (CPL) from 30 W to 20W, and then to the nominal amount of 10W as illustrated to Fig. 4.7.

Fig .4.7 shows that the recommended SMC has a superior transient response than controllers that employ passive components in parallel with CPLs to get the best results. Furthermore, the suggested controller can compel the output voltage to track the reference voltage $v_{ref} = 14V$ as quickly as possible despite fluctuations in CPL. The system stability of the buck converter is maintained even when the power utilized by the CPL fluctuates. Fig. 4.8 shows the dynamic behavior of the duty cycle of the buck converter with the consumed power changes from 10 W to 20 W.

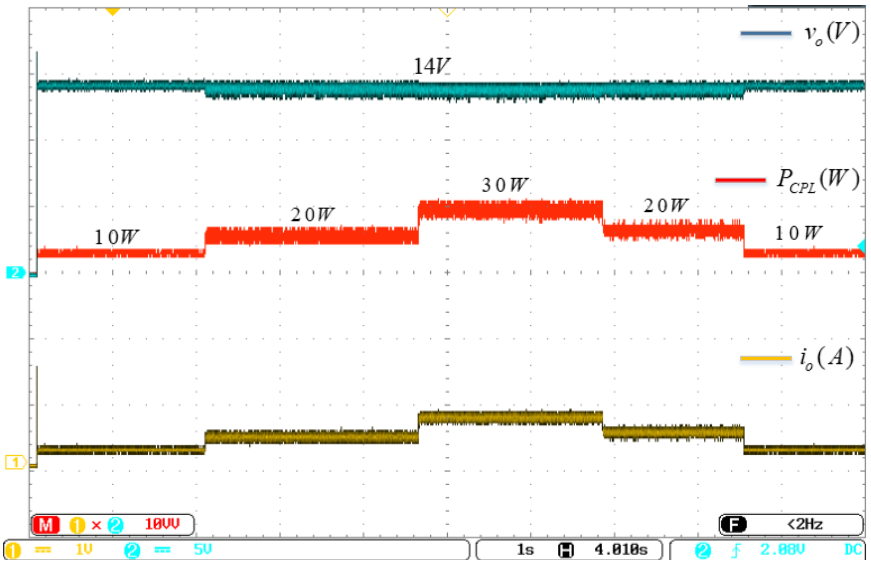

Fig. 4.7. Experimental results of CPL consumed power fluctuations sequential test

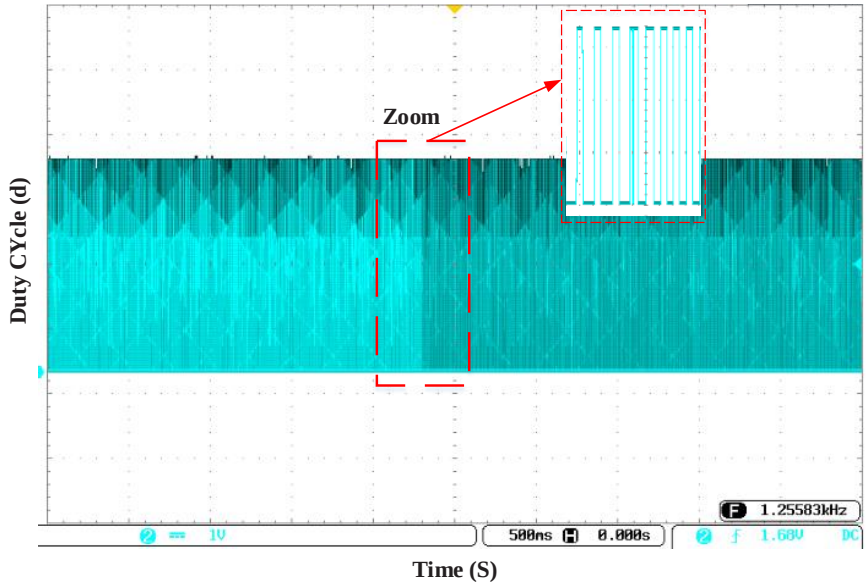

Fig.4.8. Experimental result of the duty cycle transient response against changes in power absorbed by a CPL

The second disturbance is induced by tiny fluctuations in the input voltage of the DC-DC buck converter. On the other hand, we maintained the power load (CPL) requirement unchanged. In this scenario, the input voltage is decreased sequentially from 28V to 25V and then returned to 28V.

The DC-DC buck converter operation, as shown in Fig. 4.9, has a brief transient dynamic, equating to a short settling time of less than 0.06 s. The DC-DC Buck converter's output voltage has a slight overshoot and remains steady at the intended reference value.

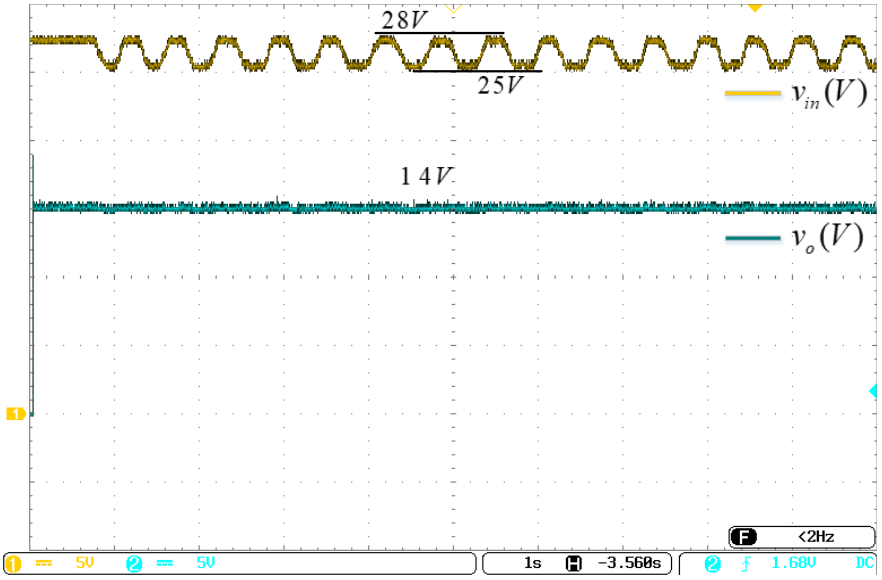

Fig. 4.9. Experimental results of input voltage variation test

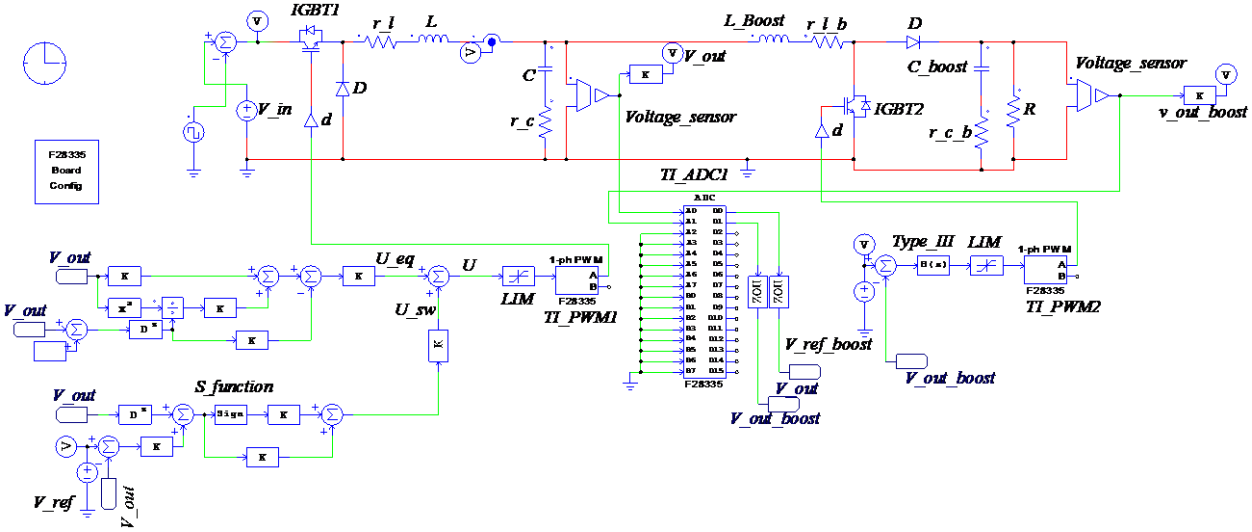

Fig. 4.10. PSIM simulation of a DC-DC Buck converter feeding a tightly voltage controlled DC-DC Boost converter in discrete-time mode

4.4. Experimental validation of a robust NTSM controller loaded for a DC-DC Buck converter feeding a CPL

As seen in Fig. 4.19, a theoretical NTSM controller has been validated in a laboratory prototype that incorporates a DC power supply, a DC-DC buck converter, a voltage sensor LA25-NP

(717087), a tightly voltage regulated boost converter, and a DSP TMS320F28035 C2000 microcontroller. Fig. 4.6 displays a same experimental platform with a Buck converter supplying a CPL, which is regulated by an NTSM controller. The type III controller is utilized for the DC-DC boost converter, and the controller's discrete time is specified in equation (4.3). PSIM simulation of a Buck converter feeding a tightly voltage-controlled DC-DC boost converter loaded by an NTSM controller in discrete-time mode, as shown in Fig. 4.18. The parameters of the DC-DC boost converter are shown in Table 4.1. Moreover, the performance of the proposed control strategy is tested by two disturbances that are usually applied to DC-DC converters to investigate the robustness and effectiveness of the proposed NTSM controller: Variations in input voltage and CPL.

For the first disturbance, the DC-DC Buck converter's CPL consumed power is increased from 10 W to 20 W and then returned to 10 W. The power of CPL is changed through the resistance of the DC-DC boost converter. Figs. 4.11, 4.12, 4.13, and 4.15 show the experimental results for this disturbance scenario. As the figures show, the suggested NTSM controller technique has less overshoot than the controllers utilized to reduce the CPL impact.

With a rapid settling time of less than 0.02s, the proposed controller adjusts the output voltage to achieve its desired purpose at $v_o = 14V$. These experimental results demonstrate that the proposed NTSM controller may be highly effective for regulating the DC-DC buck converter feeding a CPL. This controller improves its stability and adaptability in the face of external disturbances to the power used by the CPL.

Even when the power received by the CPL is impacted by sequential variations, the output voltage remains constant, according to Fig. 4.14. The asymptotic stability of the suggested controller has been determined, taking into account the changes imposed on the power load need.

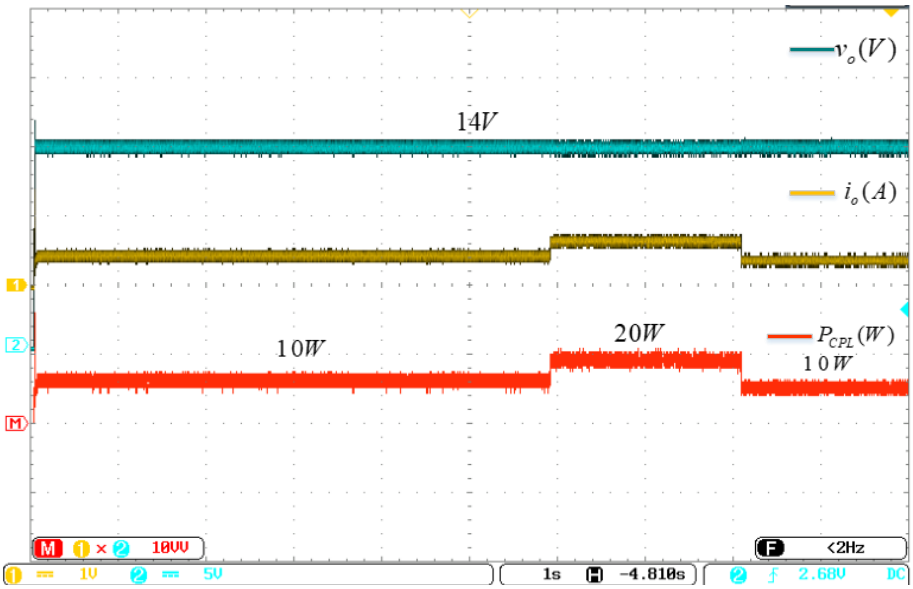

Fig. 4.11. Real-time implementation results of the CPL variation experiment

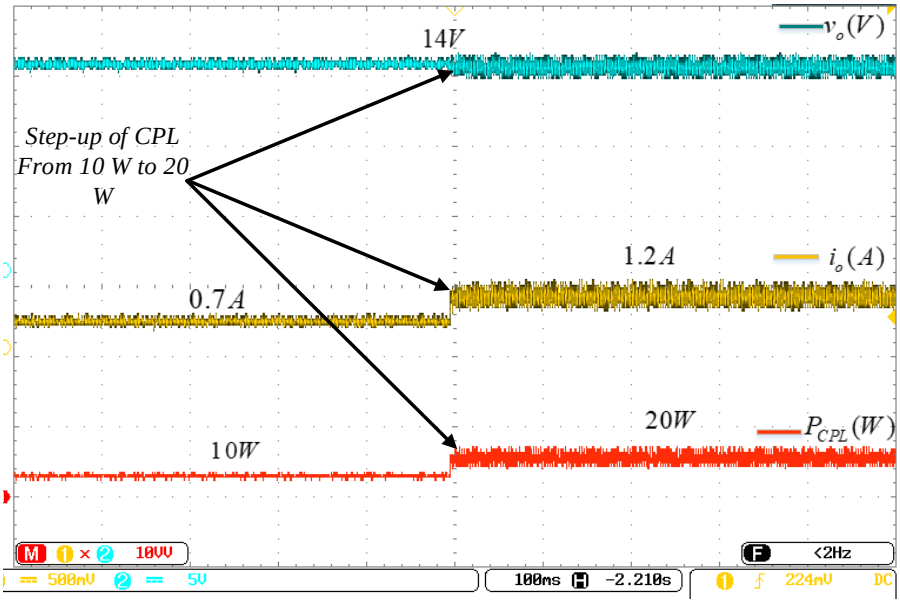

Fig. 4.12. Experiment results for increasing the power consumption by the CPL from 10 W to 20 W

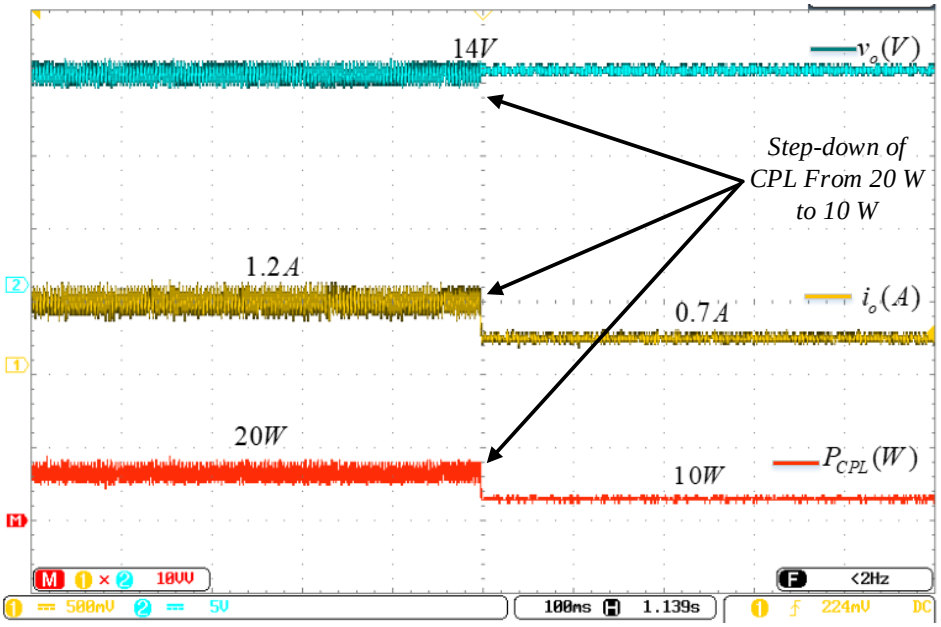

Fig. 4.13. Experiment results for reducing the CPL's power consumption from 20 W to 10 W

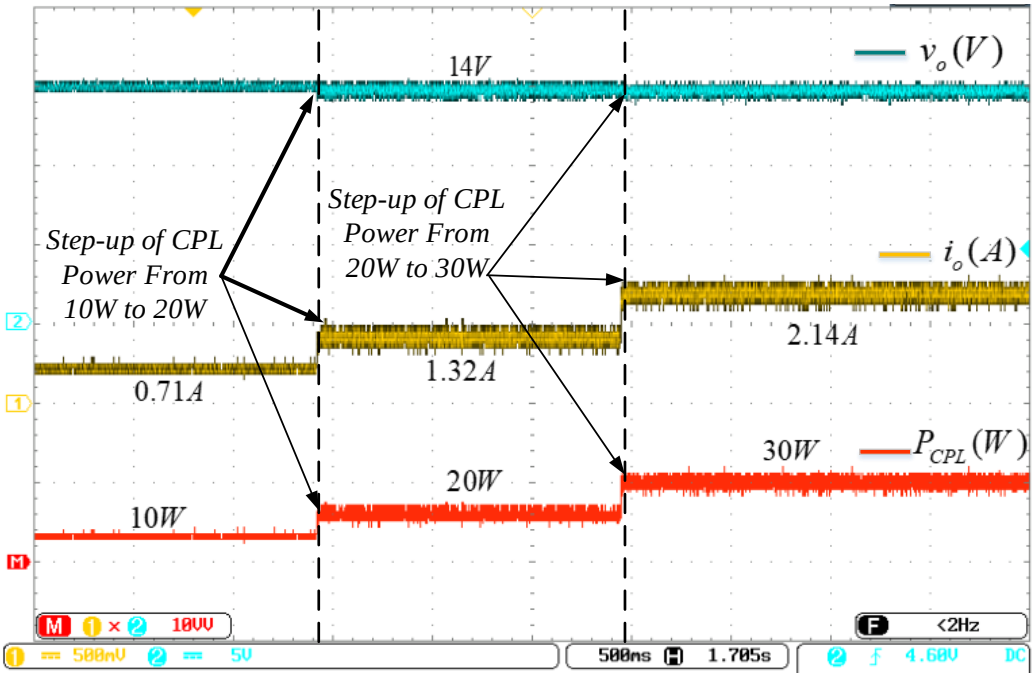

Fig. 4.14. Experiment results of different step variations in the power consumed by a CPL

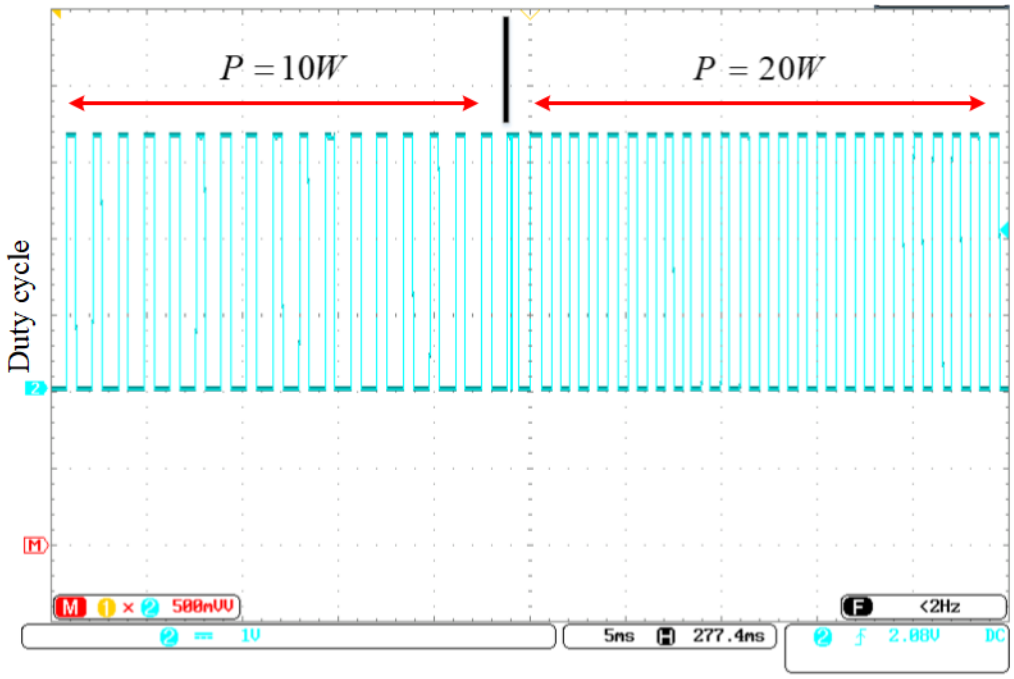

Fig. 4.15. Experimental result of duty cycle under power changes

Input voltage fluctuation is one of the most serious power quality issues, since it can damage electronic devices and cause significant systemic problems. Changes in input voltage also decrease the performance of electronic equipment and cause significant voltage and current fluctuations.

As shown in Fig. 4.17, the robustness and efficacy of the proposed NTSM controller technique, as well as power quality, were validated experimentally by implementing a 10% successive fluctuation in the input voltage of a DC-DC buck converter supplying a CPL. The CPL is represented by a boost converter whose output voltage is firmly regulated.

In this experiment, the DC-DC buck converter's input voltage was altered at a rate of 3V, going from 28 V to 25 V and back again. In this experiment, the power consumption by the CPL power is set constant at 10 W. Figs. 4.16 and 4.17 depict the output voltage response of a DC-DC Buck converter feeding a CPL before and after introducing successive adjustments in the input voltage.

Using the experimental results shown in Figs. 4.16 and 4.17, the proposed NTSM controller was shown to be both robust and dynamically efficient. As can be observed, the suggested NTSM controller operates accurately even when the input voltage fluctuates, and the output voltage of the DC-DC buck converter stays unchanged and fast-tracked to the system's reference value of 14 V. Furthermore, the effect of variable input voltage on the output voltage of a DC-DC buck

converter feeding a CPL is basically non-existent. The suggested NTSM controller avoids variations in the input voltage of the DC-DC buck converter feeding a CPL.

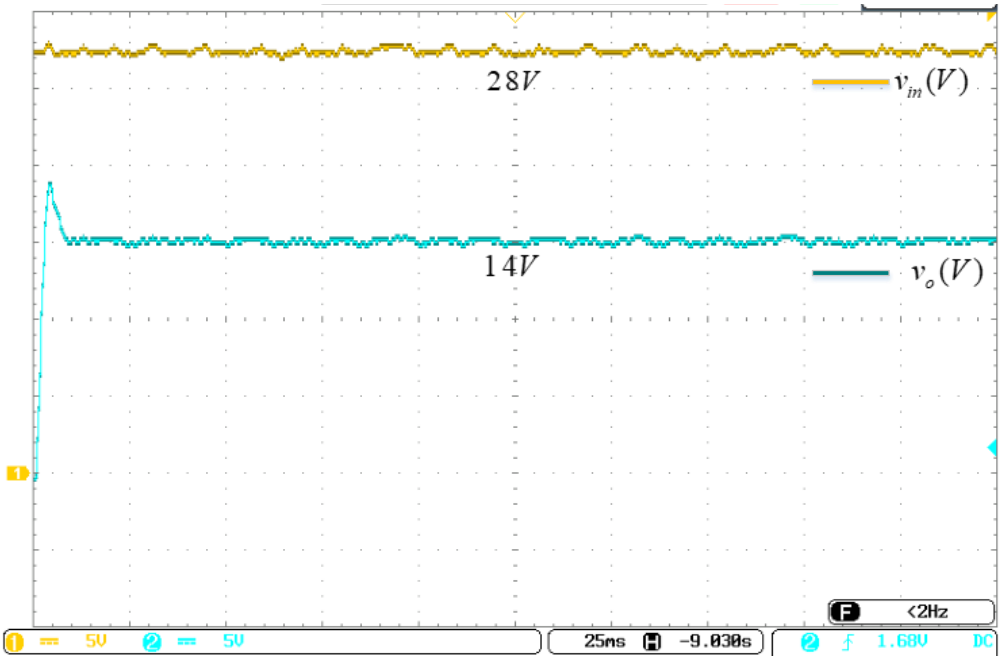

Fig. 4.16. Experiment results for DC-DC Buck converter output voltage without altering the input voltage

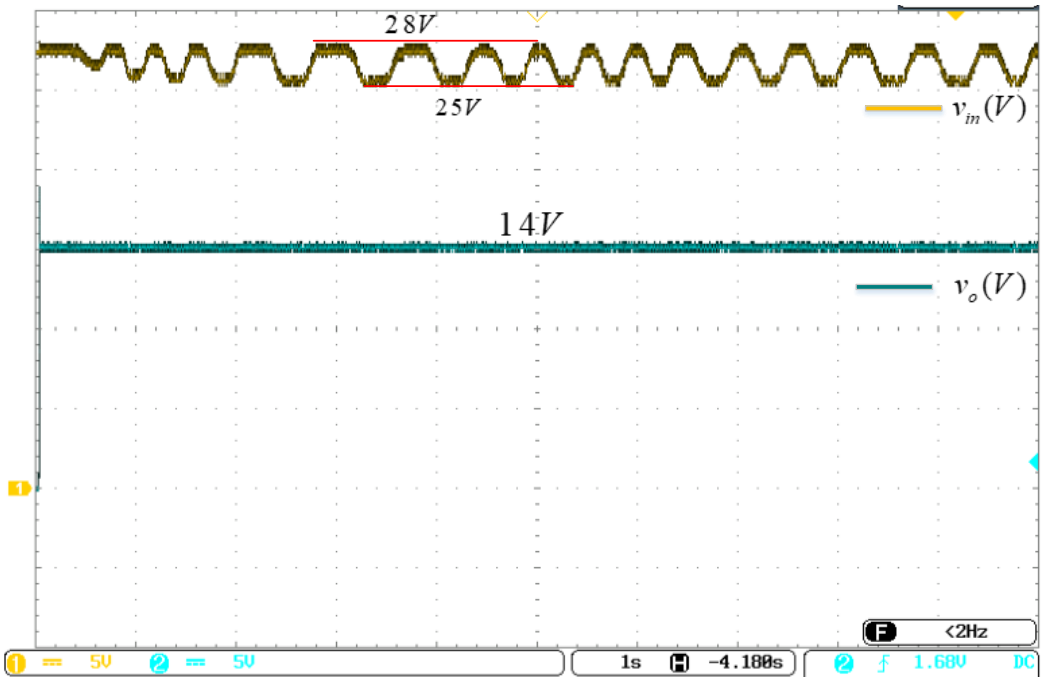

Fig. 4.17. Experimental results of output voltage under the input voltage fluctuation test

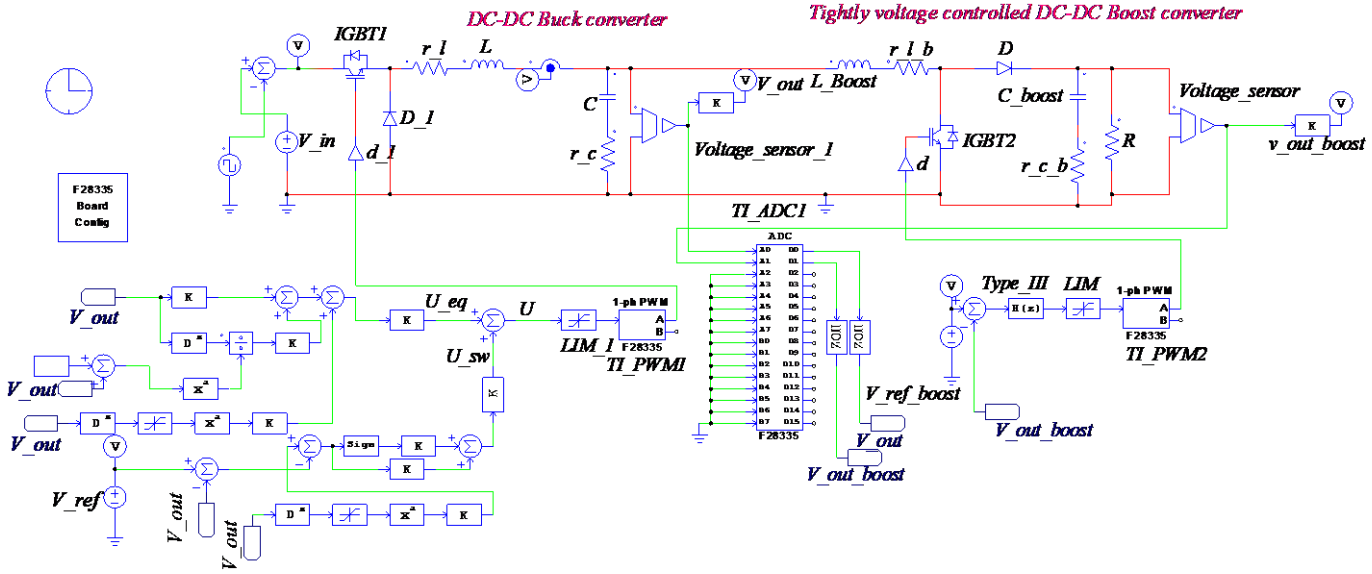

Fig. 4.18. PSIM simulation of a DC-DC Buck converter feeding a tightly voltage-controlled DC-DC Boost converter fed in discrete-time mode by an NTSM controlle

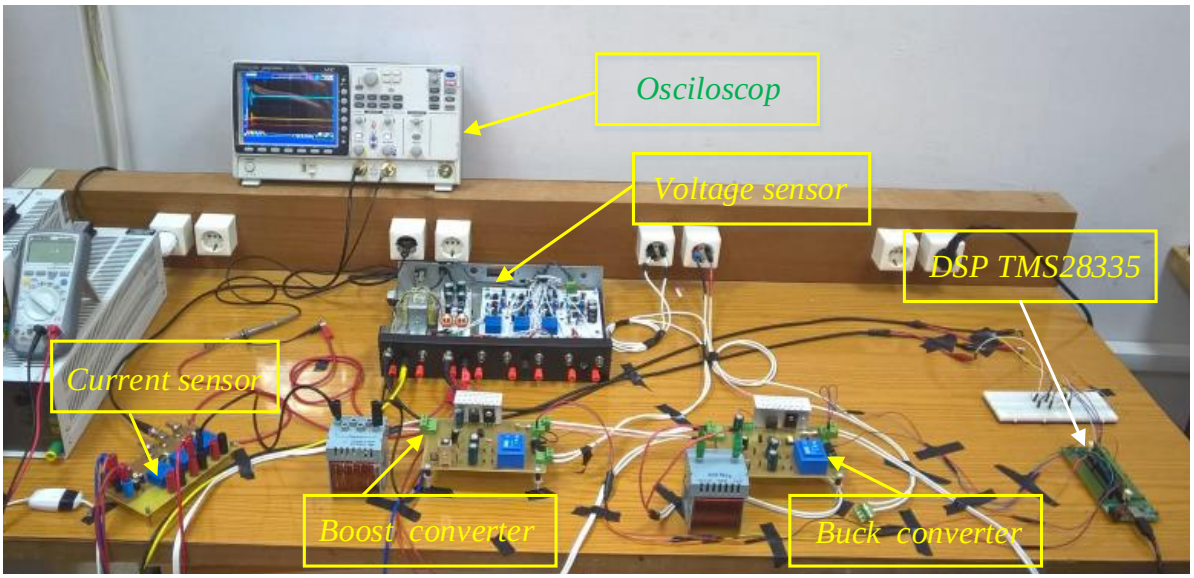

Fig. 4.19. An experimental setup of a DC-DC Buck converter feeding a tightly voltage regulated boost converter

4.5. Conclusion

The experimental validations presented in this chapter demonstrate the effectiveness of the proposed primary control approach in achieving their objectives in control and sharing the same power between the DC-DC converters. Several scenarios were conducted in the presence of external disturbances to assess the effectiveness and robustness of the suggested primary controller of the DC MG in real time. Furthermore, the robustness and dynamic efficiency of the

NTSM controller and SMC methods were evaluated using a real-time experimental setup comprising a Buck converter feeding a Boost converter whose output voltage is tightly regulated. The NTSM controller and SMC techniques perform well in terms of recovery, settling time, and overshoot when the power load demanded (CPL) and input voltage of the DC-DC Buck converter are changed in real-time.

General conclusion

The principal goal of this thesis work is to contribute to the implementation and study of a DC Microgrid that incorporates renewable sources and storage elements. A literature study on DC microgrid systems was undertaken in this context. The benefits of the DC microgrid versus the AC microgrid have been argued, with the DC microgrid being chosen due to its compact size, low power consumption, and superior efficiency when compared to the AC one. Thus, fundamental problems about DC microgrid implementation, such as CPL stability and current sharing when many DC sources operate in parallel, have been addressed. Therefore, the droop control approach (Primary control level) was used to improve current sharing across parallel DC sources. The primary control level includes decentralized controllers. Each decentralized controller is composed of a droop controller combined with voltage and current controllers. The droop controller uses a virtual impedance to minimize circulating current and focus the power of the DC MG on the resistive load. Voltage and current controllers are used to eliminate voltage differences between the output voltages of DC-DC converters from causing current to circulate. Therefore, a primary control was applied for achieving the current sharing, taking a case study of two paralleled DC-DC Buck converters feeding a single resistive load. A stability analysis was carried out in various scenarios such as plug-in/play, resistive load fluctuations, and input voltage variation.

Despite the fact that DC microgrid has grown in popularity over the last decade, this type of MG still suffers from constant power loads. Because of the INI property of CPL, energy availability in the DC MG system may be reduced. To address the INI property, a Buck converter feeding a boost converter whose output voltage is tightly controlled has been performed. This chosen application has been addressed with two controller types in consideration: SMC and NTSM controller. The SMC was used to adjust the output voltage of the DC-DC Buck converter feeding a CPL that was provided. A robust non-singular terminal sliding mode (NTSM) controller has been designed to solve the stability issue caused by CPLs and eliminate the singularity problem induced by the conventional TSM controllers. The proposed control strategy is able to solve the negative effect of CPLs without degrading the efficiency. The theoretical development has proved the stability of the buck converter feeding CPLs without adding passive loads in parallel with the CPLs. In addition, the NTSM controller has demonstrated fast response and fast-finite time convergence against sudden changes in CPL and input voltage fluctuations. The simulation study validates the effectiveness of the proposed controllers.

The results of the simulation study were confirmed experimentally utilizing two experimental setups generated by the Texas Instruments TMS320F28335 controller. The first is constructed by connecting two parallel Buck converters to supply a single resistive load, in which two DC sources supply these converters. This experimental platform was utilized to test the DC MG's primary control (Droop control approach). The second experimental setup was used to validate the proposed controllers, SMC and NTSMC, for a DC-DC Buck converter feeding a CPL. In this experimental setup, a DC source supplies a Buck converter, which feeds a voltage-controlled boost converter. The boost converter acts as a CPL. A double-lead controller (type III) was used to control the boost converter. The CPL changing test is performed by modifying the boost converter's resistive load. The input voltage variation experiment is carried out using a DC source.

Perspectives

In terms of future research, and within the context of industrial projects, the NTSM control approach will be expanded to another constant power load, such as an AC motor drive with constant speed. It is also suggested that an NTSM controller be used to provide the secondary control level for a DC Microgrid system feeding a CPL. Based on the results of this study, the authors would like to investigate and implement the tertiary control level for a DC Microgrid system feeding a CPL.

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Remarque: The term $x_1^{\frac{q}{p}-1}x_2$ is very important to define the singularity problem. For different $x_2 \neq 0$ the singular term is calculated and shown in Fig. A1. Based on the observation, the following results can be obtained:

(1) $x_1^{\frac{q}{p}-1}x_2 \to \infty$, as $x_1 \to 0$ subject to $x_2 \neq 0$

(2) $x_1^{\frac{q}{p}-1}x_2 \neq 0$, subject to $x_2 \neq 0$

(3) $sgn\left(x_1^{\frac{q}{p}-1}x_2\right) = sgn(x_2)$, subject to $x_2 \neq 0$

(4) $\lim_{x_1 \to 0, x_2 \to 0} x_1^{\frac{q}{p}-1}x_2 = 0$, along $s_1 = x_2 + \beta x_1^{\frac{q}{p}-1} = 0$

(5) The second term of the Eq. (3.40) that containing $-\beta q/p x_1^{\frac{q}{p}-1}x_2$ is singular only on the x_2-axis but excluding the point $(x_1=0, x_2=0)$.

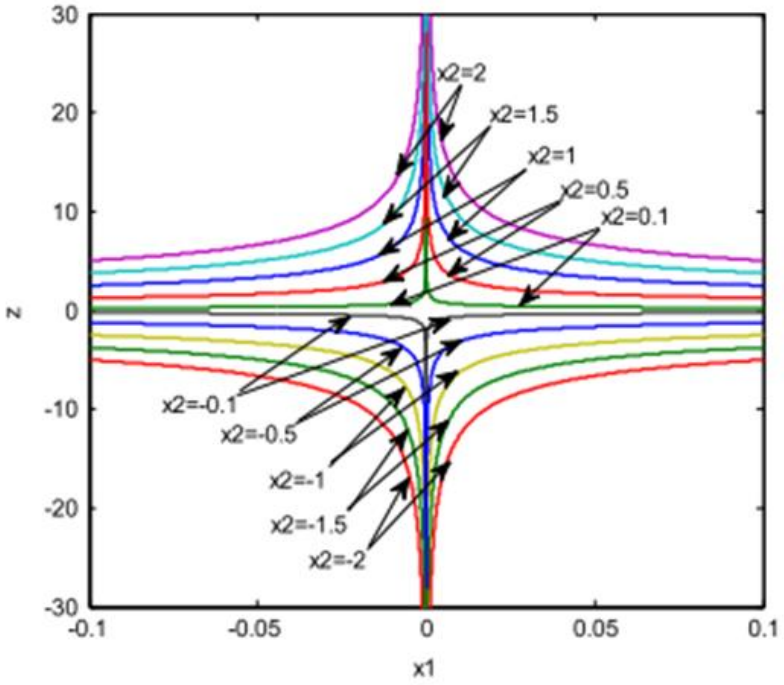

Fig. A1.Singular term $z = x_1^{\frac{q}{p}-1}x_2$

The equipment used in the experimental setup of a DC-DC buck converter feeding a voltage-controlled boost converter is listed in Table A1. This boost converter acts as a CPL.

Tab A1. Equipment used in the experimental setup of a DC-DC Buck converter feeding a CPL

N	**The equipment**
1	DC-DC Buck converter
2	DC-DC Boost converter
3	DC source giving a 28 V
4	DSP TMS28335 C2000 microcontroller
5	Voltage sensor LA25-NP (717087)
6	Current sensor LV25-P (714227)
7	The buck converter's inductance $L=2.7mH$
8	The boost converter's inductance $L_b=0.52mH$
9	The buck converter's capacitance $C=470\ uF$
10	The boost converter's capacitance $C_b=470uF$
11	The boost converter's resistive load $R_{Load}=30\Omega$
12	Code Composer Studio software (CCS)
13	PSIM software

Tab A2. Control Parameters used in Sliding Mode Controller for a DC-DC Buck converter feeding a CPL

Parameter	Value
n	1
λ	10e3
k	10e16
Q	10e16

Tab A3. Control Parameters used in nonsingular Terminal Sliding Mode controller for a DC-DC Buck Converter feeding a CPL

Parameter	Value
p	4
q	3
β	10e6
k	10e20
Q	10e16

ملخص

في العقود الأخيرة، أصبح استنزاف موارد الطاقة الأحفورية أمرا شائعا. يؤدي هذا الاستنزاف إلى استهلاك متزايد للطاقة. علاوة على ذلك، كثيرا ما يُلقى اللوم على موارد الطاقة الأحفورية هذه باعتبارها السبب الرئيسي لظاهرة الاحتباس الحراري. ويتطلب هذا التحدي البحث عن بديل ممكن لموارد الطاقة الأحفورية هذه. ومن ناحية أخرى، يتزايد الاهتمام بتطوير تقنيات جديدة لاستغلال مصادر الطاقة المتجددة بسبب نضجها التكنولوجي وانخفاض تكلفتها. ولذلك، أصبح استخدام الطاقة المتجددة لإنتاج الكهرباء حلاً شائعًا. أحد هذه الحلول هو مفهوم نظام الشبكة الصغيرة، وهو متوافق ومفيد بشكل خاص لتوليد الكهرباء بالإضافة إلى تكامل المصادر المتجددة وأنظمة تخزين الطاقة. على الرغم من فوائد نظام الشبكة الصغيرة ذات التيار المستمر، فإن أحمال الطاقة الثابتة توفر تحديًا للاستقرار بسبب المعاوقة السلبية المتزايدة لأحمالها. تعمل هذه المعاوقة الإضافية السلبية على تقليل عامل التخميد لنظام الشبكة الصغيرة ذات التيار المستمر، مما يؤدي إلى تذبذب غير مخمد في تيار الخروج والجهد. ونتيجة لهذه التذبذبات غير المخمدة، تصبح نظام الشبكة الصغيرة ذات التيار المستمر غير مستقرة. تتناول هذه الأطروحة دراسة وتطبيق في الواقع نظام الشبكة الصغيرة ذات التيار المستمر التي تغذي حمل طاقة ثابت، حيث يحاكي محول التعزيزمنظم باحكام من حيث جهد خروج حمل طاقة ثابت. تقترح هذه الأطروحة وحدة تحكم قوية في وضع الانزلاق الطرفي غير المفرد لتحقيق استقرار النظام عن طريق تجنب خاصية المعاوقة الاضافية السلبية والحفاظ على توافر الطاقة. تتميز وحدة التحكم القوية في وضع الانزلاق الطرفي غير المفرد بتجنب مشكلة التفرد التي تحدث عن طريق وحدة التحكم في وضع الانزلاق الطرفي التقليدي.

وبصرف النظر عن التحدي المتمثل في قيام نظام الشبكة الصغيرة بتزويد حمل طاقة ثابت، فقد تم أيضًا تناول مشكلة تقاسم الطاقة بين أنظمة الطاقة الموزعة التي تشكل نظام الشبكة الصغيرة ذات التيار المستمر. باستخدام دراسة حالة لمحولي جهد متوازيين يغذيان حملًا مقاومًا واحدًا، تمت معالجة مشكلة تقاسم الطاقة باستخدام مستوى التحكم الأساسي (طريقة التحكم في

التدلي). تم تنفيذ مستوى التحكم الأساسي باستخدام وحدات تحكم تناسبة-تكاملية لتنظيم التيار والجهد، بالإضافة إلى إضافة حمل مقاوم افتراضي لتجنب تداول التيار. تم تأكيد وحدات التحكم المقترحة باستخدام عمليات المحاكاة والإعداد التجريبي.

الكلمات المفتاحية: الشبكة الصغيرة ذات التيار المستمر، التحكم في التدلي، أحمال الطاقة الثابتة، تقاسم الطاقة، المعاوقة السلبية المتزايدة، وضع الانزلاق الطرفي، جهاز التحكم في وضع الانزلاق الطرفي غير المفرد، مشكلة التفرد، جهاز التحكم التناسبي-التكاملي.