



المسيلة في : 2025/11/24

الرقم : 001/ق.ا.ك.ا. 2025/

شهادة إدارية

بعد الإطلاع على التقارير الايجابية الواردة من السادة الخبراء أعضاء لجنة دراسة المطبوعة الجامعية والاتية أسماؤهم:

- بوزيت نصرالدين أستاذ محاضر "أ" جامعة فرحات عباس - سطيف 1
- بلوطي عادل أستاذ محاضر "أ" جامعة محمد بوضياف - المسيلة
- قبائلي فريدة أستاذ محاضر "أ" جامعة محمد بوضياف - المسيلة

صادق أعضاء اللجنة العلمية على قبول المطبوعة البيداغوجية مع إمكانية إتخاذها سندا في تدريس طلبة السنة الثانية ليسانس الكترولنيك، في ميدان علوم و تكنولوجيا و أن تعتمد في أي تقييم المسار العلمي للأستاذ المعني بختي الهادي (أستاذ محاضر قسم "ب" - جامعة محمد بوضياف - المسيلة) تحت عنوان :

Fundamental electronics 1

رئيس اللجنة العلمية



رئيس القسم





جامعة محمد بوضياف - المسيلة
Université Mohamed Boudiaf - M'sila

جامعة محمد بوضياف - المسيلة -

MOHAMED BOUDIAF UNIVERSITY -M'SILA-

كلية التكنولوجيا

FACULTY OF SCIENCE AND TECHNOLOGY

ELECTRONICS DEPARTMENT

Course support

Fundamental electronics 1

Second year Bachelor's degree course

Sectors : Electronics & Electrical Engineering

Directed by :

Dr. BAKHTI Haddi

May 2023

Semestre: 3**Unité d'enseignement: UEF 2.1.2****Matière 1: Electronique fondamentale 1****VHS: 45h00 (Cours: 1h30, TD: 1h30)****Crédits: 4****Coefficient: 2****Objectifs de l'enseignement:**

Expliquer le calcul, l'analyse et l'interprétation des circuits électroniques. Connaître les propriétés, les modèles électriques et les caractéristiques des composants électroniques : diodes, transistors bipolaires et amplificateurs opérationnels.

Connaissances préalables recommandées

Notions de physique des matériaux et d'électricité fondamentale.

Contenu de la matière :

Le nombre de semaines affichées sont indiquées à titre indicatif. Il est évident que le responsable du cours n'est pas tenu de respecter rigoureusement ce dimensionnement ou bien l'agencement des chapitres.

Chapitre 1. Régime continu et Théorèmes fondamentaux**3 semaines**

Définitions (dipôle, branche, nœud, maille), générateurs de tension et de courant (idéal, réel), relations tension-courant (R, L, C), diviseur de tension, diviseur de courant. Théorèmes fondamentaux : superposition, Thévenin, Norton, Millmann, Kennelly, Equivalence entre Thévenin et Norton, Théorème du transfert maximal de puissance.

Chapitre 2. Quadripôles passifs**3 semaines**

Représentation d'un réseau passif par un quadripôle. Grandeurs caractérisant le comportement d'un quadripôle dans un montage (impédance d'entrée et de sortie, gain en tension et en courant), application à l'adaptation. Filtres passifs (passe-bas, passe-haut, ...), Courbe de gain, Courbe de phase, Fréquence de coupure, Bande passante.

Chapitre 3. Diodes**3 semaines**

Rappels élémentaires sur la physique des semi-conducteurs : Définition d'un semi-conducteur, Si cristallin, Notions de dopage, Semi-conducteurs N et P, Jonction PN, Constitution et fonctionnement d'une diode, polarisations directe et inverse, Caractéristique courant-tension, régime statique et variable, Schéma équivalent.. Les applications des diodes : Redressement simple et double alternance. Stabilisation de la tension par la diode Zener. Ecrêtage, Autres types de diodes : Varicap, DEL, Photodiode.

Chapitre 4. Transistors bipolaires**3 semaines**

Transistors bipolaires : Effet transistor, modes de fonctionnement (blocage, saturation, ...), Réseau de caractéristiques statiques, Polarisation, Droite de charge, Point de repos, ... Etude des trois montages fondamentaux : EC, BC, CC, Schéma équivalent, Gain en tension, Gain en décibels, Bande passante, Gain en courant, Impédances d'entrée et de sortie. Etude d'amplificateurs à plusieurs étages BF en régime statique et en régime dynamique, condensateurs de liaisons, condensateurs de découplage. Autres utilisations du transistor : Montage Darlington, transistor en commutation, ...

Chapitre 5 - Les amplificateurs opérationnels :**3 semaines**

Principe, Schéma équivalent, Ampli-op idéal, Contre-réaction, Caractéristiques de l'ampli-op, Montages de base de l'amplificateur opérationnel : Inverseur, Non inverseur, Sommateur, Soustracteur, Compateur, Suiveur, Dérivateur, Intégrateur, Logarithmique, Exponentiel, ...

Mode d'évaluation :

Contrôle continu : 40 % ; Examen final : 60 %.

Références bibliographiques:

1. A. Malvino, Principe d'Electronique, 6^{ème} Edition Dunod, 2002.
2. T. Floyd, Electronique Composants et Systèmes d'Application, 5^{ème} Edition, Dunod, 2000.
3. F. Milsant, Cours d'électronique (et problèmes), Tomes 1 à 5, Eyrolles.
4. M. Kaufman, Electronique : Les composants, Tome 1, McGraw-Hill, 1982.
5. P. Horowitz, Traité de l'électronique Analogique et Numérique, Tomes 1 et 2, Publitronelektor, 1996.
6. M. Ouhrouche, Circuits électriques, Presses internationale Polytechnique, 2009.
7. Neffati, Electricité générale, Dunod, 2004
8. D. Dixneuf, Principes des circuits électriques, Dunod, 2007
9. Y. Hamada, Circuits électroniques, OPU, 1993.
10. I. Jelinski, Toute l'Electronique en Exercices, Vuibert, 2000.

Preface

The aim of this first part of the Fundamental Electronics 1 module is to discover the basic laws used in the analysis of electrical circuits and discover fundamental electronic components such as diodes, bipolar transistors and operational amplifiers, some basic functions, understand their operating principles, learn their modeling, be able to the identified ones in a complex electronic diagram and their implementations for the realization of very specific electronic functions.

This work is a collection of courses based on the framework of fundamental electronics 1. It is mainly aimed at students in the second year (L2) of Electronics and Electrical Engineering in the Electronics and Electrical Engineering streams. The objective of this course is to provide students with a basic document that can provide significant support to students and allow them to illustrate all the parts taught in the subject.

To this end, we have set ourselves two main objectives: the first is to provide students with a useful presentation to familiarize themselves with the general concepts of electrical networks, ranging from the PN junction to the operational amplifier. The second objective is to allow them to have a basis that can guide them in acquiring further knowledge in practical electronics in the context of in-depth studies. The course is divided into five chapters.

Firstly we present generalities on the applications of Ohm's and Kirchhoff's laws, and the methods of analysis of DC networks. In the second chapter a study of electrical networks in the form of quadrupole, followed by a study on passive electrical filters. In the third chapter a reminder on semiconductors as an introduction for the PN junction and the junction diode as well as a study of some applications based on diodes. The fourth chapter is devoted to the study of bipolar transistor assemblies in static and dynamic regime. The last chapter deals with the operation of a famous integrated circuit, popular and the most used based on transistors which are operational amplifiers as well as their basic assemblies.

Summary

Chapter I. Continuous regime and fundamental theorems.....	7
1. Definitions	7
2. Tension	9
3. Intensity.....	10
4. Ohm's law for resistors	10
4.1 Dipole Associations.....	10
5. Kirchhoff's laws	12
5. 1 Law of knots	13
5.2 Mesh law.....	13
5.3 Divisor Rules	14
6. Voltage and current sources	15
6.1. Ideal and real voltage sources	15
6.2 Ideal and real current sources	16
7. Fundamental theorems of electrical circuit analysis.....	17
7.1 Mesh method	17
7.2 Knot Method	17
7.3 Principle of superposition	18
8. Thevenin and Norton theorems.....	19
8.1 Thevenin's theorem	19
8.2 Norton's Theorem	20
8.3 Equivalence between Thevenin and Norton representations.....	20
9. Millman's Theorem.....	20
10. Kennelly's Theorem	22
11. Maximum power transfer	26
Chapter II. Quadrupoles and passive filters.....	28
1. Introduction	28
2. Definition of quadrupoles	28
2. Representative matrices of the quadrupoles	28
3. Passive-active quadrupole.....	28
4. Matrix of a quadrupole parameters and equivalent schemes.....	28
4.1. Impedance matrix Z	29
4.2 Admittance matrix Y	30
4.3 Hybrid Matrix H	31
4.4 Transfer Matrix $[T]$	32
5. Representation of quadrupoles in equivalent diagram	34
5.1 Impedance representation.....	34

5.2 Admittance representation.....	34
5.3 Hybrid Representation.....	34
6. Characteristic of a charged quadrupole is attacked by a real source.....	35
6.1 Input impedance.....	35
6.2 Output impedance.....	36
6.3 Voltage gain.....	36
6.4 Current gain.....	36
6.5 Composite voltage gainGVC.....	37
6.6 Composite Current GainGAC.....	37
7.Quadrupole Associations.....	38
7.1 Series-series association.....	38
7.2 Parallel-parallel association.....	39
7.3 Link between impedance and admittance parameters.....	41
7.4 Series-parallel association.....	41
7.5 Cascade (chain) association.....	42
7.6 Link between parameters.....	43
8. Passive Filters.....	43
8.1 The main types of filters.....	44
8.2 Complex transfer function of a filter.....	44
8.3 First Order Low Pass Filter.....	45
8.4 First Order High Pass Filter.....	48
8.5 Bandpass filter.....	50
8.6 Notch filter.....	53
Chapter III Junction Diodes and its Applications.....	56
Objective.....	56
Definitions.....	56
1. Semiconductor.....	56
2. Intrinsic semi-conduction.....	56
3. Doping.....	57
3.1 N-doping.....	57
3.2 P-doping.....	58
3.PN junction.....	58
4. Polarization of the PN junction.....	59
4.1 Reverse biased junction.....	59
4.2 Reverse biased junction.....	60
5. The junction diode.....	60
5.1 Constitution.....	60

5.2 Characteristics of a diode.....	61
5.3 Static resistance.....	62
5.4 Dynamic resistance.....	63
5.5 Diagram equivalent to a real diode.....	64
6. Half-wave rectification.....	65
6.1 Conversion from alternative to positive continuous.....	65
6.2 CONVERSION OF ALTERNATING TO NEGATIVE CONTINUOUS.....	66
8. Transistors dynamic study.....	100
Chapter V: Operational Amplifiers	116
1.Introduction	116
2. Characteristics of an operational amplifier	116
3. A0 voltage amplification	117
4. Differential input impedance Z_{ed}	118
5. Common mode input impedance Z_{ec}	118
6. Output impedance Z_{S0}	119
7. Common mode rejection ratio TRMC.....	120
8. Input offset voltage (Or offset) V_D	121
9. Input offset current I_D	121
10. IP bias current.....	121
3. Differential amplifier	121
3.1. Static study	122
3.1.1 Basic circuits of the operational amplifier.....	122
4. Inverting amplifier.....	125
5. Non-inverting amplifier	126
6. Differential amplifier	127
7. Logarithmic amplifier.....	128
8. Exponential amplifier	129
9. Integrator	129
10. Derivative	130
11. Adder.....	130
12. Comparator.....	131
13. Comparator with hysteresis.....	132

General introduction

This course is intended for students of the second year of the electronics and electrical engineering degree and for those who want to learn the basics of electronics in general. The latter presents a necessary basis for a future electronics engineer. This collection of basic courses is taught by all Algerian universities, it is mainly aimed at students of the second year of Electronics and Electrical Engineering, of the electronics and electrical engineering sectors.

This is fundamental electronics¹, the aim of which is to provide students with a basic document that can provide significant support to students and allow them to illustrate all the parts taught in the subject.

To this end, we have set ourselves two main objectives: the first is to provide students with a useful presentation to familiarize themselves with the general concepts of electrical networks, semiconductors ranging from the NP junction to the operational amplifier. The second objective is to allow them to have a basis that can guide them in acquiring other knowledge in the context of more in-depth studies. The course is divided into five chapters:

In the first chapter generalities on the applications of Ohm's and Kirchhoff's laws, and the methods of analysis of DC networks will be presented. In the second chapter introducing us to the concept of quadrupoles, a study of electrical networks in the form of quadrupole, followed by a study on passive filters will be presented. In the third chapter a reminder on semiconductors as a basic introduction for the PN junction and the junction diode as well as a study of some circuits based on diodes. The fourth chapter is dedicated to the study in static and dynamic regime of bipolar transistors with these different assemblies such as: common emitter, common base and common collector. The last chapter deals with the operation of the most popular and most used integrated circuit: the operational amplifier. Finally, each chapter is crowned with examples of applications so that the student can understand the basic concepts and solve a problem in fundamental electronics in general.

I hope that placing this modest course in the hands of our students can help them to understand and assimilate the main functions of fundamental electronics.

Chapter I. Continuous regime and fundamental theorems

1. Definitions

An electrical component can only function if it is traversed by an electric current. So it must be able to let the electric current in and let it out.

- Terminal

This is the part of an electrical component that can let the electric current in and out. Figure 1. The terminals also allow connections to be made, that is to say, to connect one electrical component to another electrical component.

- Dipole

It is an electrical component that has two terminals. The lamps, the switches, the generators, the batteries, the diodes, the LEDs, the resistances and the engines are dipoles.

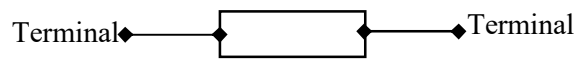


Figure I.1. Dipole

The dipole is the electrical component it has two terminals: an input terminal for the electric current and an output terminal. An electrical component cannot have fewer than two terminals. On the other hand, there are electrical components more complex than dipoles with three, four or more terminals, we then speak of tripoles, quadrupoles, etc. Transistors, transformers, or operational amplifiers are not, for example, dipoles. Each dipole has a simplified representation called standardized symbol. We generally distinguish two types of dipoles:

Active dipole: The generators which can produce electric current.

Passive dipole: Receivers that receive the electric current.

The behavior of a dipole can be described by a characteristic curve either

$$(I.1) I = f(U)$$

or

$$(I.2) U = f(I)$$

There are two types of dipoles: active dipoles and passive dipoles. A dipole is passive if its characteristic passes through zero. The behavior of a dipole is characterized by two dual electrical quantities: voltage and current. The voltage across a dipole represents the potential difference $u(t)$ between the two terminals of the dipole. The voltage is expressed in Volts (V).

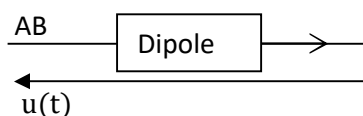


Figure I.2. Voltage across a dipole

$$u(t) = V_A - V_B \quad (I.3)$$

The current flowing through a dipole corresponds to the movement of electric charges under the effect of the electric field induced by the potential difference at the terminals of the dipole. At any time, the current entering through one terminal of a dipole is equal to the current leaving through the other terminal. The intensity $i(t)$ is the flow rate of electric charges flowing through a section of conductor:

$$i(t) = \frac{dq(t)}{dt} \quad (I.4)$$

Intensity is expressed in Amperes (A). Electric current is an oriented quantity. Conventionally, the positive direction corresponds to the direction of movement of positive charges.

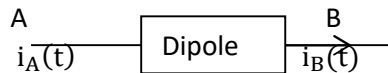


Figure I.3. The current in a dipole

$$i(t) = i_A(t) = i_B(t) \quad (I.5)$$

There are two possibilities for choosing the conventional directions of voltage and current. Depending on whether u and i are in the same direction or not, we have:

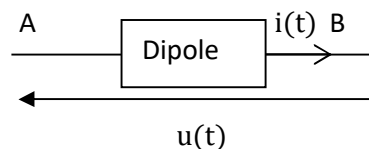


Figure I.4. Receiver

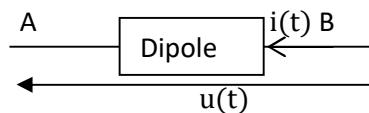


Figure I.5. Generator

In a steady state, independent of time, there is a relationship between the intensity i crossing the dipole and the voltage u between its terminals. This relationship can be put in the form.

$$i = i(u) \quad \text{or} \quad u = u(i)$$

The graphs obtained are called static characteristics:

$i = i(u)$: static current-voltage characteristic of the dipole

$u = u(i)$: static voltage-current characteristic of the dipole

A dipole is passive if its short-circuit current and its open-circuit voltage are zero: its static characteristics pass through the origin. It is said to be active in the opposite case. A dipole is linear if:

$$i(\alpha v_1 + \beta v_2) = \alpha i(v_1) + \beta i(v_2) \quad (I.6)$$

$$u(\alpha i_1 + \beta i_2) = \alpha u(i_1) + \beta u(i_2) \quad (I.7)$$

- **Network**

A network is a set of dipoles connected to each other by wires. drivers of resistance negligible.

- **Node**

In electricity as in electronics, a node is the electrical connection point between several components.

- **Branch**

A branch of a network is a set of dipoles connected in series.

- **Mesh**

A network mesh is a set of branches forming a closed circuit in which each node is encountered only once.

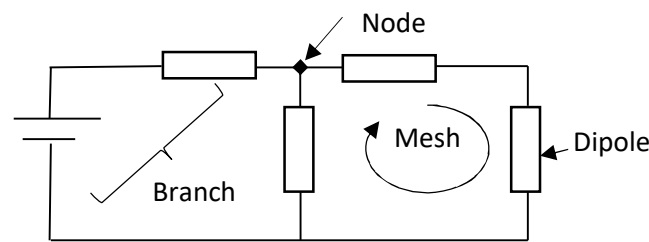


Figure I.6. Electrical network

2. Tension

The electrical voltage between two points of a network is equal to the difference in electrical potential between these two points. The latter is an algebraic quantity, represented by an arrow shown below.

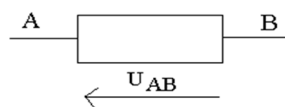


Figure I.7. Voltage across a dipole

If V_A is the potential at point A and the potential at point B then we have: $V_A - V_B$

$$U_{AB} = V_A - V_B \quad (I.8)$$

$$U_{AB} > 0 \Rightarrow V_A > V_B \quad (I.9)$$

$$U_{AB} < 0 \Rightarrow V_A < V_B \quad (\text{I.10})$$

Like electric potential, voltage is expressed in Volts (V).

3.Intensity

Quantity characterizing an electric current, that is to say a movement of all mobile charges in a conductor. The intensity is expressed in Amperes (A). Relationship with other units of the International System: the intensity is linked to the charge crossing a section of the conductor by the relationship: $i(t) q$

$$i(t) = \frac{dq}{dt} \quad (\text{I.11})$$

$i(t)$ in A, in Coulomb (C), in second. $qt(s)$

4. Ohm's law for resistors

The electrical energy produced by the passage of a current I in a resistance is converted by the Joule effect into heat, it is expressed by the relation:

$$P = R \cdot I^2 \quad (\text{I.12})$$

On the other hand, the power consumed is equal to:

$$P = U \cdot I \quad (\text{I.13})$$

Where U denotes the potential difference “ddp” across the resistor; these two powers are equal, we then obtain the following equality:

$$U \cdot I = R \cdot I^2 \quad (\text{I.14})$$

Dividing by I we get:

$$U = R \cdot I \quad (\text{I.15})$$

This last relationship is Ohm's law.

4.1 Dipole Associations

Dipoles are said to be in series if they are traversed by the same intensity of electric current. And they are said to be in parallel if they have the same potential difference at their terminals.

4.1.1 Series connection of resistors

Let there be n resistors connected in series and carrying the same current I (figure 7).

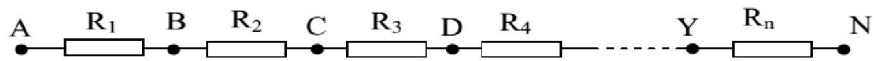


Figure I.8. Series resistors

If we consider that the resistances between A and N behave as a single resistance and as the resistances are in series; then the same current I which passes from A to N therefore we can write: R_{eq}

$$U_{AN} = R_{eq}I \quad (I.16)$$

By applying Ohm's law to each of these resistances we can write the following relationships:

$$U_{AB} = R_1I; U_{BC} = R_2I; U_{CD} = R_3I; U_{DE} = R_4I; \dots; U_{YN} = R_nI;$$

The ddp between the ends A and N i.e. of the circuit is equal to the sum of the ddp between A and B, between B and C, between C and D, ..., and between Y and N. $U_{AN} = U_{AB} + U_{BC} + U_{CD} + \dots + U_{YN}$

$$U_{AN} = R_1I + R_2I + R_3I + R_4I + \dots + R_nI \quad (I.17)$$

$$U_{AN} = (R_1 + R_2 + R_3 + R_4 + \dots + R_n)I \quad (I.18)$$

So by comparison we will have:

$$R_{eq} = R_1 + R_2 + R_3 + R_4 + \dots + R_n \quad (I.19)$$

So we can conclude that the resistances of a branch (connected in series) are equivalent to a single resistance equal to the sum of these resistances of the latter.

4.1.2 Parallel or shunt connection of resistors

Let us place several resistances (for example four resistances, figure 8) between two points N and M. The current I in the circuit creates several derived currents, the intensity of which is equal to the sum of the intensities of these derived currents.

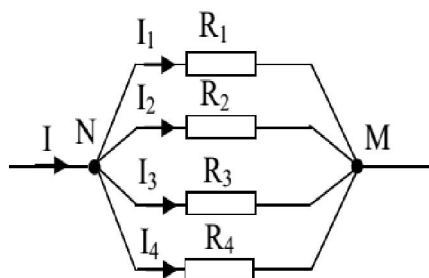


Figure I.9. Resistors in parallel.

If we consider that the resistances between M and N behave like a single resistance, we can write R_{eq} :

$$U_{MN} = R_{eq}I \quad (I.20)$$

SO

$$I = \frac{U_{MN}}{R_{eq}} = \left(\frac{1}{R_{eq}}\right)U_{MN} \quad (I.21)$$

We know that

$$I = I_1 + I_2 + I_3 + I_4 + \dots + I_n \quad (I.22)$$

Applying Ohm's law between nodes M and N to each of the resistors, knowing that the voltage between M and N is constant, we can write the following relations: $R_1; R_2; R_3; R_4; \dots; R_n$

$$U_{MN} = R_1I_1 = R_2I_2 = R_3I_3 = R_4I_4 = \dots = R_nI_n \quad (I.23)$$

$$I_1 = \frac{U_{MN}}{R_1}; I_2 = \frac{U_{MN}}{R_2}; I_3 = \frac{U_{MN}}{R_3}; I_4 = \frac{U_{MN}}{R_4}; \dots \dots; I_n = \frac{U_{MN}}{R_n} \quad (I.24)$$

We replace the values of in the previous equation we will have

$$I = \frac{U_{MN}}{R_1} + \frac{U_{MN}}{R_2} + \frac{U_{MN}}{R_3} + \frac{U_{MN}}{R_4} + \dots + \frac{U_{MN}}{R_n} \quad (I.25)$$

$$I = \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_4} + \dots + \frac{1}{R_n}\right)U_{MN} \quad (I.26)$$

SO

$$\frac{1}{R_{eq}} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_4} + \dots + \frac{1}{R_n} \quad (I.27)$$

From the last relation we can conclude that the inverse of the equivalent resistance is equal to the sum of the inverses of the resistances connected in parallel.

Rating:

The inverse of resistance is known as: conductance we can write the relationship $G \left(G = \frac{1}{R}\right)$.

$$\frac{1}{R_{eq}} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_4} + \dots + \frac{1}{R_n} \quad (I.28)$$

In the following manner using the conductances

$$G_{eq} = G_1 + G_2 + G_3 + G_4 + \dots + G_{eq} \quad (I.29)$$

5. Kirchhoff's laws

An electrical circuit or network is a set of dipoles connected to each other by perfect conducting wires. A node is a point in the circuit connected to two or more dipoles. A network branch is the part of the circuit between two nodes. A mesh is a closed path of branches passing at most once through a given node. Kirchhoff's two laws allow the analysis of electrical networks.

5. 1 Law of knots

At any node of a circuit, and at any instant, the sum of the currents that arrive is equal to the sum of the currents that leave. This is a consequence of the conservation of electric charge.

$$\sum i_{\text{Entrant au noeud}} = \sum i_{\text{Sortant des noeuds}} \quad (\text{I.30})$$

Or else

$$\sum i_{\text{Arrivent au noeud}} = \sum i_{\text{Partent du noeud}} \quad (\text{I.31})$$

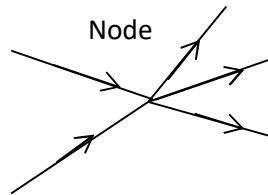


Figure I.10. Currents in a node

The law of nodes can also be written in the following form: At any node of a network the algebraic sum of the currents is zero.

$$\sum_{k=1}^N \pm I_k = 0 \quad (\text{I.32})$$

5.2 Mesh law

Along any mesh of an electrical network, at any time, the algebraic sum of the voltages is zero.

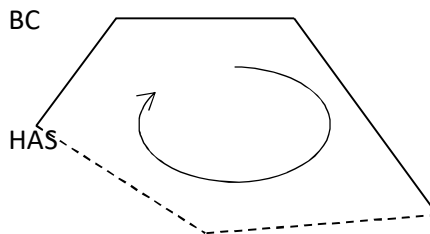


Figure I.11. Tensions in a mesh

$$(V_A - V_B) + (V_B - V_C) + (V_C - V_D) + \dots + (V_7 - V_A) = 0 \quad (\text{I.33})$$

If we call the potential difference

$$(V_A - V_B) = V_1, \dots, (V_B - V_C) = V_2, \dots, (V_7 - V_A) = V_k \quad (\text{I.34})$$

So the law of meshes becomes

$$\sum_{k=1}^N \pm V_k = 0 \quad (\text{I.35})$$

5.3 Divisor Rules

5.3.1 Voltage divider

It is applied to elements in series, crossed by the same current. (R_i)

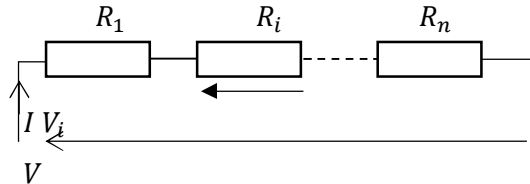


Figure I.12. Voltage divider

We have

$$V = (\sum_{i=1}^n R_i)I \quad (I.36)$$

And

$$V_i = R_i I \quad (I.37)$$

We can deduce the voltage at the terminal from the resistance $V_k R_k$

$$V_k = \frac{R_i}{\sum_{k=1}^n R_k} V \quad (I.38)$$

5.3.2 Current divider

It is applied for elements () in parallel subjected to the same voltage $G_j V$

$G_j = \frac{1}{R_j}$: is the conductance.

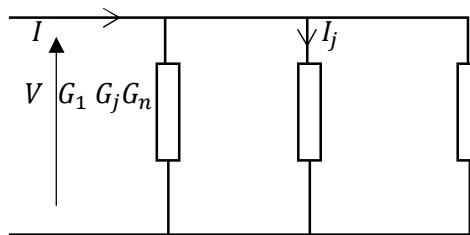


Figure I.13. Current divider

We have

$$I = V(\sum_{k=1}^n G_k) \quad (I.36)$$

And

$$I_j = V G_j \quad (I.37)$$

From the ratio of the last two equations we can deduce the current flowing through the conductance. I_j

$$G_j I_j = \frac{G_j}{(\sum_{k=1}^n G_k)} I \quad (I.38)$$

Or in terms of resistances

$$I_j = \frac{\frac{1}{R_j}}{\left(\sum_{k=1}^n \frac{1}{R_k}\right)} I \quad (\text{I.39})$$

6. Voltage and current sources

6.1. Ideal and real voltage sources

An ideal voltage generator delivers a voltage independent of the current supplied:

$$V_A - V_B = e = \text{constante} \forall I \quad (\text{I.40})$$

i : the current delivered by the voltage source.

This voltage is the electromotive force (emf) of the generator.

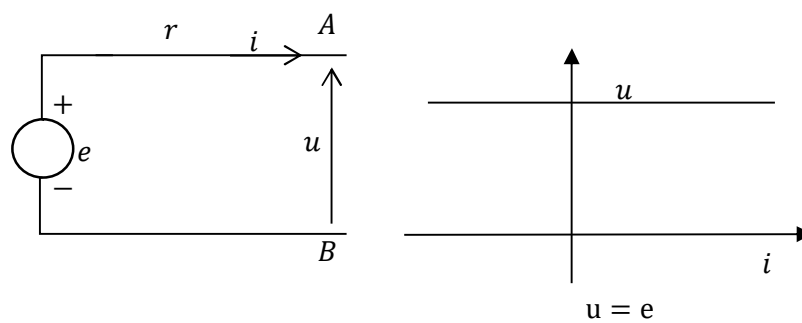


Figure I.14. Ideal generator

The internal resistance of an ideal voltage generator is zero, which is generally not the case for a real generator. A real generator is modeled by an ideal generator in series with its internal resistance. In generator convention, the static voltage-current characteristic of the real voltage generator becomes:

$$u = e - r I \quad (\text{I.41})$$

Internal resistance induces a voltage drop.

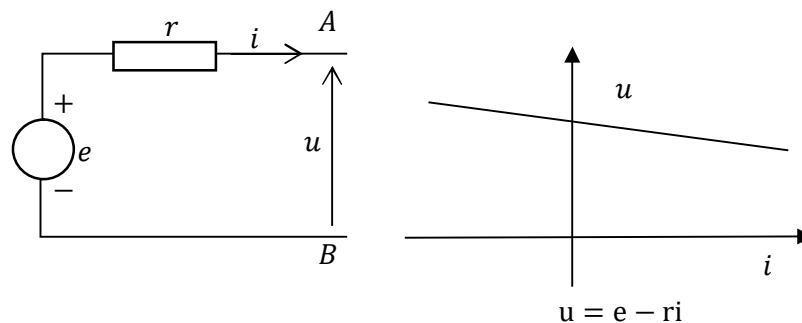


Figure I.15. Real generator

There are two types of voltage sources. An independent, or autonomous, source is a source whose emf value is constant and does not depend on the circuit. A controlled, monitored, or

linked source is a source whose emf value depends on a quantity external to the source, for example a voltage or current of the circuit.

An ideal voltage generator is an example of a polarized dipole: the sign of the emf is independent of that of the current. Depending on the case, it functions as a generator or receiver. Indeed, in notation, generator represents the power delivered to the rest of the circuit by the voltage source. Thus: $p = u i$

$$\text{If, source = generator } i > 0 \Rightarrow p > 0 \quad (\text{I.42})$$

$$\text{If, source = receiver } i < 0 \Rightarrow p < 0 \quad (\text{I.43})$$

6.2 Ideal and real current sources

An ideal current generator delivers a current whose intensity is independent of the voltage across the generator terminals:

$$i = i_S = \text{constante } \forall u \quad (\text{I.44})$$

The following figure shows the symbol of an ideal current source and its current-voltage characteristic.

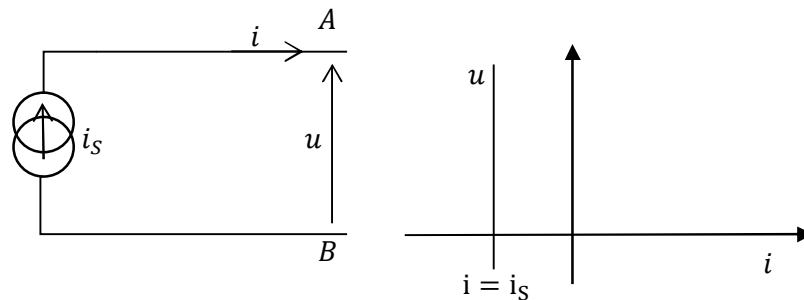


Figure I.16. Ideal current source

The internal resistance of an ideal current source is infinite. For a real generator, its internal resistance is taken into account by modeling it by an ideal current source in parallel with its internal resistance. In generator convention, the static current-voltage characteristic of the real current generator is therefore:

$$i = i_S - \frac{u}{r} \quad (\text{I.45})$$

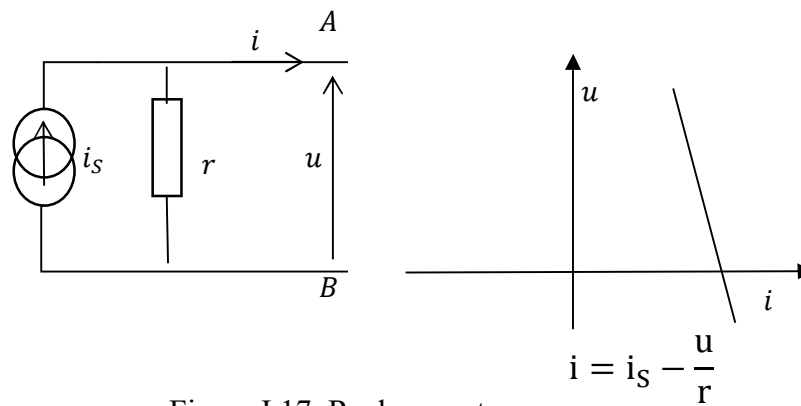


Figure I.17. Real current source

As with voltage sources, we distinguish between independent current sources and controlled current sources which depend on an electrical quantity in the circuit.

7. Fundamental theorems of electrical circuit analysis

Kirchhoff's laws are used to determine the current intensities and the potential differences (ppd) at the terminals of each branch of the electrical network. This operation is called analysis of the circuit or of the electrical network. Since all the constituent elements of the network are known, the complete calculation requires as many equations as branches. The analysis is simplified by the application of associative laws and appropriate theorems.

7.1 Mesh method

It allows to solve the problem by writing M equations to the meshes:

- We choose a system of M independent meshes.
- Each of these meshes is assigned a fictitious current flowing in an arbitrarily chosen direction.
- We apply Kirchhoff's 2nd law to each of these meshes.
- The real current of a given branch is obtained by performing the algebraic sum of the fictitious currents flowing in the branch considered.
- Branch ddps are deduced from actual currents

7.2 Knot Method

Represent by writing N equations at the nodes:

- We choose a reference node (which is most often the ground);

- Each of the remaining nodes is assigned an unknown potential V_1, V_2, \dots, V_N ;
- We write for each of these N nodes Kirchhoff's 1st law.

7.3 Principle of superposition

When it contains only linear dipoles, the response (current and voltage in each branch) of a network comprising several independent sources (voltage and/or current) is equal to the sum of the responses that would be obtained by considering each of these sources separately.

For each of the independent sources, we study the response of the circuit, the other independent sources being "off". On the other hand, the controlled sources always remain active. The principle of superposition is a direct consequence of the linearity of the network.

An ideal "off" voltage source is replaced by a short circuit (\circ). An ideal "off" current source is replaced by an open circuit (\square). $i_s = 0 \forall i_s = 0 \forall u$

Consider a circuit with n dipoles, including N independent voltage or current sources. The electrical state of this circuit, or its response, can be characterized by the set of current intensities flowing through each dipole and the voltages across them:

$$\{R_k = i_k V_k\}_{k=1,n} \quad (I.46)$$

We can calculate N partial states by considering each of the N sources in service only, the others being "off":

$$\{R_k = i_k V_k\}_{k=1,n} \quad (I.47)$$

Each resistance can be characterized by:

For $j=1, N$

$$R^j = \{i_k^j, V_k^j\}_{k=1,n} \quad (I.48)$$

The principle of superposition allows us to write the complete response from the partial states:

$$R = \sum_{j=1}^N R^j \quad (I.49)$$

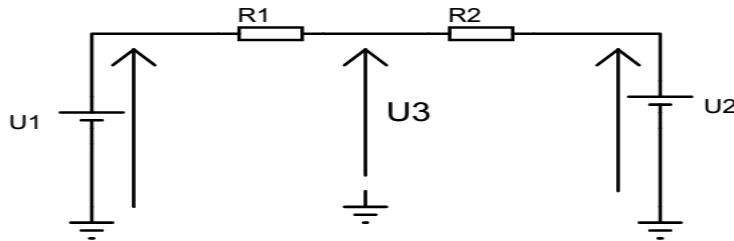
Either :

$$\begin{cases} i_k = \sum_{j=1}^N i_k^j \\ V_k = \sum_{j=1}^N V_k^j \end{cases} \quad \forall k = 1, n \quad (I.50)$$

In another way, for a circuit of n voltage sources (E1 to En), if we want to determine the value of a potential or a potential difference of any kind in the assembly, it is sufficient:

- 1- To calculate the value of this potential taking into account only the source E1. The remaining n-1 sources being extinguished.
- 2- Repeat this operation for each voltage source (n calculations).
- 3- Add all the voltage values calculated in 1 and 2

Example for the circuit below



U1 and U2 known, we wish to determine the voltage U3

The value of the potential U3 can be found in two steps:

- We turn off the source U2 (replaced by a short circuit) and we calculate U31, as a function of U1, R1 and R2.
- We turn off the source U1 (replaced by a short circuit) and we calculate U32, as a function of U2, R1 and R2.

The potential difference U3 is then U31+U32.

8. Thevenin and Norton theorems

8.1 Thevenin's theorem

A linear network, comprising only independent sources of voltage, current and resistances, taken between two terminals behaves like a voltage generator E0 in series with a resistance R0. The emf E0 of the equivalent generator is equal to the voltage existing between the two terminals considered when the network is in open circuit.

The resistance R_0 is that of the circuit seen from the two terminals when all the sources are off.

8.2 Norton's Theorem

Similarly, any linear network, not including controlled sources, taken between two of its terminals can be replaced by a current source I_0 in parallel with a resistance R_0 . The intensity I_0 is equal to the short-circuit current, the two terminals being connected by a perfect conductor. The resistance R_0 is that of the circuit seen from the two terminals when all the sources are off.

8.3 Equivalence between Thevenin and Norton representations

The respective application of Thevenin and Norton's theorems allows us to show the equivalence of the following two circuits:

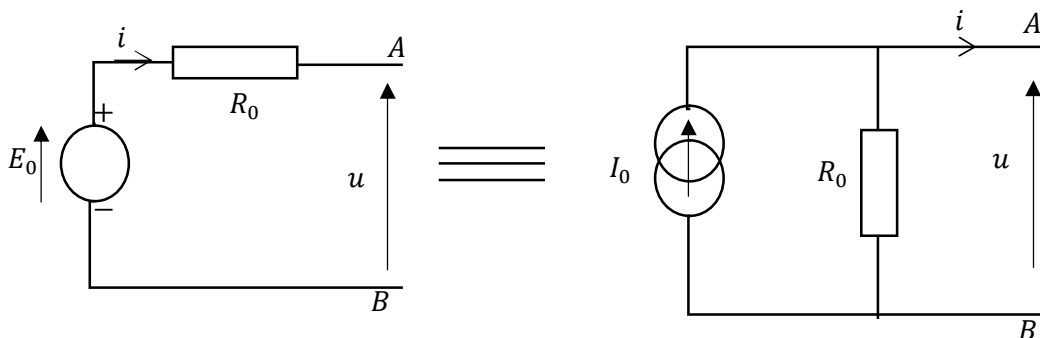


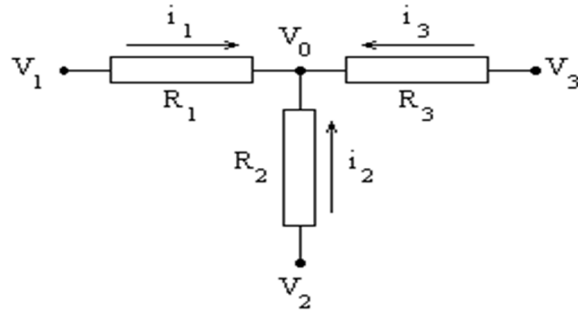
Figure I.18. Thevenin equivalence Norton

With :

$$E_0 = R_0 I_0 \quad (I.51)$$

9. Millman's Theorem

Consider the following circuit:



For each of the branches we can write:

$$\begin{cases} V_1 - V_0 = R_1 I_1 \\ V_2 - V_0 = R_2 I_2 \\ V_3 - V_0 = R_3 I_3 \end{cases} \quad (I.52)$$

Or again:

$$\begin{cases} I_1 = \frac{V_1 - V_0}{R_1} \\ I_2 = \frac{V_2 - V_0}{R_2} \\ I_3 = \frac{V_3 - V_0}{R_3} \end{cases} \quad (I.53)$$

By adding up these relations we get:

$$I_1 + I_2 + I_3 = \frac{V_1 - V_0}{R_1} + \frac{V_2 - V_0}{R_2} + \frac{V_3 - V_0}{R_3} \quad (I.54)$$

Now we have: , therefore: $I_1 + I_2 + I_3 = 0$

$$V_0 \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right) = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \quad (I.55)$$

Or

$$V_0 = \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}} \quad (I.56)$$

This result generalizes to any number of branches:

$$V_0 = \frac{\sum_1^n \frac{V_k}{R_k}}{\frac{1}{R_k}} = \frac{\sum_1^n G_k V_k}{\sum_1^n G_k} \quad (I.57)$$

The voltage at the node is the average of the voltages across all dipoles weighted by the respective conductances.

10. Kennelly's Theorem

Presentation of the assemblies in the form of a triangle (left) and a star (right). Kennelly's theorem, or triangle-star transformation, or Y- Δ transformation, or T-II transformation, is a mathematical technique that simplifies the study of certain electrical networks.

This theorem, named in homage to Arthur Edwin Kennelly, allows you to move from a "triangle" configuration (or Δ , or Π , depending on how you draw the diagram) to a "star" configuration (or, similarly, Y or T). The diagram opposite is drawn in the "triangle-star" form; the diagrams below in the T-II form.

This theorem is used in electrical engineering or in power electronics in order to simplify three-phase systems. It is also commonly used in electronics to simplify the calculation of filters or attenuators. The two circuits in Figure 17 are equivalent if the values of their resistances are related by the relationships shown below.

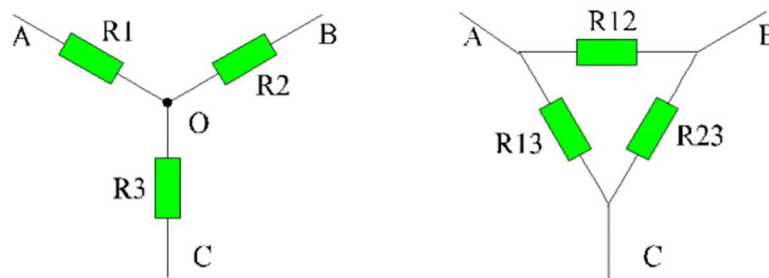


Figure I.19. Star-rod equivalence or Pi-Ti

The transition from the triangle structure (ABC) to the star structure (OABC) is obtained by the relations:

If we disconnect point A, there must be equality of impedances between B and C.

$$R_2 + R_3 = \frac{R_a(R_b + R_c)}{R_a + R_b + R_c} \quad (\text{I.58})$$

We draw the following three equalities:

$$R_2 + R_3 = \frac{R_a(R_b + R_c)}{R_a + R_b + R_c} \quad (\text{I.59})$$

$$R_2 + R_1 = \frac{R_c(R_a + R_b)}{R_a + R_b + R_c} \quad (\text{I.60})$$

$$R_1 + R_3 = \frac{R_b(R_a + R_c)}{R_a + R_b + R_c} \quad (\text{I.61})$$

By adding the first two equalities and subtracting the third, we deduce:

$$R_1 = \frac{R_b R_c}{R_a + R_b + R_c} \quad (\text{I.62})$$

$$R_2 = \frac{R_a R_c}{R_a + R_b + R_c} \quad (\text{I.63})$$

$$R_3 = \frac{R_b R_a}{R_a + R_b + R_c} \quad (\text{I.64})$$

For the inverse transformation, we connect B and C: the conductance between A and BC is then written:

$$\frac{1}{Z_a} = \frac{1}{R_c} + \frac{1}{R_b} = \frac{R_2 + R_3}{R_1 R_2 + R_2 R_3 + R_1 R_3} \quad (\text{I.65})$$

$$\frac{1}{Z_b} = \frac{1}{R_a} + \frac{1}{R_c} = \frac{R_1 + R_3}{R_1 R_2 + R_2 R_3 + R_1 R_3} \quad (\text{I.66})$$

$$\frac{1}{Z_c} = \frac{1}{R_a} + \frac{1}{R_b} = \frac{R_1 + R_2}{R_1 R_2 + R_2 R_3 + R_1 R_3} \quad (\text{I.67})$$

And we calculate

$$\frac{1}{Z_a} = \frac{1}{Z_b} - \frac{1}{Z_c} \quad (\text{I.68})$$

He comes

$$\frac{2}{R_b} = \frac{2R_2}{R_1 R_2 + R_2 R_3 + R_1 R_3} \quad (\text{I.69})$$

Either

$$R_b = \frac{R_1 R_2 + R_2 R_3 + R_1 R_3}{R_2} \quad (\text{I.70})$$

Similarly we can also write that:

$$R_c = \frac{R_1 R_2 + R_2 R_3 + R_1 R_3}{R_3} \quad (\text{I.71})$$

$$R_a = \frac{R_1 R_2 + R_2 R_3 + R_1 R_3}{R_1} \quad (\text{I.72})$$

This theorem is used to transform networks in triangle form (Pi) to star form (T) and vice versa (figure 16).

1) Triangle \rightarrow star transformation ($\Delta \rightarrow Y$)

$$R_1 = \frac{R_b R_c}{R_a + R_b + R_c} \quad (\text{I.73})$$

$$R_2 = \frac{R_a R_c}{R_a + R_b + R_c} \quad (I.74)$$

$$R_3 = \frac{R_b R_a}{R_a + R_b + R_c} \quad (I.75)$$

2) Star \rightarrow triangle transformation ($Y \rightarrow \Delta$)

$$R_b = \frac{R_1 R_2 + R_2 R_3 + R_1 R_3}{R_2} \quad (I.76)$$

$$R_c = \frac{R_1 R_2 + R_2 R_3 + R_1 R_3}{R_3} \quad (I.77)$$

$$R_a = \frac{R_1 R_2 + R_2 R_3 + R_1 R_3}{R_1} \quad (I.78)$$

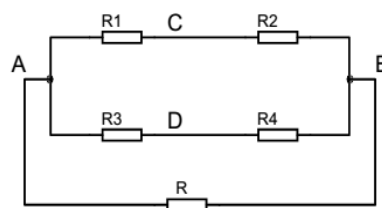
Exercise

This network represents the passive elements of a Wheatstone bridge, in the case where the internal resistance of the power supply is not negligible. Calculate the equivalent resistance to the network:

a) seen from **A** and **B**

b) seen from **C** and **D**

Digital application: $R_1 = R_2 = R_3 = R_4 = 350\Omega$, $R = 50\Omega$



Quick solution

a) Three branches connect **A** and **B**:

- a branch containing two resistance dipoles, in series. R_1 et R_2
- a branch containing two other resistance dipoles, in series. R_3 et R_4
- a branch containing a resistance dipole. R

The first branch has equivalent resistance $R_{12} = R_1 + R_2 = 700\Omega$

The second branch has equivalent resistance, the conductances are added:

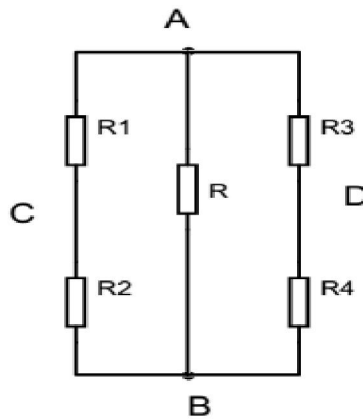
$$G_{AB} = G_{12} + G_{34} + G$$

$$\frac{1}{R_{AB}} = \frac{1}{R_{12}} + \frac{1}{R_{34}} + \frac{1}{R} = \frac{1}{700} + \frac{1}{700} + \frac{1}{50}$$

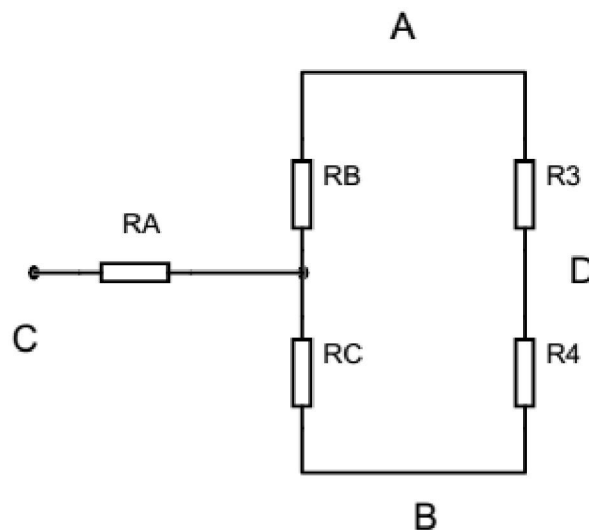
$$R_{AB} = 43,75\Omega$$

$$R_{AB} = 43,75$$

b) To go from C to D we can go either through A or B; A and B are connected by a branch containing a dipole of resistance R. We can redraw the network as follows:



To calculate the resistance of the network seen from C and D, we transform one of the triangles into a star, for example ABC.



According to Kennelly's theorem.

$$R_C = \frac{R_1 R_2}{R_1 + R_2 + R} = 163,3\Omega$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2 + R} = 23,3\Omega$$

$$R_A = \frac{R_1 R}{R_1 + R_2 + R} = 23,3\Omega$$

The dipoles in series are replaced by their equivalent resistance

$$R_{A3} = R_A + R_3 = 373,3\Omega$$

$$R_{B4} = R_B + R_4 = 373,3\Omega$$

$$G_{A3B4} = G_{A3} + G_{B4}$$

$$\frac{1}{R_{A3B4}} = \frac{1}{R_{A3}} + \frac{1}{R_{B4}}$$

$$R_{A3B4} = 186,7\Omega$$

And we apply the law of serial association.

$$R_{CD} = R_C + R_{A3B4} = 350\Omega$$

11. Maximum power transfer

If we consider a circuit containing sources and passive elements (impedances); we can represent it by a voltage source which is the Thevenin generator and a resistance or Thevenin impedance as shown in the figure below.

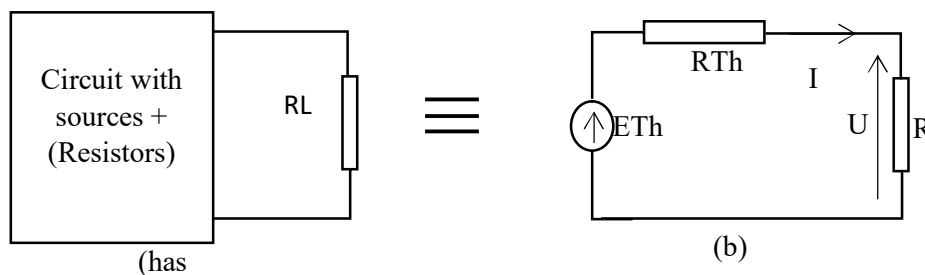


Figure I.20. Thevenin equivalence

To calculate the condition for which there will be a maximum power transfer for the circuit Figure (a) we use its Thevenin equivalent; then the current absorbed by the load will be:

$$I = \frac{E_{Th}}{R_{Th} + R_L} \quad (I.79)$$

So the power consumed by the load is:

$$U = R_L I \quad (I.80)$$

$$P = U.I = R_L I^2 = R_L \left(\frac{E_{th}}{R_{Th} + R_L} \right)^2 \quad (I.81)$$

To calculate when the maximum power is transferred one must calculate the maximum power i.e.:

$$\frac{dP}{dR_L} = \left(\frac{E_{th}}{R_{Th} + R_L} \right)^2 + 2R_L \left(\frac{E_{th}}{R_{Th} + R_L} \right) \left(\frac{-E_{th}}{(R_{Th} + R_L)^2} \right) \quad (I.82)$$

$$\frac{dP}{dR_L} = \left(\frac{E_{th}^2 (R_{Th} + R_L) - 2R_L E_{th}^2}{(R_{Th} + R_L)^3} \right) \quad (I.83)$$

$$\frac{dP}{dR_L} = 0 \Rightarrow \left(\frac{E_{th}^2 (R_{Th} + R_L) - 2R_L E_{th}^2}{(R_{Th} + R_L)^3} \right) = 0 \Rightarrow$$

$$E_{th}^2 (R_{Th} + R_L) - 2R_L E_{th}^2 = E_{th}^2 (R_{Th} - R_L) = 0 \Rightarrow$$

$$R_{Th} - R_L = 0 \Rightarrow R_{Th} = R_L \quad (I.84)$$

It can be concluded that there will be maximum power transfer to the load when $R_{Th} = R_L$

In this case we will have

$$P_{max} = R_L \left(\frac{E_{th}}{R_{Th} + R_L} \right)^2 = R_L \left(\frac{E_{th}}{R_L + R_L} \right)^2 = R_L \left(\frac{E_{th}}{2R_L} \right)^2 = \frac{E_{th}^2}{4R_L} \quad (I.85)$$

$$\Rightarrow P_{max} = \frac{E_{th}^2}{4R_L} \quad (I.86)$$

Chapter II. Quadrupoles and passive filters

1. Introduction

The second chapter is divided into two parts: The first is devoted to quadrupoles, definitions, the different matrices representing a quadrupole as well as the fundamental parameters such as the input and output impedance, the voltage and current gains. The second part is a representation of the different filters following a detailed study on each type of filter.

2. Definition of quadrupoles

A quadrupole is an electrical circuit consisting of a number of passive and active elements with four terminals, hence its name. It has two input terminals and two output terminals:

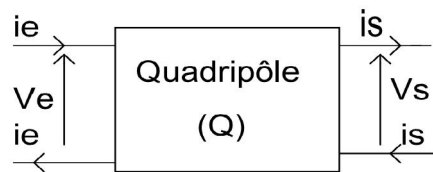


Figure II.1. Representative diagram of a quadrupole

The quadrupole is characterized by four electrical parameters: input voltage and current and , and output voltage and current and . Two of these variables are independent. The others are linked to them by the parameters of the quadrupole. Under normal conditions of use, the quadrupole (Q) is driven at the input by a voltage source and its internal impedance and closed at the output on a load of impedance $V_e I_e V_s I_s Z_g Z_u$

2. Representative matrices of the quadrupoles

The variables V_e, I_e, V_s, I_s are related to each other by equations and form several types of matrices, which are used to represent the quadrupoles. The choice of the type of matrix is determined by the conditions of the problem studied. $V_s I_e I_s$

3. Passive-active quadrupole

A quadrupole is said to be passive if it does not contain any energy source, it only contains passive RLC elements. A quadrupole is said to be active if it contains at least one energy source.

4. Matrix of a quadrupole parameters and equivalent schemes

If we consider the quadrupole in the figure below

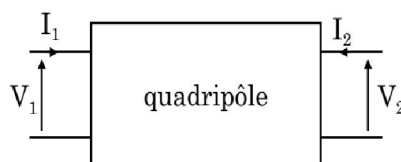


Figure II.2. Conventional representation of a quadropole

The main advantage of the quadropole representation is that it considerably simplifies the study of electronic circuits.

4.1. Impedance matrix[Z]

The input and output voltages are expressed as a function of the input and output currents. The elements of the matrix have the dimension of impedances. The voltages are expressed as a function of the currents. The elements of the matrix have the dimension of impedances (resistances).

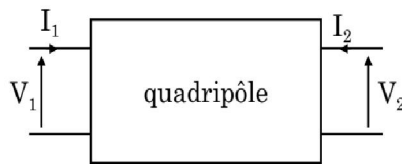


Figure II.3. Quadropole impedance

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = [Z] \times \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \times \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \Rightarrow \begin{cases} V_1 = Z_{11}I_1 + Z_{12}I_2 \\ V_2 = Z_{21}I_1 + Z_{22}I_2 \end{cases} \text{(II.1)}$$

$Z_{11} = \left(\frac{V_1}{I_1} \right)_{I_2=0}$: This is the input impedance with open circuit output.

$Z_{12} = \left(\frac{V_1}{I_2} \right)_{I_1=0}$: This is the reverse transfer impedance with the input open circuit.

$Z_{21} = \left(\frac{V_2}{I_1} \right)_{I_2=0}$: This is the direct transfer impedance with the output open circuit.

$Z_{22} = \left(\frac{V_2}{I_2} \right)_{I_1=0}$: This is the output impedance with the input open circuit.

Example

Calculate the parameters of the following quadropole[Z]

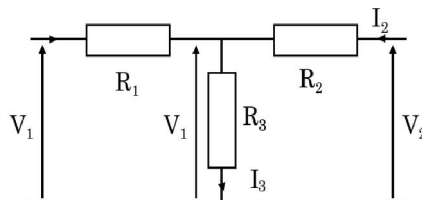


Figure II.4. Quadropole impedance

Answer

We have

$$\begin{cases} V_1 = Z_{11}I_1 + Z_{12}I_2 \\ V_2 = Z_{21}I_1 + Z_{22}I_2 \end{cases}$$

1. First case: $I_1 = 0$

$$\begin{cases} V_1 = Z_{12}I_2 = R_3I_2 \\ V_2 = Z_{22}I_2 = (R_2 + R_3)I_2 \end{cases}$$

$$\begin{cases} Z_{12} = R_3 \\ Z_{22} = (R_3 + R_2) \end{cases}$$

2. First case: $I_2 = 0$

$$\begin{cases} V_1 = Z_{11}I_1 = (R_1 + R_3)I_1 \\ V_2 = Z_{21}I_1 = R_3I_1 \end{cases}$$

$$\begin{cases} Z_{11} = (R_3 + R_2) \\ Z_{21} = R_3 \end{cases}$$

The matrix is therefore $[Z]$

$$[Z] = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} (R_1 + R_3) & R_3 \\ R_3 & (R_3 + R_2) \end{bmatrix}$$

4.2 Admittance matrix $[Y]$

Currents are expressed as a function of voltages. The elements of the matrix have the dimension of admittances.

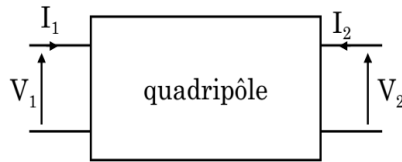


Figure II.5. Quadripole admittance

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = [Y] \times \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \times \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \Rightarrow \begin{cases} V_1 = Y_{11}V_1 + Y_{12}V_2 \\ V_2 = Y_{21}V_1 + Y_{22}V_2 \end{cases} \text{(II.2)}$$

$Y_{11} = \left(\frac{I_1}{V_1} \right)_{V_2=0}$: This is the input admittance with shorted output.

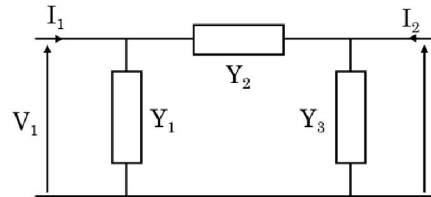
$Y_{12} = \left(\frac{I_1}{V_2} \right)_{V_1=0}$: This is the direct transfer admittance with the input shorted.

$Y_{21} = \left(\frac{I_2}{V_1} \right)_{V_2=0}$: This is the reverse transfer admittance with the output shorted.

$Y_{22} = \left(\frac{I_2}{V_2} \right)_{V_1=0}$: This is the output admittance with the input shorted.

Example

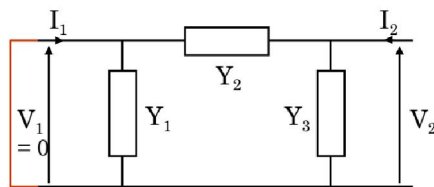
Calculate the admittance matrix for the quadropole in the figure below



Answer

$$\begin{cases} I_1 = Y_{11}V_1 + Y_{12}V_2 \\ I_2 = Y_{21}V_1 + Y_{22}V_2 \end{cases}$$

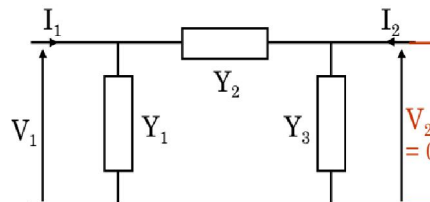
1. First case: $V_1 = 0$



$$\begin{cases} I_1 = Y_{12}V_2 = (Y_2 + Y_3)V_2 \\ I_2 = Y_{22}V_2 = -Y_2V_2 \end{cases}$$

$$\begin{cases} Y_{12} = (Y_2 + Y_3) \\ Y_{22} = -Y_2 \end{cases}$$

2. First case: $V_2 = 0$



$$\begin{cases} I_1 = Y_{11}V_1 = (Y_1 + Y_2)V_1 \\ I_2 = Y_{21}V_1 = -Y_2V_1 \end{cases}$$

$$\begin{cases} Y_{11} = (Y_1 + Y_2) \\ Y_{21} = -Y_2 \end{cases}$$

The matrix is therefore $[Y]$

$$[Y] = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} (Y_1 + Y_2) & -Y_2 \\ -Y_2 & (Y_2 + Y_3) \end{bmatrix}$$

4.3 Hybrid Matrix[H]

The output current and input voltage are expressed as a function of the input current and output voltage. This is a representation commonly used in the study of transistors.

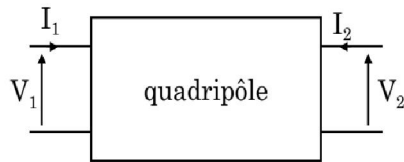


Figure II.6. Hybrid Quadrupole

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = [H] \times \begin{bmatrix} I_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \times \begin{bmatrix} I_1 \\ V_2 \end{bmatrix} \Rightarrow \begin{cases} V_1 = h_{11}I_1 + h_{12}V_2 \\ I_2 = h_{21}I_1 + h_{22}V_2 \end{cases} \text{(II.3)}$$

$h_{11} = \left(\frac{V_1}{I_1}\right)_{V_2=0}$: This is the input impedance with shorted output.

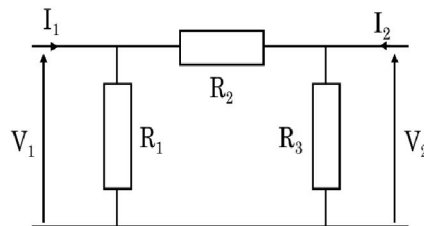
$h_{12} = \left(\frac{V_1}{V_2}\right)_{I_1=0}$: This is the reverse voltage gain with the input open circuit.

$h_{21} = \left(\frac{I_2}{I_1}\right)_{V_2=0}$: This is the forward current gain with the output shorted.

$h_{22} = \left(\frac{I_2}{V_2}\right)_{I_1=0}$: This is the output admittance with the input open circuit.

Example

Calculate the hybrid parameters of the following quadrupole[H]



Answer

$$\begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} = \begin{bmatrix} \frac{R_1 \cdot R_2}{R_1 + R_2} & \frac{R_1}{R_1 + R_2} \\ -R_1 & \frac{R_1 + R_2 + R_3}{(R_1 + R_2) \cdot R_3} \end{bmatrix}$$

4.4 Transfer Matrix [T]

The output current and input voltage are expressed as a function of the input current and output voltage. This is a representation commonly used in the study of transistors.

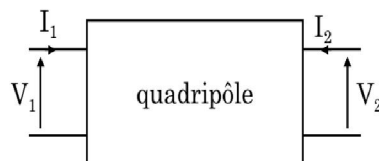


Figure II.7. Transfer quadrupole [T]

$$\begin{bmatrix} V_2 \\ I_2 \end{bmatrix} = [H] \times \begin{bmatrix} V_1 \\ -I_1 \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \times \begin{bmatrix} V_1 \\ I_1 \end{bmatrix} \Rightarrow \begin{cases} V_2 = T_{11}V_1 - T_{12}I_1 \\ I_2 = T_{21}V_1 - T_{22}I_1 \end{cases} \quad (\text{II.4})$$

$T_{11} = \left(\frac{V_2}{V_1}\right)_{I_1=0}$: This is the voltage gain with the output open circuit.

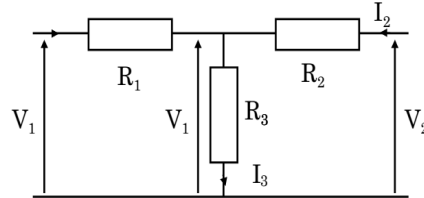
$T_{12} = \left(\frac{V_2}{I_1}\right)_{V_1=0}$: This is the transfer impedance with the input shorted.

$T_{21} = \left(\frac{I_2}{V_1}\right)_{I_1=0}$: This is the direct admittance with the output short-circuited.

$T_{22} = \left(\frac{I_2}{I_1}\right)_{V_1=0}$: This is current gain with the input shorted.

Example

Calculate the parameters of the following quadrupole[T]



Answer

We have

$$\begin{cases} V_2 = T_{11}V_1 - T_{12}I_1 \\ I_2 = T_{21}V_1 - T_{22}I_1 \end{cases}$$

First case: $V_1 = 0$

$$\begin{cases} V_2 = T_{12}I_1 = \left(R_1 + R_2 + \frac{R_1R_2}{R_3}\right)I_1 \\ I_2 = T_{22}I_1 = \frac{1}{R_3}(R_1 + R_3)I_1 \end{cases}$$

$$\begin{cases} T_{12} = \left(R_1 + R_2 + \frac{R_1R_2}{R_3}\right) \\ T_{22} = \left(1 + \frac{R_1}{R_3}\right) \end{cases}$$

1. First case: $I_1 = 0$

$$\begin{cases} V_2 = T_{11}V_1 = \left(1 + \frac{R_2}{R_3}\right)V_1 \\ I_2 = T_{21}V_1 = \left(\frac{1}{R_3}\right)V_1 \end{cases} \begin{cases} T_{11} = \left(1 + \frac{R_2}{R_3}\right) \\ T_{21} = \left(\frac{1}{R_3}\right) \end{cases}$$

The matrix is therefore:[T]

$$[T] = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} = \begin{bmatrix} \left(1 + \frac{R_2}{R_3}\right) & \left(R_1 + R_2 + \frac{R_1 R_2}{R_3}\right) \\ \left(\frac{1}{R_3}\right) & \left(1 + \frac{R_1}{R_3}\right) \end{bmatrix}$$

5. Representation of quadrupoles in equivalent diagram

5.1 Impedance representation

It is sometimes convenient to replace the quadrupole studied by its equivalent scheme given by the quadrupole matrix. Knowledge of this equivalent scheme is particularly useful when the real network is not known and the determination of the parameters results from measurements.

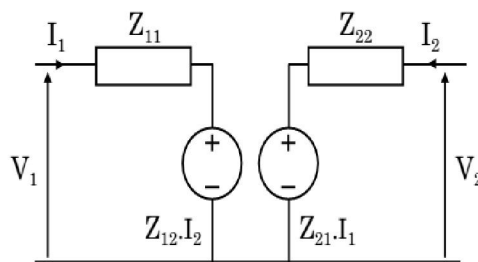


Figure II.8. Representation of a quadrupole in impedance

5.2 Admittance representation

Equivalent diagram with admittances and current sources

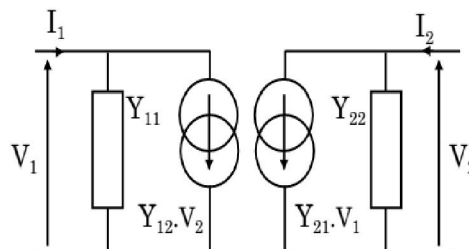


Figure II.9. Representation of a quadrupole in admittance

5.3 Hybrid Representation

The equivalent circuit is composed of an impedance (h_{11}), an admittance (h_{22}), a voltage source ($h_{12} \cdot V_2$) and a current source ($h_{21} \cdot I_1$).

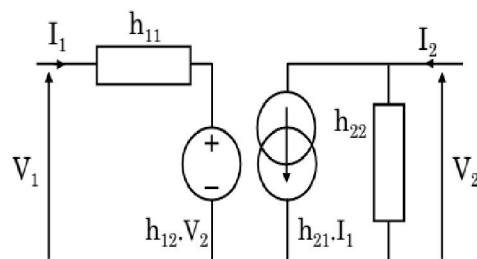


Figure II.10. Representation of a quadrupole in hybrid parameters

6. Characteristic of a charged quadrupole is attacked by a real source.

To characterize a quadrupole, connect a source dipole () to the two input terminals. To the two output terminals, we connect a load dipole denoted as shown in the figure below. E_G, R_G, Z_L

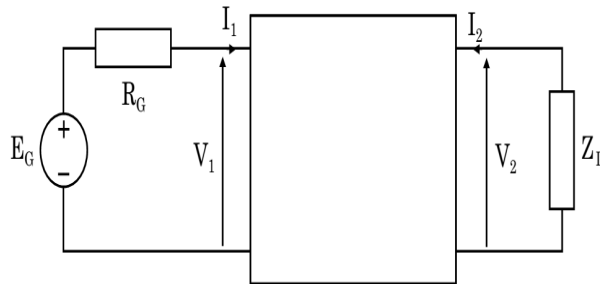


Figure II.11. Quadripole under load attacked by a real voltage source.

For example we define a quadrupole by the matrix , the equations which allow the determination of the state of the network are: $Q[Z]$

$$V_1 = Z_{11}I_1 + Z_{12}I_2$$

$$V_2 = Z_{21}I_1 + Z_{22}I_2$$

$$E_G = V_1 + R_G I_1$$

$$V_2 = -Z_L I_2$$

6.1 Input impedance

The input impedance is the impedance seen by the source driving the quadrupole when empty or loaded.

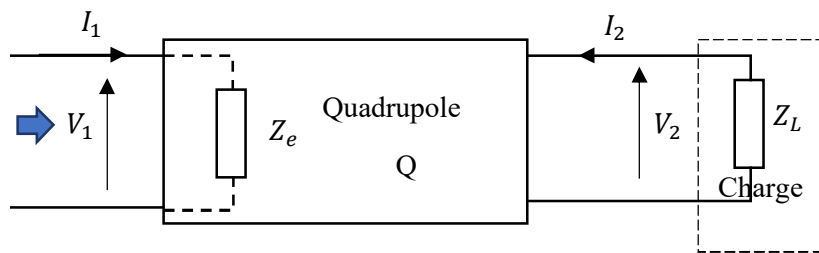


Figure II.12. The input impedance of a quadrupole.

The input impedance is given by:

$$Z_e = \frac{V_1}{I_1} \tag{II.5}$$

If we use the previous equations relating to the parameters we find $[Z]$

$$Z_e = \frac{Z_L Z_{11} + \Delta Z}{Z_L + Z_{22}} \tag{II.6}$$

Where is the determinant of the matrix. $\Delta Z [Z]$

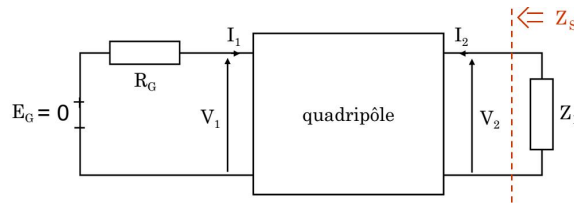
$$\Delta Z = Z_{11}Z_{22} - Z_{12}Z_{21} \quad (\text{II.7})$$

6.2 Output impedance

The impedance is expressed by the relation:

$$Z_s = \left. \frac{V_2}{I_2} \right|_{E_G=0} \quad (\text{II.8})$$

This is the impedance seen at the output when the input is closed by an impedance, which is the impedance of the generator. A calculation similar to the previous case gives: R_G



$$\begin{aligned} V_1 &= Z_{11}I_1 + Z_{12}I_2 = -R_G I_1 \\ V_2 &= Z_{21}I_1 + Z_{22}I_2 \\ Z_s &= \frac{V_2}{I_2} \end{aligned}$$

We obtain by analogy to the previous one the output impedance:

$$Z_s = \frac{R_G Z_{22} + \Delta Z}{R_G + Z_{11}} \quad (\text{II.9})$$

6.3 Voltage gain

The voltage gain is defined by the ratio between the output voltage and the input voltage, i.e.:

$$G_V = \frac{V_2}{V_1} \quad (\text{II.10})$$

If the quadripole is defined by the parameters and by the use of the equations [Z]

$$\begin{aligned} V_1 &= Z_{11}I_1 + Z_{12}I_2 \\ V_2 &= Z_{21}I_1 + Z_{22}I_2 \\ V_2 &= -Z_L I_2 \end{aligned}$$

We obtain:

$$G_V = \frac{Z_{21}Z_L}{Z_{11}Z_L + \Delta Z} \quad (\text{II.11})$$

6.4 Current gain

Current gain is defined by the ratio of output current to input current I_2 / I_1

$$G_A = \frac{I_2}{I_1} \quad (\text{II.12})$$

If the quadrupole is defined by the parameters and by using the equations and using the equations: [Z]

$$V_2 = Z_{21}I_1 + Z_{22}I_2$$

$$V_2 = -Z_L I_2$$

We obtain:

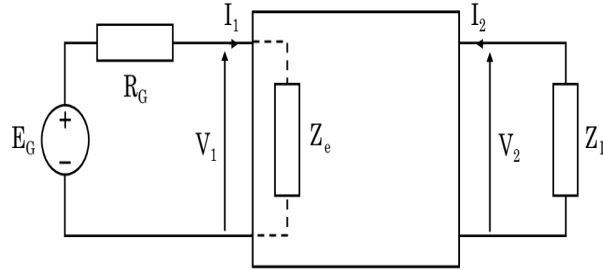
$$G_A = -\frac{Z_{21}}{Z_{22} + \Delta Z} \quad (\text{II.13})$$

6.5 Composite voltage gain G_{VC}

The composite voltage gain is defined as the ratio of the output voltage to the source voltage: $V_2 E_G$

$$G_{VC} = \frac{V_2}{E_G} \quad (\text{II.14})$$

If we replace the quadrupole with its equivalent as shown in the figure below



If we multiply the nominator and the denominator by V_1

$$G_{VC} = \frac{V_2}{E_G} \times \frac{V_1}{V_1} = \frac{V_2 V_1}{V_1 E_G} = G_V \times \frac{V_1}{E_G}$$

We use input mesh and the voltage divider will have:

$$V_1 = E_G \times \frac{Z_e}{R_G + Z_e}$$

We replace this last equation in the previous equation we will have:

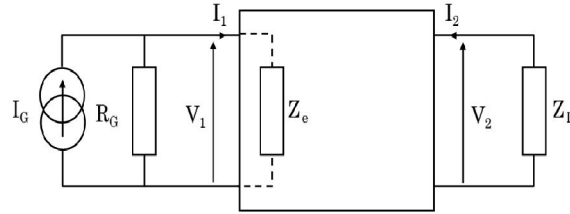
$$G_{VC} = G_V \times \frac{Z_e}{R_G + Z_e} \quad (\text{II.15})$$

6.6 Composite Current Gain G_{AC}

The composite current gain is defined as the ratio of the output current to the current delivered by the source: $I_2 I_G$

$$G_{VC} = \frac{I_2}{I_G} \quad (II.16)$$

If we replace the quadrupole with its equivalent by changing the voltage source with a current source using Norton's theorem as shown in the figure below.



If we multiply the nominator and the denominator by I_1

$$G_{AC} = \frac{I_2}{I_G} \times \frac{I_1}{I_1} = \frac{V_2 I_1}{I_1 I_G} = G_A \times \frac{I_1}{I_G}$$

We use input mesh and the voltage divider will have:

$$I_1 = I_G \times \frac{R_G}{R_G + Z_e}$$

We replace this last equation in the previous equation we will have:

$$G_{AC} = G_A \times \frac{R_G}{R_G + Z_e} \quad (II.17)$$

This gain only makes sense if the load is present: $I_2 \neq 0$

7. Quadrupole Associations

7.1 Series-series association

Let the two quadrupoles and having the respective impedance matrices and which are connected in series-series as shown in the figure below. $Q'Q''[Z'][Z'']$

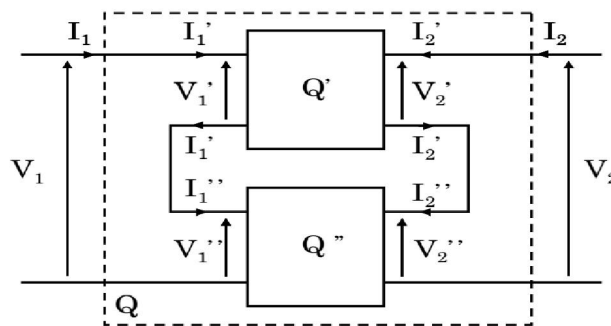


Figure II.13. Quadrupole associated in series-series

We use the impedance matrices and the two associated quadrupoles. $[Z'][Z'']$

$$[Z'] = \begin{bmatrix} Z_{11}' & Z_{12}' \\ Z_{21}' & Z_{22}' \end{bmatrix} \quad (II.18)$$

$$[Z''] = \begin{bmatrix} Z_{11}'' & Z_{12}'' \\ Z_{21}'' & Z_{22}'' \end{bmatrix} \quad (\text{II.19})$$

SO

$$\begin{bmatrix} V_1' \\ V_2' \end{bmatrix} = [Z'] \times \begin{bmatrix} I_1' \\ I_2' \end{bmatrix} = \begin{bmatrix} Z_{11}' & Z_{12}' \\ Z_{21}' & Z_{22}' \end{bmatrix} \times \begin{bmatrix} I_1' \\ I_2' \end{bmatrix} \quad (\text{II.20})$$

$$\begin{bmatrix} V_1'' \\ V_2'' \end{bmatrix} = [Z''] \times \begin{bmatrix} I_1'' \\ I_2'' \end{bmatrix} = \begin{bmatrix} Z_{11}'' & Z_{12}'' \\ Z_{21}'' & Z_{22}'' \end{bmatrix} \times \begin{bmatrix} I_1'' \\ I_2'' \end{bmatrix} \quad (\text{II.21})$$

As

$$\begin{cases} I_1 = I_1' = I_1'' \\ I_2 = I_2' = I_2'' \end{cases} \text{and} \begin{cases} V_1 = V_1' + V_1'' \\ V_2 = V_2' + V_2'' \end{cases} \quad (\text{II.22})$$

SO

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} V_1' \\ V_2' \end{bmatrix} + \begin{bmatrix} V_1'' \\ V_2'' \end{bmatrix} \quad (\text{II.23})$$

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = [Z'] \times \begin{bmatrix} I_1' \\ I_2' \end{bmatrix} + [Z''] \times \begin{bmatrix} I_1'' \\ I_2'' \end{bmatrix} \quad (\text{II.24})$$

$$= [Z'] \times \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} + [Z''] \times \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

$$= ([Z'] + [Z'']) \times \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \Rightarrow$$

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = [Z] \times \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \Rightarrow$$

SO

$$[Z] = [Z'] + [Z''] \quad (\text{II.25})$$

7.2 Parallel-parallel association

Let the two quadrupoles and having the admittance matrices and respectively are mounted in parallel-parallel as shown in the figure below. Q'Q''[Y][Y']

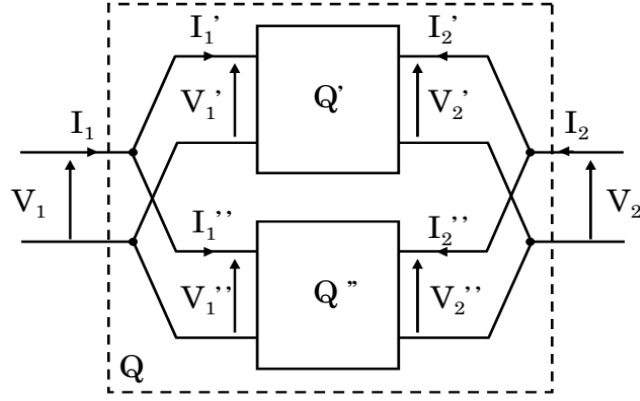


Figure II.14. Association of parallel-parallel quadrupoles

We use the admittance matrices and the two associated quadrupoles. \$[Y][Y''\$

$$[Y'] = \begin{bmatrix} Y_{11}' & Y_{12}' \\ Y_{21}' & Y_{22}' \end{bmatrix} \quad (II.26)$$

$$[Y''] = \begin{bmatrix} Y_{11}'' & Y_{12}'' \\ Y_{21}'' & Y_{22}'' \end{bmatrix} \quad (II.27)$$

SO

$$\begin{bmatrix} I_1' \\ I_2' \end{bmatrix} = [Y'] \times \begin{bmatrix} V_1' \\ V_2' \end{bmatrix} = \begin{bmatrix} Y_{11}' & Y_{12}' \\ Y_{21}' & Y_{22}' \end{bmatrix} \times \begin{bmatrix} V_1' \\ V_2' \end{bmatrix} \quad (II.28)$$

$$\begin{bmatrix} I_1'' \\ I_2'' \end{bmatrix} = [Y''] \times \begin{bmatrix} V_1'' \\ V_2'' \end{bmatrix} = \begin{bmatrix} Y_{11}'' & Y_{12}'' \\ Y_{21}'' & Y_{22}'' \end{bmatrix} \times \begin{bmatrix} V_1'' \\ V_2'' \end{bmatrix} \quad (II.29)$$

As

$$\begin{cases} I_1 = I_1' + I_1'' \\ I_2 = I_2' + I_2'' \end{cases} \text{ and } \begin{cases} V_1 = V_1' = V_1'' \\ V_2 = V_2' = V_2'' \end{cases} \quad (II.30)$$

SO

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} I_1' \\ I_2' \end{bmatrix} + \begin{bmatrix} I_1'' \\ I_2'' \end{bmatrix} \quad (II.31)$$

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = [Y'] \times \begin{bmatrix} V_1' \\ V_2' \end{bmatrix} + [Y''] \times \begin{bmatrix} V_1'' \\ V_2'' \end{bmatrix}$$

$$= [Y'] \times \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} + [Y''] \times \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

$$= ([Y'] + [Y'']) \times \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \Rightarrow$$

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = [Y] \times \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \Rightarrow$$

SO

$$[Y] = [Y'] + [Y''] \quad (II.32)$$

7.3 Link between impedance and admittance parameters

For reasons of simplicity, the determination of the admittance matrix can be done by determining the impedance matrix.

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \times \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \Rightarrow \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \times \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}^{-1} \times \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad (\text{II.33})$$

With

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \frac{1}{\Delta Z} \begin{bmatrix} Z_{22} & -Z_{21} \\ -Z_{12} & Z_{11} \end{bmatrix} \quad (\text{II.34})$$

And

As we noted before. $\Delta Z = Z_{22}Z_{11} - Z_{12}Z_{21}$

7.4 Series-parallel association

Let the two quadrupoles and having respectively the hybrid matrices and are connected in series-parallel as shown in the figure below. $Q'Q''[H'][H'']$

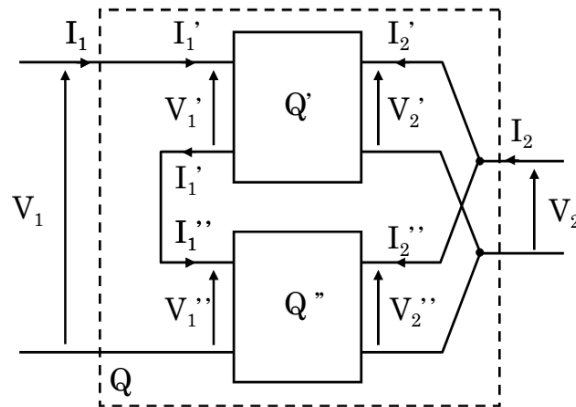


Figure II.15. Association of series-parallel quadrupoles

$$[H'] = \begin{bmatrix} h_{11}' & h_{12}' \\ h_{21}' & h_{22}' \end{bmatrix} \quad (\text{II.35})$$

$$(\text{II.36}) [H''] = \begin{bmatrix} h_{11}'' & h_{12}'' \\ h_{21}'' & h_{22}'' \end{bmatrix}$$

SO

$$\begin{bmatrix} V_1' \\ I_2' \end{bmatrix} = [H'] \times \begin{bmatrix} I_1' \\ V_2' \end{bmatrix} = \begin{bmatrix} h_{11}' & h_{12}' \\ h_{21}' & h_{22}' \end{bmatrix} \times \begin{bmatrix} I_1' \\ V_2' \end{bmatrix} \quad (\text{II.37})$$

$$\begin{bmatrix} V_1'' \\ I_2'' \end{bmatrix} = [H''] \times \begin{bmatrix} I_1'' \\ V_2'' \end{bmatrix} = \begin{bmatrix} h_{11}'' & h_{12}'' \\ h_{21}'' & h_{22}'' \end{bmatrix} \times \begin{bmatrix} I_1'' \\ V_2'' \end{bmatrix} \quad (\text{II.38})$$

As

$$\text{and (II.39)} \begin{cases} I_1 = I_1' = I_1'' \\ V_2 = V_2' = V_2'' \end{cases} \begin{cases} V_1 = V_1' + V_1'' \\ I_2 = I_2' + I_2'' \end{cases}$$

SO

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} V_1' \\ I_2' \end{bmatrix} + \begin{bmatrix} V_1'' \\ I_2'' \end{bmatrix} \quad (\text{II.40})$$

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = [H'] \times \begin{bmatrix} I_1' \\ V_2' \end{bmatrix} + [H''] \times \begin{bmatrix} I_1'' \\ V_2'' \end{bmatrix} \quad (\text{II.41})$$

$$= [H'] \times \begin{bmatrix} I_1 \\ V_2 \end{bmatrix} + [H''] \times \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

$$= ([H'] + [H'']) \times \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \Rightarrow$$

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = [H] \times \begin{bmatrix} I_1 \\ V_2 \end{bmatrix} \Rightarrow$$

SO

$$[H] = [H'] + [H''] \quad (\text{II.42})$$

7.5 Cascade (chain) association

Let the two quadrupoles and having the transfer matrices and respectively are cascaded as shown in the figure below. $Q'Q''[T'][T'']$

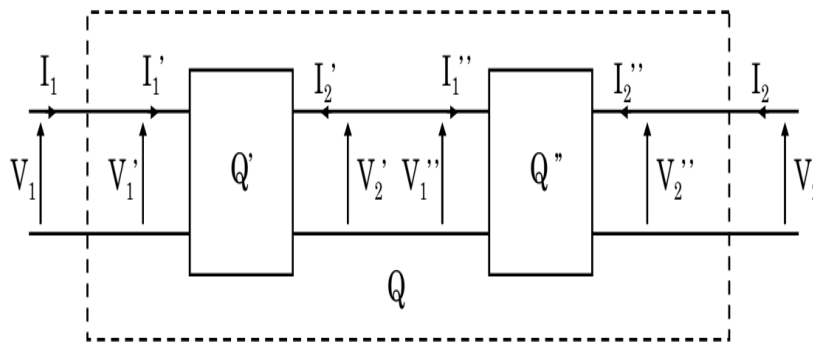


Figure II.16. Association of cascaded quadrupoles

The transfer matrices and the two associated quadrupoles are used. $[T'][T'']$

$$[T'] = \begin{bmatrix} T_{11}' & T_{12}' \\ T_{21}' & T_{22}' \end{bmatrix} \quad (\text{II.43})$$

$$[T''] = \begin{bmatrix} T_{11}'' & T_{12}'' \\ T_{21}'' & T_{22}'' \end{bmatrix} \quad (\text{II.44})$$

SO

$$\begin{bmatrix} V_2' \\ I_2' \end{bmatrix} = [T'] \times \begin{bmatrix} V_1' \\ -I_1' \end{bmatrix} = \begin{bmatrix} T_{11}' & T_{12}' \\ T_{21}' & T_{22}' \end{bmatrix} \times \begin{bmatrix} V_1' \\ -I_1' \end{bmatrix} \quad (\text{II.45})$$

$$\begin{bmatrix} V_2'' \\ I_2'' \end{bmatrix} = [T''] \times \begin{bmatrix} V_1'' \\ -I_1'' \end{bmatrix} = \begin{bmatrix} T_{11}'' & T_{12}'' \\ T_{21}'' & T_{22}'' \end{bmatrix} \times \begin{bmatrix} V_1'' \\ -I_1'' \end{bmatrix} \quad (\text{II.46})$$

As and $I_1'' = I_2' V_1'' = V_2'$

SO

$$\begin{bmatrix} V_2 \\ I_2 \end{bmatrix} = \begin{bmatrix} T_{11}'' & T_{12}'' \\ T_{21}'' & T_{22}'' \end{bmatrix} \times \begin{bmatrix} V_2' \\ I_2' \end{bmatrix} \quad (\text{II.47})$$

$$\begin{bmatrix} V_2 \\ I_2 \end{bmatrix} = \begin{bmatrix} T_{11}'' & T_{12}'' \\ T_{21}'' & T_{22}'' \end{bmatrix} \times \begin{bmatrix} T_{11}' & T_{12}' \\ T_{21}' & T_{22}' \end{bmatrix} \times \begin{bmatrix} V_1 \\ -I_1 \end{bmatrix} \quad (\text{II.47})$$

$$= ([T'] \times [T'']) \times \begin{bmatrix} V_1 \\ -I_1 \end{bmatrix} \Rightarrow$$

$$\begin{bmatrix} V_2 \\ I_2 \end{bmatrix} = [T] \times \begin{bmatrix} V_1 \\ -I_1 \end{bmatrix} \Rightarrow$$

SO

$$[T] = [T'] \times [T''] \quad (\text{II.48})$$

The equivalent quadrupole transfer matrix is equal to the product of the second transfer matrix by the first. This product is not commutative.

7.6 Link between parameters

The relationship between the quadrupole parameters is summarized in the following table

	T	Z	Y	h
T	$\begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix}$	$\begin{bmatrix} Z_{11}/Z_{21} & -\Delta Z/Z_{21} \\ 1/Z_{21} & -Z_{22}/Z_{21} \end{bmatrix}$	$\begin{bmatrix} -Y_{22}/Y_{21} & 1/Y_{21} \\ -\Delta Y/Y_{21} & Y_{11}/Y_{21} \end{bmatrix}$	$\begin{bmatrix} -\Delta h/h_{21} & -h_{11}/h_{21} \\ -h_{22}/h_{21} & -1/h_{21} \end{bmatrix}$
Z	$\begin{bmatrix} T_{11}/T_{21} & \Delta T/T_{21} \\ 1/T_{21} & T_{22}/T_{21} \end{bmatrix}$	$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}$	$\begin{bmatrix} Y_{22}/\Delta Y & -Y_{12}/\Delta Y \\ -Y_{21}/\Delta Y & Y_{11}/\Delta Y \end{bmatrix}$	$\begin{bmatrix} \Delta h/h_{22} & h_{12}/h_{22} \\ -h_{21}/h_{22} & 1/h_{22} \end{bmatrix}$
Y	$\begin{bmatrix} T_{22}/T_{12} & -\Delta T/T_{12} \\ -1/T_{12} & T_{11}/T_{12} \end{bmatrix}$	$\begin{bmatrix} Z_{22}/\Delta Z & -Z_{12}/\Delta Z \\ -Z_{21}/\Delta Z & Z_{11}/\Delta Z \end{bmatrix}$	$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}$	$\begin{bmatrix} 1/h_{11} & -h_{12}/h_{11} \\ h_{21}/h_{11} & \Delta h/h_{11} \end{bmatrix}$
h	$\begin{bmatrix} T_{12}/T_{22} & \Delta T/T_{22} \\ -1/T_{22} & T_{21}/T_{22} \end{bmatrix}$	$\begin{bmatrix} \Delta Z/Z_{22} & Z_{12}/Z_{22} \\ -Z_{21}/Z_{22} & 1/Z_{22} \end{bmatrix}$	$\begin{bmatrix} 1/Y_{11} & -Y_{12}/Y_{11} \\ Y_{21}/Y_{11} & \Delta Y/Y_{11} \end{bmatrix}$	$\begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix}$

8. Passive Filters

Often we need to cancel certain frequencies or keep only a particular frequency band. This is the function of filters. The quadrupoles that we have just studied constitute them. Their role is to pass or block a specific frequency band of an alternating signal.

There are two families of filters:

Passive filters

They only consist of resistors, inductors and capacitors. They do not allow amplification (the output power is less than the input power).

Active filters

Consist of one or more active elements such as operational amplifiers, transistors and passive components. They allow the signal to be amplified.

8.1 The main types of filters

Depending on the main task of the filters to let or not let certain frequencies, the filters are subdivided into 4 types:

- Low-pass filters: only allow low frequencies to pass;
- High-pass filters: only allow high frequencies to pass;
- Band-pass filters: only allow a range of frequencies to pass;
- Band-Notch filters: do not allow a range of frequencies to pass.

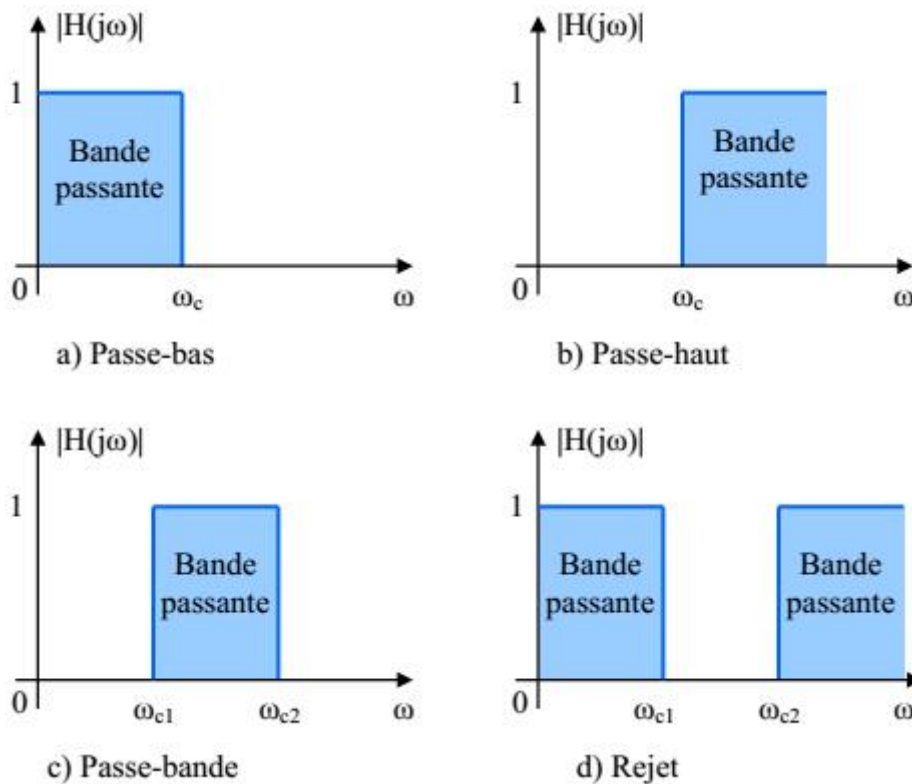


Figure II.17. Some types of filters

8.2 Complex transfer function of a filter

Filters are characterized by a very important parameter that can describe their behavior, which is the transfer function or complex transmittance. It is a mathematical function that describes the behavior as a function of the frequency of a filter (in sinusoidal mode). The modulus of the transfer function corresponds to the voltage amplification: $H(\omega)$.

$$H(\omega) = |\underline{H}(\omega)| = \left| \frac{V_s}{V_e} \right| \quad (\text{II.49})$$

The phase shift introduced by the filter can be calculated by:

$$\varphi(\omega) = \text{Arg}(\underline{H}(\omega)) = \text{Arg}\left(\frac{V_s}{V_e}\right) = \text{Arg}(V_s) - \text{Arg}(V_e) \quad (\text{II.50})$$

The modulus and the argument of the complex transmittance which are represented by curves in the Bode plane, are used to obtain data that allow predicting the response of the system studied under any excitation conditions (frequency response). The Bode diagram is adopted to graphically represent the variation of as a function of the angular frequency (or frequency). Because of the large range of values of the modulus of $H(\omega)$ depending on the frequency, This forced us to use a logarithmic scale, i.e. the representation of the function:

$$G = 20 \log_{10}|H(\omega)| \quad (\text{II.51})$$

as a function of the pulsation. is called the gain of the transfer function and is expressed in decibels (dB).

8.2.1 Behavior of impedances L and C as a function of frequency

The impedance of the coil for low frequencies tends to zero, therefore the coil behaves like a short circuit and for high frequencies tends to infinity, and it behaves like an open circuit. The capacitor the same behavior observed but in an inverted way. The following table summarizes their behaviors according to the frequency:

Component	Impedance	Low frequencies	High frequencies
Bobine (Self)	$jL\omega$	Short circuit (CC)	Open Court (OC)
Capacitor	$\frac{1}{jC\omega}$	Open Court (OC)	Short circuit (CC)

8.3 First Order Low Pass Filter

8.3.1 Transfer function

Consider the RC circuit in Figure II.11. Where the output voltage V_s is deduced from the voltage divider rule:

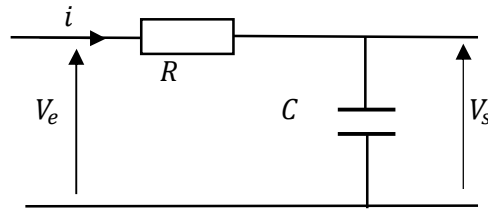


Figure II.18. Passive low-pass filter

We pose

$$Z_C = \frac{1}{jC\omega}$$

To calculate the transfer function we have:

$$V_e = (R + Z_C)i$$

And

$$V_s = Z_C i$$

So, the report gives us:

$$\begin{aligned} \frac{V_s}{V_e} &= \frac{Z_C}{R + Z_C} = \frac{\frac{1}{jC\omega}}{R + \frac{1}{jC\omega}} = \frac{1}{1 + jRC\omega} \\ \frac{V_s}{V_e} &= \frac{1}{1 + jRC\omega} \\ H(\omega) &= \frac{1}{1 + jRC\omega} \end{aligned}$$

Or we simply use the voltage divider and we will have

$$V_s = \frac{Z_C}{R + Z_C} V_e = \frac{\frac{1}{jC\omega}}{R + \frac{1}{jC\omega}} V_e = \frac{1}{1 + jRC\omega} V_e$$

SO

$$\begin{aligned} \frac{V_s}{V_e} &= \frac{1}{1 + jRC\omega} \\ H(\omega) &= \frac{1}{1 + jRC\omega} \end{aligned}$$

The transmittance modulus or voltage gain is

$$|H(\omega)| = \left| \frac{1}{1 + jRC\omega} \right| = \frac{1}{\sqrt{1 + (RC\omega)^2}} = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2}}$$

Or

$$\omega_0 = \frac{1}{RC}$$

8.3.2 Bode plot of gain

$$G(\omega) = 20\text{Log}_{10}H(\omega) = 20\text{Log}_{10}\left(\frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2}}\right) = -10\text{Log}_{10}\left(1 + \left(\frac{\omega}{\omega_0}\right)^2\right)$$

$$\varphi = -\arctan\left(\frac{\omega}{\omega_0}\right)$$

8.3.3 Cut-off pulse at -3dB

The cut-off pulse can be calculated as follows

$$H(\omega_c) = \frac{H_{\max}}{\sqrt{2}}$$

$$H_{\max} = H(\omega \rightarrow 0) = 1$$

$$\Rightarrow \frac{1}{\sqrt{1 + \left(\frac{\omega_c}{\omega_0}\right)^2}} = \frac{1}{\sqrt{2}}$$

From where

$$\frac{\omega_c}{\omega_0} = 1 \Rightarrow \omega_c = \omega_0 = \frac{1}{RC}$$

8.3.4 Limit study

As the pulsation approaches zero, the gain approaches zero and the argument approaches zero. $\omega \rightarrow 0$ $G \rightarrow 0$ $\varphi \rightarrow 0$

And when tends to infinity, tends to and tends to And for ; and . $\omega \rightarrow \infty$ $G \rightarrow -\infty$ $\varphi \rightarrow -\pi/2$ $\omega = \omega_c$ $G = -3\text{dB}$ $\varphi = -\pi/4$

8.3.5 Determination of asymptotes to the curves and: $G(\omega)$ $\varphi(\omega)$

For ; and $\omega \ll \omega_0$ $G(\omega) \cong 0 \text{ dB}$ $\varphi(\omega) \cong 0$

For ; This asymptotic line decreases as a function of the pulsation with a slope of . It passes through the

point (,0).and . $\omega \gg \omega_0$ $G(\omega) \cong 20\text{Log}_{10}\frac{\omega_0}{\omega} - 20\text{dB/décade}$ $\varphi(\omega) \cong -\pi/2$

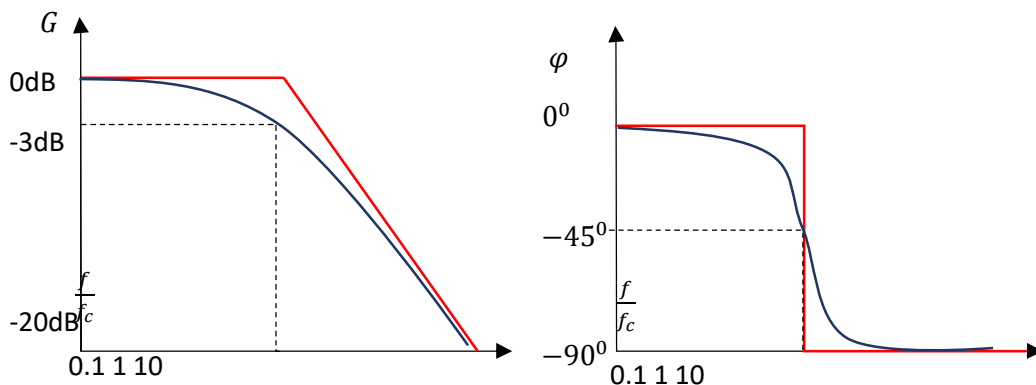


Figure II.19. Representation of gain and phase in the Bode plane of a low-pass filter

8.4 First Order High Pass Filter

8.4.1 Transfer function

The same circuit as before with the location of the resistor and capacitance reversed.

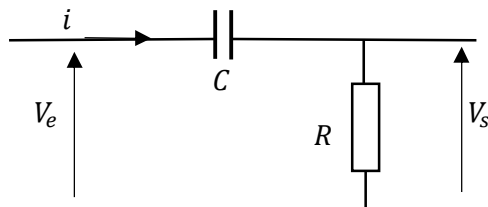


Figure II.20. Passive high pass filter

We pose

$$Z_C = \frac{1}{jC\omega}$$

To calculate the transfer function we have:

$$V_e = (R + Z_C)i$$

And

$$V_s = Ri$$

So, the report gives us:

$$\begin{aligned} \frac{V_s}{V_e} &= \frac{R}{R + Z_C} = \frac{R}{R + \frac{1}{jC\omega}} = \frac{jRC\omega}{1 + jRC\omega} \\ \frac{V_s}{V_e} &= \frac{jRC\omega}{1 + jRC\omega} \\ H(\omega) &= \frac{jRC\omega}{1 + jRC\omega} \end{aligned}$$

Or we simply use the voltage divider and we will have

$$V_s = \frac{R}{R + Z_C} V_e = \frac{R}{R + \frac{1}{jC\omega}} V_e = \frac{jRC\omega}{1 + jRC\omega} V_e$$

SO

$$\begin{aligned} \frac{V_s}{V_e} &= \frac{jRC\omega}{1 + jRC\omega} \\ H(\omega) &= \frac{jRC\omega}{1 + jRC\omega} \\ H(\omega) &= \frac{j \frac{\omega}{\omega_0}}{1 + j \frac{\omega}{\omega_0}} \end{aligned}$$

The transmittance modulus or voltage gain is

$$|H(\omega)| = \left| \frac{j \frac{\omega}{\omega_0}}{1 + j \frac{\omega}{\omega_0}} \right| = \frac{1}{\sqrt{1 + \left(\frac{\omega_0}{\omega}\right)^2}}$$

With

$$\omega_0 = \frac{1}{RC}$$

8.4.2 Bode plot of gain

$$G(\omega) = 20 \text{Log}_{10} H(\omega) = 20 \text{Log}_{10} \left(\frac{1}{\sqrt{1 + \left(\frac{\omega_0}{\omega}\right)^2}} \right) = -10 \text{Log}_{10} \left(1 + \left(\frac{\omega_0}{\omega}\right)^2 \right)$$

$$\varphi = \frac{\pi}{2} - \arctan \left(\frac{\omega_0}{\omega} \right)$$

8.4.3 Cutoff pulse at -3dB

The cut-off pulse can be calculated as follows

$$H(\omega_c) = \frac{H_{\max}}{\sqrt{2}}$$

$$H_{\max} = H(\omega \rightarrow 0) = 1$$

$$\Rightarrow \frac{1}{\sqrt{1 + \left(\frac{\omega_c}{\omega_0}\right)^2}} = \frac{1}{\sqrt{2}}$$

From where

$$\frac{\omega_c}{\omega_0} = 1 \Rightarrow \omega_c = \omega_0 = \frac{1}{RC}$$

8.4.4 Limit study

When the pulsation tends to zero, the gain tends to and the argument tends to . And when tends to infinity, tends to and tends to And for ; and . $\omega \rightarrow 0 \Rightarrow G = 0 \text{ dB}$ $\varphi = \pi/2$ $\omega \rightarrow \infty \Rightarrow G = -3 \text{ dB}$ $\varphi = \pi/4$

8.4.5 Determination of asymptotes to curves and $G(\omega)$ $\varphi(\omega)$

For ; and $0 \ll \omega \ll \omega_0 \Rightarrow G(\omega) \cong 0 \text{ dB}$ $\varphi(\omega) \cong$

For ; This asymptotic line decreases as a function of the pulsation with a slope of . It passes through the point $(\omega_0, -3 \text{ dB})$ and $\omega \gg \omega_0 \Rightarrow G(\omega) \cong 20 \text{Log} \frac{\omega_0}{\omega} - 20 \text{ dB/décade}$ $\varphi(\omega) \cong -\pi/2$

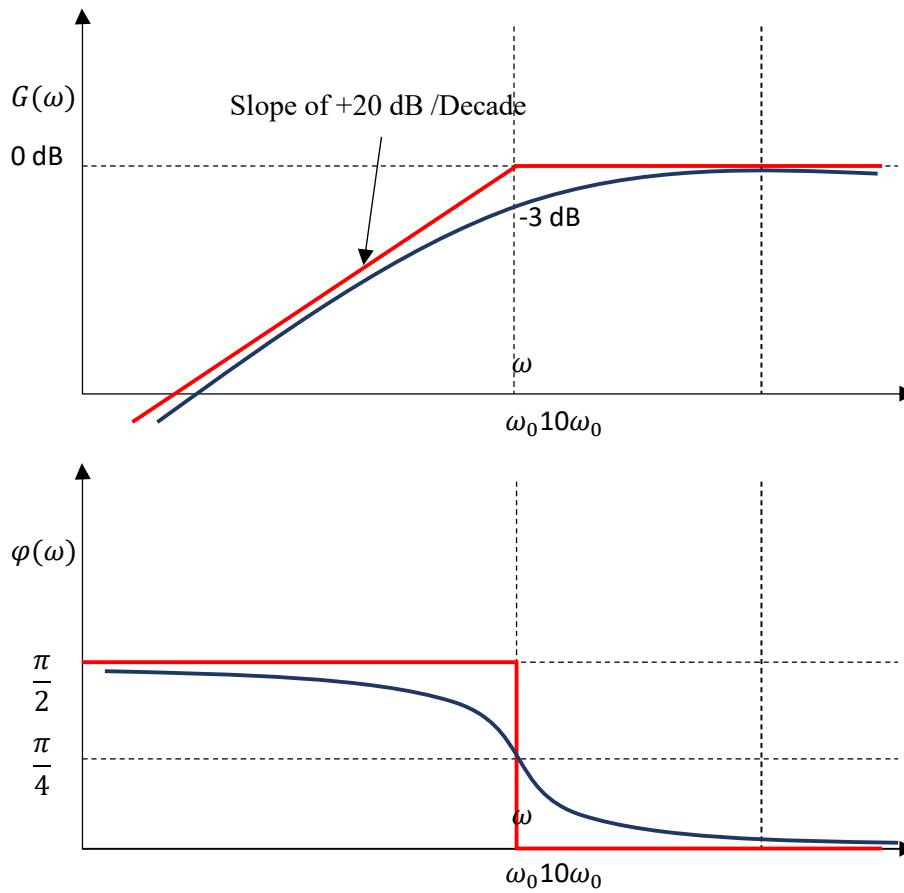


Figure II.21. Representation of gain and phase in the Bode plane of a high-pass filter

8.5 Bandpass filter

For this type of filter we adopt the series RLC circuit where the output is taken between the terminals of the resistor:

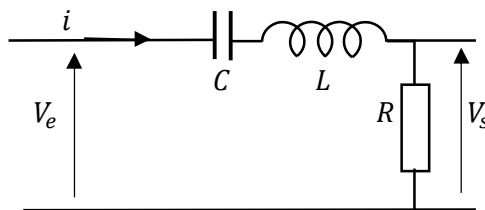


Figure II.22. Passive band pass filter

Since the capacitor behaves like an open circuit at low frequencies, no current flows through the resistor. On the other hand, at high frequencies, it is the inductance that behaves like an open circuit and therefore no current flows through the resistor. Therefore, the transfer of energy from the input to the output occurs between high and low frequencies. At a certain frequency,

the impedance of the capacitor (which is negative) cancels the impedance of the inductance, the amplitude of the transfer function is real, and the output voltage is the same as that of the input.

We pose

$$\text{And } Z_C = \frac{1}{jC\omega} Z_L = jL\omega$$

To calculate the transfer function we have:

$$V_e = (R + Z_C + Z_L)i$$

And

$$V_s = Ri$$

So, the report gives us:

$$\frac{V_s}{V_e} = \frac{R}{R + Z_C + Z_L} = \frac{R}{R + jL\omega + \frac{1}{jC\omega}} = \frac{jRC\omega}{1 + jLC\omega^2 + jRC\omega} = \frac{1}{1 + j\left(\frac{L}{R}\omega - \frac{1}{RC\omega}\right)}$$

$$\frac{V_s}{V_e} = \frac{1}{1 + j\left(\frac{L}{R}\omega - \frac{1}{RC\omega}\right)} = \frac{1}{1 + jQ\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)}$$

$$H(\omega) = \frac{1}{1 + jQ\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)}$$

With

$$\text{And } \omega_0 = \frac{1}{\sqrt{LC}} Q = \frac{1}{R} \sqrt{\frac{L}{C}}$$

The transmittance modulus or voltage gain is

$$|H(\omega)| = \left| \frac{1}{1 + jQ\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)} \right| = \frac{1}{\sqrt{1 + Q^2 \left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)^2}}$$

8.5.1 Bode plot of gain

$$G(\omega) = 20\text{Log}_{10}H(\omega) = 20\text{Log}_{10} \frac{1}{\sqrt{1 + Q^2 \left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)^2}} = -10\text{Log}_{10} \left(1 + Q^2 \left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)^2 \right)$$

$$\varphi(\omega) = -\arctan Q \left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right)$$

8.5.2 Cutoff pulses at -3dB

The cut-off pulses can be calculated by solving the equation:

$$H(\omega_c) = \frac{H_{\max}}{\sqrt{2}}$$

$$H_{\max} = H(\omega \rightarrow 0) = 1$$

$$\Rightarrow \frac{1}{\sqrt{1 + Q^2 \left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right)^2}} = \frac{1}{\sqrt{2}}$$

Hence the two cutoff pulses are:

$$\omega_{c1} = -\frac{R}{2L} + \sqrt{\frac{1}{LC} + \left(\frac{R}{2L}\right)^2} ; \omega_{c2} = +\frac{R}{2L} + \sqrt{\frac{1}{LC} + \left(\frac{R}{2L}\right)^2}$$

8.5.3 Filter Bandwidth

The filter bandwidth is the difference between and : $\omega_{c1} \omega_{c2}$

$$\beta = \omega_{c1} - \omega_{c2} = \frac{R}{L}$$

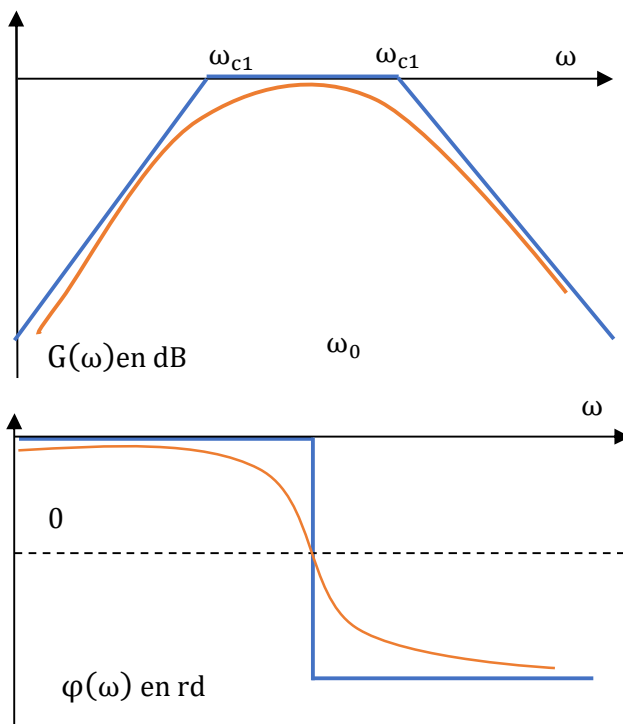


Figure II.23. Represents the response of a band-pass filter. The cutoff frequencies are defined by the points where the amplitude reaches the maximum value.

8.5.4 Limit study

As the pulsation approaches zero, the gain approaches zero and the argument approaches zero. $\omega \ll \omega_0$ $G \approx 0$ $\varphi \approx 0$

And when tends to infinity, tends to and tends to And for ; and . $\omega \gg \omega_0$ $G \approx -3\text{dB}$ $\varphi \approx -\pi/2$

8.5.5 Determination of asymptotes to curves and $G(\omega)$ $\varphi(\omega)$

For ; and $\omega \ll \omega_0$ $G(\omega) \cong 0 \text{ dB}$ $\varphi(\omega) \cong 0$

For ; This asymptotic line decreases as a function of the pulsation with a slope of . It passes through the point $(\omega_0, 0)$. and $\omega \gg \omega_0$ $G(\omega) \cong 20 \text{Log} \frac{\omega_0}{\omega} - 20 \text{dB/décade}$ $\varphi(\omega) \cong -\pi/2$

8.6 Notch filter

We use the same series RLC circuit from the previous filter but this time the output is taken from the terminals of the inductance and the capacitor in series.

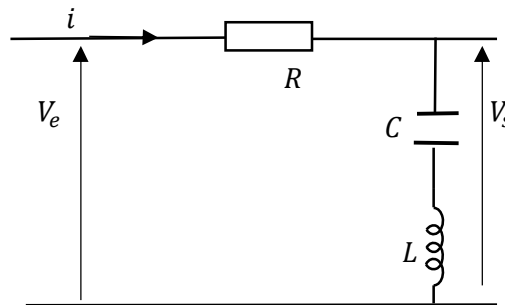


Figure II.24. Passive band-stop filter

8.6.1 Operating principle

The capacitor behaves like an open circuit; at low frequencies, therefore the output voltage is the same as the input. At high frequencies: it is the inductance that behaves like an open circuit, and the output is the same as the input. At the resonant frequency, the impedance of the inductance cancels the impedance of the capacitor, and therefore there is a short circuit, and the output is zero.

The transfer function of this circuit is:

We pose

$$\text{And } Z_C = \frac{1}{jC\omega} \quad Z_L = jL\omega$$

To calculate the transfer function we have:

$$V_e = (R + Z_C + Z_L)i$$

And

$$V_s = (Z_C + Z_L)i$$

So, the report gives us:

$$\frac{V_s}{V_e} = \frac{(Z_C + Z_L)}{R + Z_C + Z_L} = \frac{jL\omega + \frac{1}{jC\omega}}{R + jL\omega + \frac{1}{jC\omega}} = \frac{\frac{1}{LC} - \omega^2}{\frac{1}{LC} - \omega^2 + j\frac{R}{L}\omega}$$

$$H(\omega) = \frac{\frac{1}{LC} - \omega^2}{\frac{1}{LC} - \omega^2 + j\frac{R}{L}\omega}$$

With

The transmittance modulus or voltage gain is

$$|H(\omega)| = \left| \frac{\frac{1}{LC} - \omega^2}{\frac{1}{LC} - \omega^2 + j\frac{R}{L}\omega} \right| = \frac{\left| \frac{1}{LC} - \omega^2 \right|}{\sqrt{\left(\frac{1}{LC} - \omega^2\right)^2 + \left(\frac{R}{L}\omega\right)^2}}$$

$$\varphi(\omega) = -\arctan Q \left(\frac{\frac{R}{L}\omega}{\frac{1}{LC} - \omega^2} \right)$$

8.6.2 Bode plot of gain

$$G(\omega) = 20\text{Log}_{10}H(\omega) = 20\text{Log}_{10} \frac{\left| \frac{1}{LC} - \omega^2 \right|}{\sqrt{\left(\frac{1}{LC} - \omega^2\right)^2 + \left(\frac{R}{L}\omega\right)^2}}$$

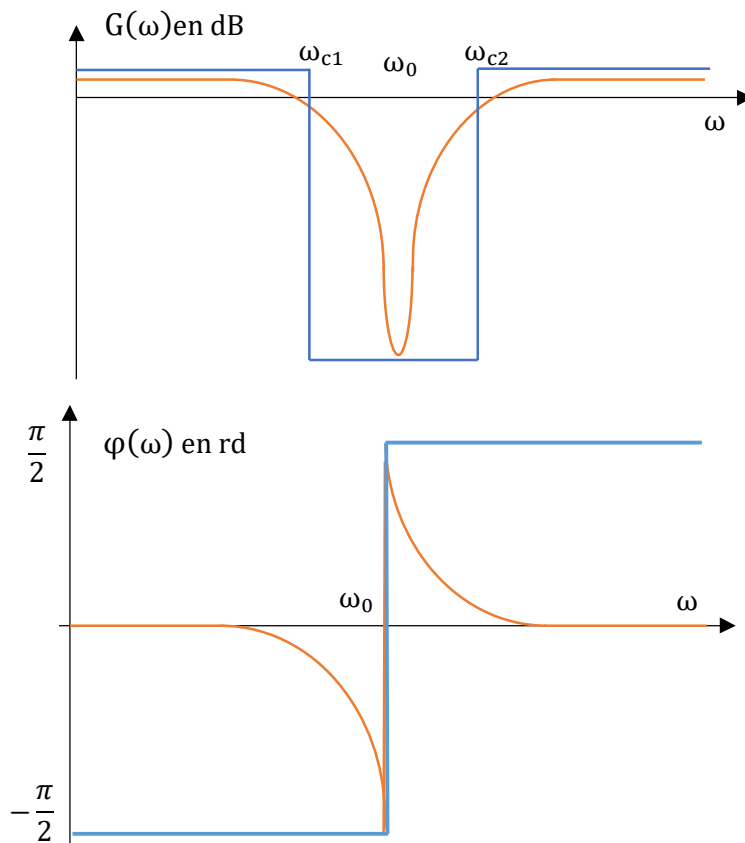


Figure II.25. Represents the response of a band-pass filter. The cutoff frequencies are defined by the points where the amplitude reaches the maximum value.

8.6.3 Limit study

As the pulsation approaches zero, the gain approaches zero and the argument approaches zero. $\omega \rightarrow 0 \Rightarrow G \rightarrow 0 \Rightarrow \varphi \rightarrow 0$

And when tends to infinity, tends to and tends to And for ; and $\omega \rightarrow \infty \Rightarrow G \rightarrow 0 \Rightarrow \varphi \rightarrow -\pi/2$. $\omega = \omega_c \Rightarrow G = -3\text{dB} \Rightarrow \varphi = -\pi/4$

8.6.4 Determination of asymptotes to curves and $G(\omega)\varphi(\omega)$

For ; and $\omega \ll \omega_0 G(\omega) \cong 0 \text{ dB}$ $\varphi(\omega) \cong 0$

For ; This asymptotic line decreases as a function of the pulsation with a slope of . It passes through the point $(,0)$. and $\omega \gg \omega_0 G(\omega) \cong 20 \text{Log} \frac{\omega_0}{\omega} - 20 \text{dB/décade}$ $\varphi(\omega) \cong -\pi/2$

Chapter III Junction Diodes and its Applications

Objective

Define semiconductors, doping types, N-type and P-type semiconductors.

Describe the PN junction quantitatively and discover the fundamental mechanisms of its operation. Understand the influence of an external voltage V applied to the junction to calculate the resulting $I(V)$ characteristic. Highlight the particular properties when the junction is subjected to a dynamic signal. Presentation of some fundamental functions based on diodes.

Definitions

1. Semiconductor

A material which has the electrical characteristics of an insulating, but for which the probability that an electron can contribute to an electric current, although small, is sufficiently large. In other words, the electrical conductivity of a semiconductor is intermediate between that of metals and that of insulators.

The electrical behavior of semiconductors is usually modeled using the band theory energy. According to this, a semiconductor material has a band gap small enough that electrons from the valence band can easily reach the conduction band. If an electric potential is applied to its terminals, a weak electric current appears, caused both by the movement of electrons and by that of the "holes" that they leave in the valence band.

Silicon is the most commercially used semiconductor material, due to its good properties, and its natural abundance even if there are also dozens of other semiconductors used, such as germanium, gallium arsenide or silicon carbide.

2. Intrinsic semi-conduction

A semiconductor is said to be intrinsic when it is pure: it contains no impurities and its electrical behavior depends only on the structure of the material. This behavior corresponds to a perfect semiconductor, that is to say without structural defects or chemical impurities. A real semiconductor is never perfectly intrinsic but can sometimes be close to it, like silicon pure monocrystalline.

In an intrinsic semiconductor, the charge carriers are created only by crystal defects and thermal excitation. The number of electrons in the conduction band is equal to the number of holes in the valence band. These semiconductors do not conduct current, or conduct very little, except if they are heated to high temperatures.

3. Doping

Since the formation of forbidden bands is due to the regularity of the crystal structure, any perturbation of it tends to create accessible states inside these forbidden bands, making the gap more permeable. Doping consists of implanting correctly selected atoms (called impurities) inside an intrinsic semiconductor in order to control its electrical properties.

Doping increases the carrier density inside the semiconductor material. If it increases the electron density, it is called N-type doping. If it increases the hole density, it is called P-type doping. Materials doped in this way are called extrinsic semiconductors. The electrical conductivity of semiconductors can be controlled by doping, by introducing a small amount of impurities into the material to produce an excess of electrons or a deficit. Differently doped semiconductors can be brought into contact to create junctions, allowing to control the direction and the quantity of current which passes through the assembly. This property is the basis for the functioning of the components of modern electronics (diodes, transistors, etc.).

3.1 N-doping

N-type doping involves increasing the electron density in the semiconductor. This is done by including a number of electron-rich atoms in the semiconductor.

For example, in the case of silicon (Si), Si atoms have four valence electrons, each bonded to a neighboring Si atom by a covalent bond forming a tetrahedron. To dope silicon with N, an atom with five valence electrons is included, such as those in column V (VA) of the periodic table: Phosphorus (P), Arsenic (As) or Antimony (Sb), etc.

This atom incorporated in the crystal lattice will have four covalent bonds and a free electron. This fifth electron, which is not a bonding electron, is only weakly bound to the atom and can be easily excited towards the conduction band. At ordinary temperatures, almost all of these electrons are. Since the excitation of these electrons does not lead to the formation of holes in this type of material, the number of electrons far exceeds the number of holes. Electrons are majority carriers and holes are minority carriers. And because atoms with five electrons have an extra electron to "donate," they are called donor atoms.

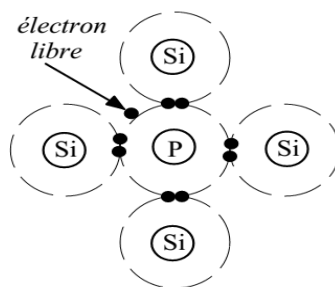


Figure III.1. Doping by donor atom (Phosphorus in this example)

3.2 P-doping

P-type doping involves increasing the hole density in the semiconductor. This is done by including a number of electron-poor atoms in the semiconductor to create an excess of holes. In the silicon example, a trivalent atom (column III of the periodic table) will be included, usually an atom of boron. This atom having only three valence electrons, it can only create three covalent bonds with its four neighbors, thus creating a hole in the structure, a hole that can be filled by an electron donated by a neighboring silicon atom, thus displacing the hole. When the doping is sufficient, the number of holes far exceeds the number of electrons. The holes are then majority carriers and the electrons are minority carriers.

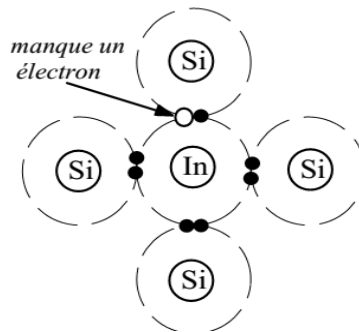


Figure III.2. Doping by acceptor atom (Indium in this example)

3. PN junction

A PN junction is obtained by the juxtaposition of two portions of the same crystal which are oppositely doped N and P.

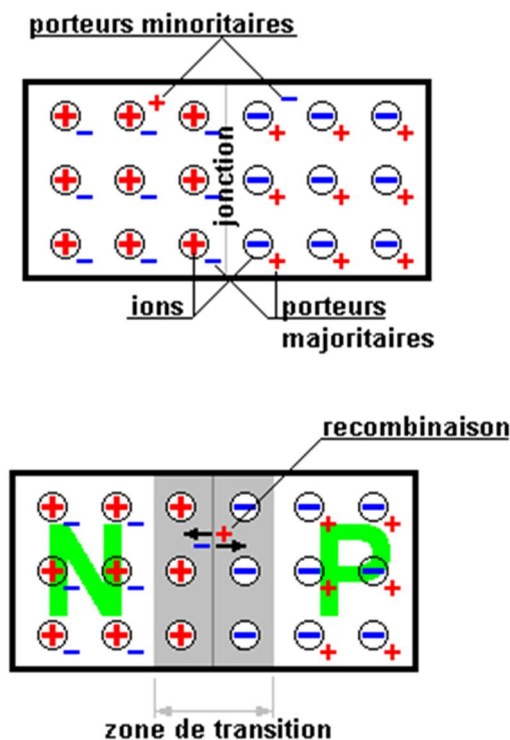


Figure III.3. PN junction

If we place two semiconductor crystals, one of type P and the other of type N, against each other in the vicinity of the junction thus made, the majority electrons on the N side will diffuse towards the P side and the majority holes on the P side will diffuse towards the N side. The electrons passed to the P side will recombine with the abundant holes on this side, and the holes passed to the N side will recombine with the abundant electrons on this side. A region without carriers is then created where there are only positive ions on the N side and negative ions on the P side. This region, called the space charge zone or depopulated zone, is no longer electrically neutral. On either side of the junction, there is a double distribution of charges quite similar to that found on the plates of a capacitor, the positive charges on one side, the negative ones on the other. An internal electric field is then created, oriented from N to P, which will oppose the diffusion of carriers on either side of the junction. Indeed, if an electron arrives in the depopulated zone, it will be recalled by the field to the zone from which it came. In the same way, the holes which arrive in this zone are returned by the field to the zone P from which they came. If we take the phenomenon from the beginning, as the carriers diffuse on either side of the junction, the space charges (+) and (-) increase and the field increases with them. The more the field increases, the more the diffusion of carriers is slowed down; we say that a potential barrier is created which prevents the carriers from crossing the junction. There comes a point where a statistical equilibrium is established, everything happens as if no electron manages to diffuse on the P side and no hole manages to diffuse on the N side, the charges (+) and (-) on each side of the junction stop increasing and the field too. \vec{E}_i

4. Polarization of the PN junction

4.1 Reverse biased junction

A PN junction is said to be forward biased when the P end is connected to the (+) pole and the N end to the (-) pole of a voltage generator (Fig. III-2). The external field E_{ext} created by this generator within the junction opposes the internal field E_i . As long as the generator voltage U remains below a certain threshold, E_{ext} remains below E_i , and the carriers still cannot cross the junction, so there is no current. If the generator voltage becomes higher than the threshold, E_{ext} becomes higher than E_i , the resulting field in the junction is now oriented from P to N and will therefore promote the diffusion of electrons from N to P and holes from P to N. A significant electric current is then created from P to N within the junction (from N to P in the external circuit). The diode is said to be conducting. The voltage threshold at which the diode becomes conductive is approximately 0.2V for germanium and 0.65V for silicon.

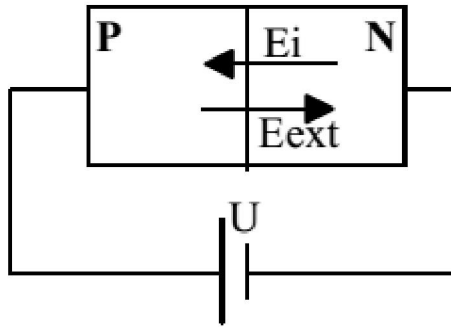


Figure III.4. Forward polarized junction

A junction is said to be reverse biased.

4.2 Reverse biased junction

When the potential of its N end is higher than that of its P end (Figure III.5). The action of the field E_{ext} created by the external generator adds to that of the internal field E_i , the majority carriers are pushed back a little further from the junction which increases the width of the depopulated zone. No significant current flows in the junction, it is said to be blocked. The only current that manages to pass is that created by the minority carriers whose diffusion is encouraged by the field. This current remains very low, however, so much so that we can consider that a reverse-biased PN junction corresponds to a very high resistance or even to an open circuit.

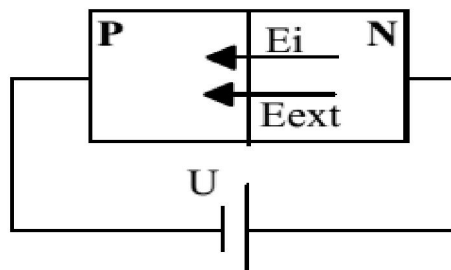


Figure III.5. Reverse biased junction

5. The junction diode

5.1 Constitution

It is made by a PN junction. The junction diode represents the basic component of semiconductor elements. It is obtained by simply making a PN junction. Figure-II.1 represents the semiconductor structure of a diode and its symbol in electronic circuits.

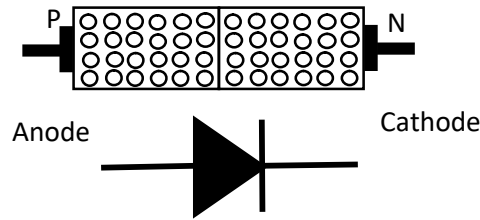


Figure III.6. The semiconductor structure of a diode and its symbol.

5.2 Characteristics of a diode

The voltage V between the anode and the cathode of a diode and the current I flowing through it are linked by an exponential relationship such as:

$$I = I_S \left(e^{\frac{eV_d}{kT}} - 1 \right) \quad (\text{III.1})$$

In the direct direction The curve representing the equation(III.1)is given in Figure III.7. The voltage V_0 is the threshold of the diode. The current I_S is the saturation current. It represents the current that flows through the diode in the case where the latter is blocked. The voltage V_B called the breakdown voltage, it corresponds to the value of the reverse voltage that triggers the avalanche phenomenon.

In practice, to study or analyze diode circuits, we replace the diodes found there:

- By a voltage source V_0 in series with a resistor R_d for forward polarization of the diodes.
- By a resistance R_i for blocked diodes With:

$$V_0 \cong 0.6V \text{ for Si.}$$

$$V_0 \cong 0.3V \text{ for Ge.}$$

R_d = low value direct resistance.

R_i = very high value reverse resistance.

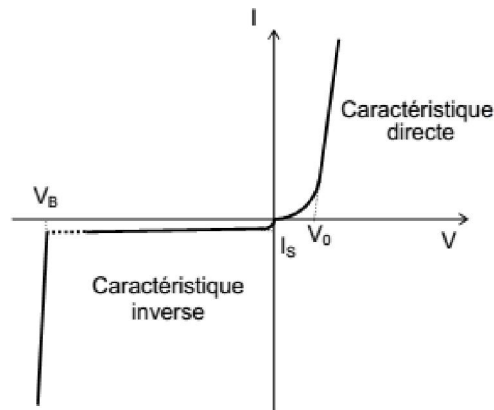


Figure III.7. Characteristics of a diode (Direct characteristic for passing diode and reverse characteristic for blocked diode).

In practice, and especially in the case where V_0 has a low value in comparison with the electrical quantities of the circuit to be studied, the diodes will be considered ideal. This makes it possible to simplify the study of diode circuits by replacing a passing diode with a short circuit, and a blocked diode with an open circuit.

5.3 Static resistance

The static resistance of a diode defines the equivalent resistance of the diode when a constant current flows through it. From Figure 8 we see that diode D is biased by a continuous source of emf E.

The equivalent resistance to the diode seen by the source E is a static resistance R_S which can be expressed by:

$$R_S = \frac{V}{I} \quad (\text{III.2})$$

The value of this resistance can also be determined graphically. In addition to the curve representing the diode characteristic, the circuit in Figure II.3 allows us to express I as a function of V, with respectively I current in D and V voltage between its terminals.

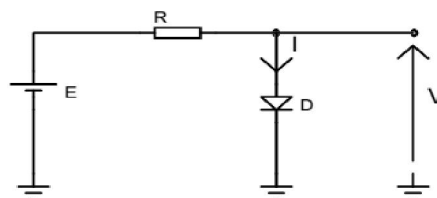


Figure III.8. In this circuit the diode is polarized in its forward direction.

It is seen by the rest of the circuit as a static resistance R_S . The circuit contains only continuous quantities which do not vary with time, hence the word static.

From the circuit in Figure III.8 we have:

$$E = RI + V \quad (\text{III.3})$$

$$I = -\frac{E}{R} + \frac{V}{R} \quad (\text{III.4})$$

It can be seen that expression III.4 represents the equation of a straight line. This straight line is known as the load line. To determine the value of the static resistance, it is necessary to know the value of I and that of V. These two values can be determined graphically as the coordinates of the point of intersection between the load line and the diode characteristic, as illustrated in Figure 8. The point Q with coordinates (I₀, V₀) is the operating point of the diode. $I = f(V)$

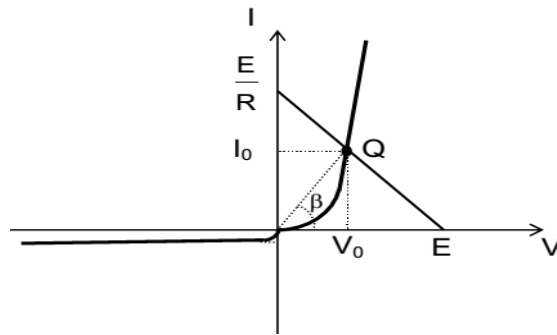


Figure III.9. Graphically, the static resistance is the ratio between the voltage V₀, ordinate of the operating point Q, and its ordinate I₀. Which corresponds to the inverse of the tangent of the angle β.

$$R_s = \frac{V_0}{I_0} = \frac{1}{\text{Tg}(\beta)} \quad (\text{III.5})$$

5.4 Dynamic resistance

Dynamic resistance defines the equivalent resistance of the diode in variable mode, it is also called: differential resistance or AC resistance. Its expression is given by the ratio of the variation of the voltage at the terminals of the diode to the variation of the current flowing through it, i.e.:

$$R_d = \frac{\Delta V}{\Delta I} \quad (\text{III.6})$$

By differentiating the equation of the characteristic of a diode (II.1) we obtain:

$$\frac{dV}{dI} = \frac{e}{KT} I_s e^{\frac{eV}{KT}} = \frac{e}{KT} (I + I_s) \quad (\text{III.7})$$

$$R_d = \frac{dV}{dI} = \frac{\frac{KT}{e}}{I + I_s} = \frac{KT}{e(I + I_s)} \quad (\text{III.8})$$

Since I_s is negligible compared to I, we make the following approximation without introducing a large error.

$$R_d = \frac{KT}{eI} \quad (\text{III.9})$$

$\frac{KT}{e}$ Is the thermal voltage which for an ambient temperature it takes a value of the order of 0.026V. Therefore at T=300°K the dynamic resistance can be given by the relation:

$$R_d = \frac{0,026[V]}{I[A]} = \frac{26[mV]}{I[mA]} \quad (\text{III.10})$$

Graphically, the dynamic resistance is defined as the inverse of the tangent to the diode characteristic curve at the operating point. Figure 9 shows that the dynamic resistance of a diode can be expressed as:

$$R_d = \frac{1}{Tg(\alpha)} \quad (\text{III.11})$$

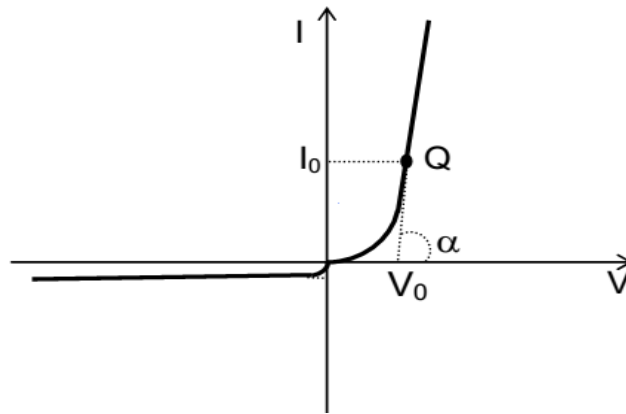


Figure III.10. Once the bias of a diode is known, then for any variation around its operating point Q, the diode behaves like a dynamic resistance R_d

5.5 Diagram equivalent to a real diode

In an electronic circuit, the diode can only be in one of the following two states: blocking state or conduction state. For the study of circuits containing diodes, it would be interesting to replace, according to its state, each of the diodes found there, by an equivalent circuit.

A passing diode is replaced by an emf generator V_0 , threshold of the diode, in series with a resistor R_d "direct resistance", as shown in figure III.11. While in the blocked state, the diode will be replaced by a resistor R_i of large value as shown in figure 11.

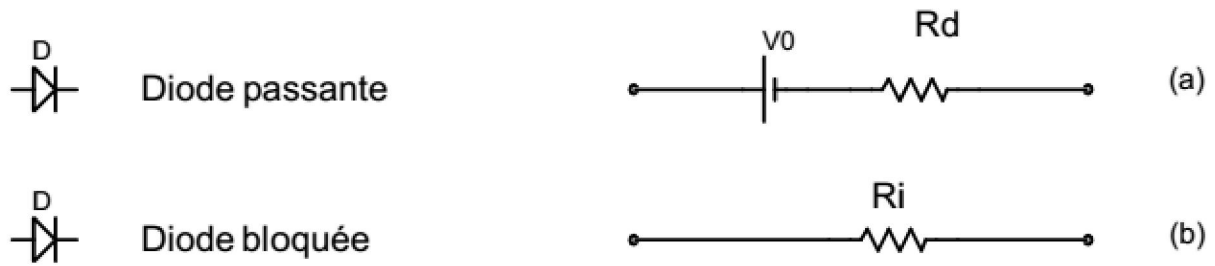


Figure III.11. Equivalent diagram for a diode. (a) case of a passing diode, (b) case of a blocked diode.

6. Half-wave rectification

Rectification can be defined as the operation that converts a bipolar signal into a unipolar signal. We can also define it as the conversion of AC into DC. Moreover, there can be two possible cases: obtaining a positive DC signal or obtaining a negative signal from an AC signal.

6.1 Conversion from alternative to positive continuous.

In this case, the circuit to be created consists of eliminating the negative part of the alternating signal and only allowing its positive part to pass. Figure II.7 shows a simple circuit that allows a sinusoidal signal to pass to a positive continuous signal. The operating principle is illustrated by the timing diagram in Figure II.8 where the diode used is assumed to be ideal.

- For $0 < t < T/2 \Rightarrow e(t) > 0 \Rightarrow i(t) > 0$ the diode is conductive. It behaves like a short circuit. Then all the positive alternation of $e(t)$ is recovered at the terminals of R.
- For $T/2 > t > T \Rightarrow e(t) < 0 \Rightarrow i(t) \text{ tendhas etre } < 0$ which blocks the diode.

The latter can in this case be replaced by an open circuit which results in a zero current $i(t)$. Consequently the voltage across R will be zero.

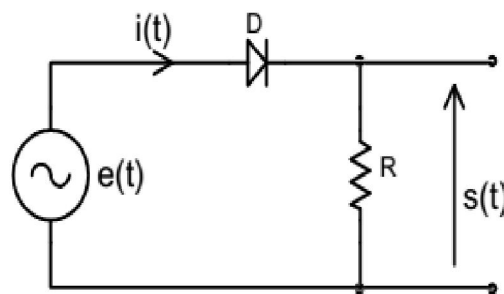


Figure III.12. Basic circuit of a half-wave rectifier. In general and especially for power supplies, $e(t)$ represents the voltage taken from the secondary of a transformer.

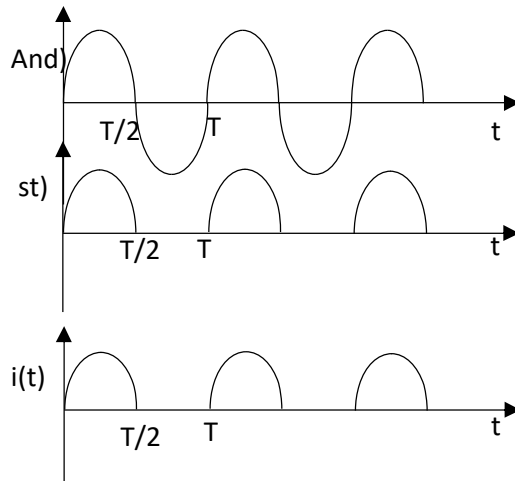


Figure III.13. This timing diagram shows how the negative alternation is suppressed. We have gone from a bipolar signal to a positive unipolar signal.

6.2 CONVERSION OF ALTERNATING TO NEGATIVE CONTINUOUS

In this case, the circuit to be created consists of eliminating the positive part of the alternating signal and letting its negative part pass. Figure III.14 shows the circuit which allows a sinusoidal signal to be rectified.

The operating principle is illustrated by the timing diagram in Figure III.14, from which we can see that the positive alternation is absent at the output.

-For $0 < t < T/2 \Rightarrow e(t) > 0 \Rightarrow i(t) = 0$ positive current from the cathode to the anode blocks the diode. The latter can in this case be replaced by an open circuit which results in a zero current $i(t)$. Consequently the voltage across R will be zero.

-For $T/2 < t < T \Rightarrow e(t) < 0 \Rightarrow i(t) < 0$, the diode is crossed by a positive current from the anode to the cathode. The diode is therefore conductive. It behaves like a short circuit. Then all the negative alternation of $e(t)$ will be recovered at the terminals of R.

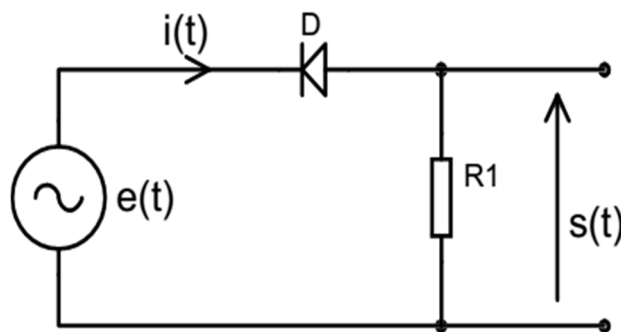


Figure III.14. With simple inversion of the diode of circuit III.12. We have arrived at having a negative unipolar output signal

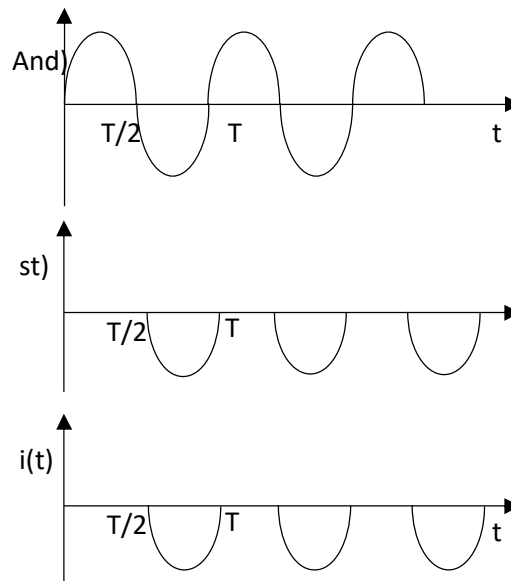


Figure III.15. This timing diagram shows how the positive alternation is suppressed. We have gone from a bipolar signal to a negative unipolar signal.

6.3 Some properties of single alternance rectification

In the remainder of this section, we consider that the diodes used are ideal.

6.3.1 Average value of a rectified signal

The mean value of a periodic function $f(t)$ of period T is defined as:

$$F = \frac{1}{T} \int_0^T f(t) dt \quad (\text{III.12})$$

Applying this formula to both cases:

CircuitFigure III.12

The average value of the output voltage

$$S_{\text{moy}} = \frac{1}{T} \int_0^T s(t) dt = \frac{1}{T} \int_0^{\frac{T}{2}} s(t) dt = \frac{S_m}{\pi}$$

$$S_{\text{moy}} = \frac{S_m}{\pi} \quad (\text{III.13})$$

The average value of the current in the resistance R

$$I_{\text{moy}} = \frac{1}{T} \int_0^T i(t) dt = \frac{1}{T} \int_0^{\frac{T}{2}} i(t) dt = \frac{I_m}{\pi}$$

$$I_{\text{moy}} = \frac{I_m}{\pi} \quad (\text{III.14})$$

S_m and I_m are the respective peak values of voltage $s(t)$ and current $i(t)$.

CircuitFigure III.14.

The average value of the output voltage

$$S_{\text{moy}} = \frac{1}{T} \int_0^T s(t) dt = \frac{1}{T} \int_0^{\frac{T}{2}} s(t) dt = -\frac{S_m}{\pi}$$

$$S_{\text{moy}} = -\frac{S_m}{\pi} \quad (\text{III.15})$$

The average value of the current in the resistance R

$$I_{\text{moy}} = \frac{1}{T} \int_0^T i(t) dt = \frac{1}{T} \int_0^{\frac{T}{2}} i(t) dt = -\frac{I_m}{\pi}$$

$$I_{\text{moy}} = -\frac{I_m}{\pi} \quad (\text{III.16})$$

S_m and I_m are the respective peak values of voltage $s(t)$ and current $i(t)$.

6.3.2 Form factor

The form factor F of an electrical quantity is the ratio of its effective value to its mean value. Its smallest value $F=1$ is obtained in the case of a purely continuous signal.

In the case of a single-wave rectified signal, the form factor is given for the two cases studied as:

$$F = \frac{S_{\text{eff}}}{S_{\text{moy}}} \quad (\text{III.17})$$

$$S_{\text{eff}} = \sqrt{\frac{1}{T} \int_0^T s(t)^2 dt} \quad (\text{III.18})$$

Circuit of theFigure III.12.

$$S_{\text{moy}} = \frac{S_m}{\pi}$$

$$S_{\text{eff}} = \frac{S_m}{2}$$

$$F = \frac{\pi}{2} = 1.57 \quad (\text{III.19})$$

Circuit of theFigure III.14

$$S_{\text{moy}} = -\frac{S_m}{\pi}$$

$$S_{\text{eff}} = -\frac{S_m}{2}$$

$$F = \frac{\pi}{2} = 1.57 \quad (\text{III.20})$$

6.3.3 Ripple rate

A ripple represents the alternating part of an electrical signal. In the case of a rectified signal, the mathematical expression representing the signal can be put in the form:

$$s(t) = S_{\text{moy}} + s_{\text{ond}}(t) \quad (\text{III.21})$$

With

S_{moy} : Average value of the $s(t)$

$s_{\text{ond}}(t)$: The ripple of $s(t)$

The ripple rate β is defined as the ratio of the effective value S_0 of the ripple to the mean value of the signal. S_{moy}

$$\beta = \frac{S_0}{S_{\text{moy}}} \quad (\text{III.22})$$

To determine the ripple rate for the case of half-wave rectification, we first calculate the effective value of the ripple of its rectified signal.

$$S_0 = \sqrt{\frac{1}{T} \int_0^T (s(t) - S_{\text{moy}})^2 dt} \quad (\text{III.23})$$

$$S_0 = \sqrt{\frac{S_m^2}{4} - \frac{S_m^2}{\pi^2}}$$

$$S_0 = \sqrt{\frac{\pi^2}{4} - 1} \quad (\text{III.23})$$

Either :

$\beta = 121\%$ for single-phase rectification feeding into a pure resistance.

6.3.4 Performance

The efficiency is used to evaluate the average power dissipated by the load due to the continuous component compared to that due to the ripple. If we take the case of single-wave rectification given in Figure III.13, the efficiency can then be defined by:

$$\eta = \frac{RI_{\text{moy}}^2}{RI_0^2} \quad (\text{III.24})$$

$$\eta = \frac{RI_{\text{moy}}^2}{RI_0^2} \quad (\text{III.25})$$

$$\eta = \frac{R_m^2}{\frac{R_m^2}{\pi^2}} = \frac{4}{\pi^2} = 0,41 \quad (\text{III.26})$$

Either

$$\eta = 41\% \quad (\text{III.27})$$

7 Full-wave rectification

Full-wave rectification also allows the transition from an alternating signal to a unipolar or continuous signal while preserving both parts of the alternating signal.

-In the case where we want to obtain a positive unipolar signal, the positive alternation of the alternating signal is preserved while the negative one is converted into positive alternation.

-In the case where we want to obtain a negative unipolar signal, the negative alternation of the alternating signal is preserved while the positive one is converted into negative alternation.

Generally, we encounter two main circuits for full-wave rectification. The choice of one of them depends on the type of application. The two circuits are:

- Full-wave rectification with mid-point transformer.
- Full-wave rectification with diode bridge or Graetz bridge.

7.1 Full-wave rectification with transformer a middle point

The diagram in Figure III.16 shows the assembly of a full-wave rectifier with a center-tapped transformer. In addition to its main functions of isolation and lowering the input voltage, the transformer in this case makes it possible to obtain at its output two signals equal in amplitude but in phase opposition as shown by the timing diagram in Figure II.14.

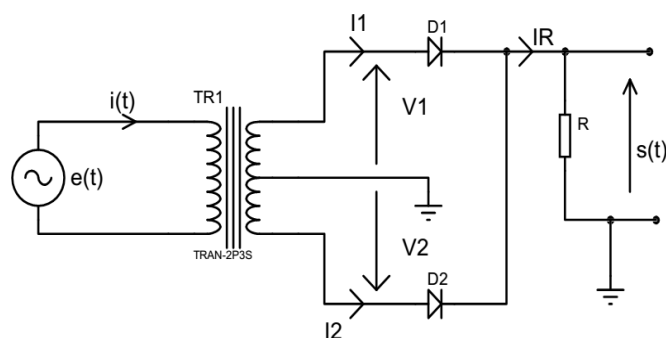


Figure III.16. The voltages v_1 and v_2 at the secondary level are equal in amplitude and they have a phase shift of π . With respect to $e(t)$, the amplitudes of v_1 and v_2 depend on the transformation ratio.

7.1.1 Operating principle

To study the operation of circuit II.1, we take a sinusoidal voltage to be rectified $e(t)$. The transformer is taken such that the voltage v_1 is in phase with $e(t)$.

$v_1 > 0 \Rightarrow D_1$ passing

For $0 < t < T/2 \Rightarrow e(t) > 0 \Rightarrow v_2 < 0 \Rightarrow D_2$ blocked

The circuit corresponding to this step is given in Figure II.12. Diode D_1 is replaced by a short circuit while D_2 is replaced by an open circuit.

The current in the load R which from the circuit of figure II.11 appears as the sum of I_1 and I_2 , will be equal in this case to I_1 .

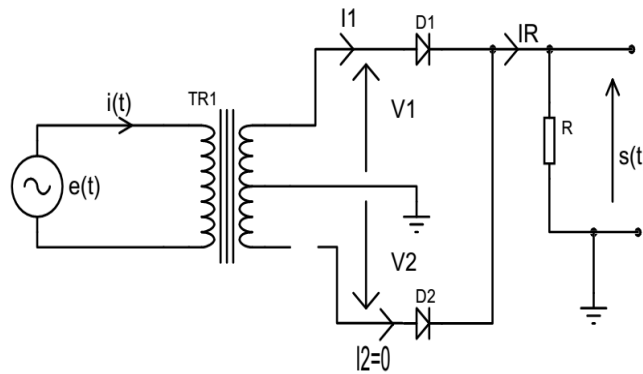


Figure III.17. Schematic equivalent to the circuit in Figure III-11 with D_1 passing replaced by a short circuit and D_2 blocked replaced by an open circuit.

For $\frac{T}{2} > t > T \Rightarrow e(t) < 0 \Rightarrow \begin{cases} v_1 < 0 \Rightarrow D_1 \text{ bloquée} \\ v_2 > 0 \Rightarrow D_2 \text{ passante} \end{cases}$

The circuit corresponding to this step is given in figure III.17. Diode D_1 is blocked, it is replaced by an open circuit. Diode D_2 is conducting, it is replaced by a short circuit. Current I_1 being zero because of the blocking of D_1 , the current in load R takes the value of I_2 .

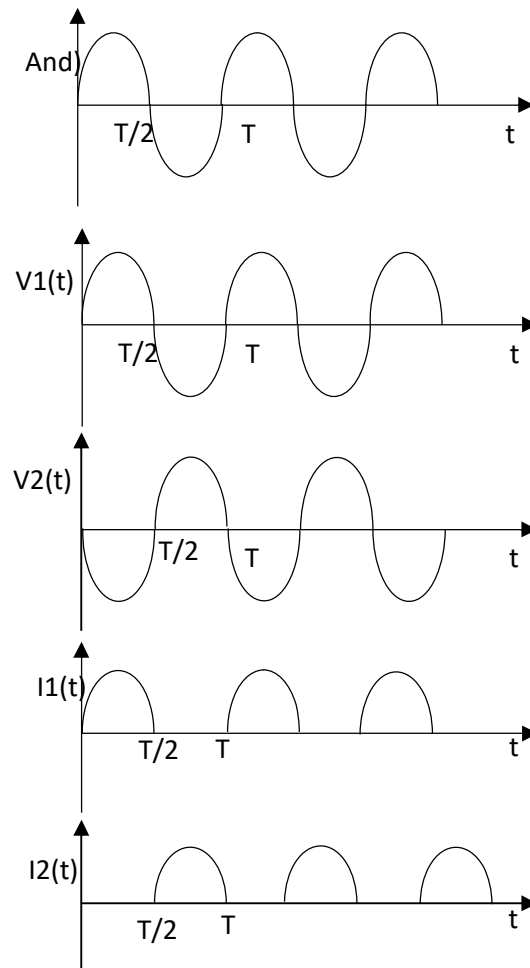
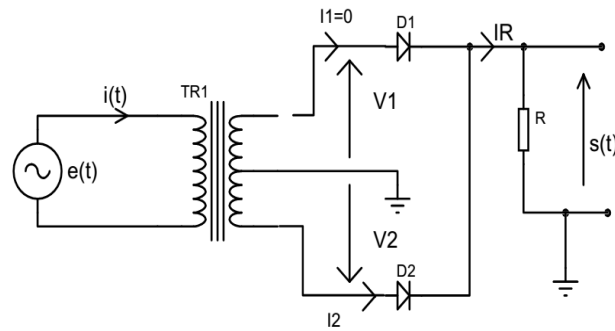


Figure III.17. The current in the load is equal to the sum of the two currents rectified respectively by D1 and D2. This makes it possible to recover the two alternations at the load level

We note from the above study that the two diodes work in an alternating manner. During each of the two alternations, only one diode is connected in series with the load R. The timing diagram in Figure III.17 shows the shape of the currents I_1 , I_2 and I_R as well as that of the curve representing $s(t)$.

7.2 Full-wave rectification with diode bridge

Full-wave rectification with bridge eliminates the need for a center-tapped transformer, which reduces the size and cost of the device. Figure III.18 shows a rectifier circuit with four diodes D1, D2, D3 and D4 connected in a bridge.

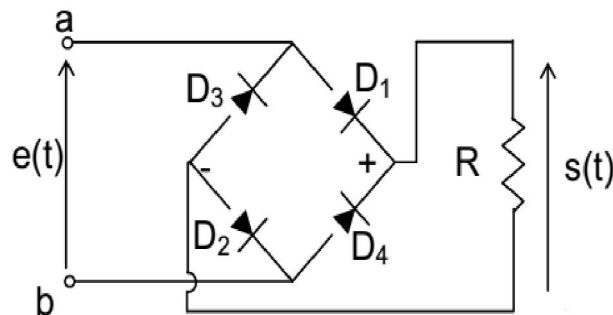


Figure III.18. Diagram of a diode bridge rectifier. The + terminal of the bridge indicates the positive current output. Indeed, whatever the sign of $e(t)$, a positive current always flows through the load in the same direction, from + to -.

7.2.1 Operating principle

•For $0 < t < T/2 \Rightarrow e(t) > 0 \Rightarrow$ a positive current flows out of terminal a and enters through terminal b. This causes D3 and D4 to be blocked and D1 and D2 to conduct. The circuit corresponding to this state is reduced to the circuit presented by the Figure III.19.

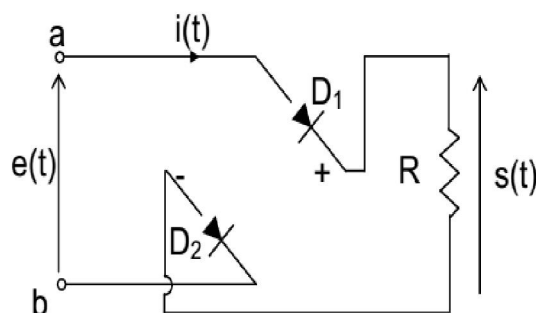


Figure III.19. In this circuit for the positive alternation of $e(t)$ only D1 and D2 enter into the operation of the rectifier. The other two diodes D3 and D4 are replaced by open circuits.

For $T/2 < t < T \Rightarrow e(t) < 0 \Rightarrow$ a positive current leaves through terminal b and enters through terminal a. D1 and D2 are blocked, but diodes D3 and D4 are conducting. The circuit corresponding to this state is shown in Figure III.20.

From the two previous cases we see that during each alternation the load R is connected in series with two diodes. Indeed, the voltage drop across the two diodes is twice the threshold of a diode. Therefore, it is recommended to avoid the use of full-wave rectification by bridge for low amplitude signals.

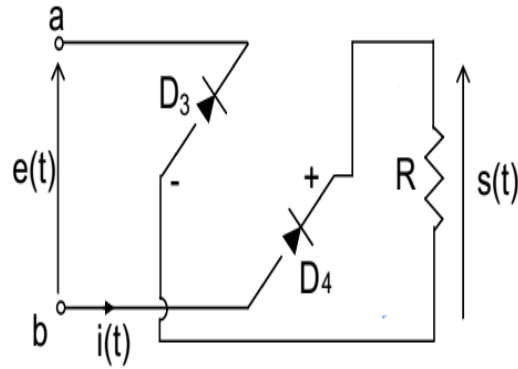


Figure III.20. During the negative alternation the active part of the circuit is limited to the two diodes D3 and D4. The other two diodes D1 and D2 are replaced by open circuits.

As can be seen from these two circuits, a positive current flowing through the load resistor R always comes out through the + terminal. This reminds us of the definition of a DC voltage generator. If we want to have a negative DC voltage, we simply take the + terminal as a reference.

7.3 Properties of full-wave rectification

7.3.1 Average value

Unlike single-wave rectification, in double-wave rectification both the negative and positive parts of the alternating signal to be rectified are recovered. Therefore, the average value of the rectified signal will be twice that found in single-wave rectification.

$$S_{\text{moy}} = \frac{1}{T} \int_0^T s(t) dt = \frac{2}{T} \int_0^{\frac{T}{2}} s(t) dt = \frac{2S_m}{\pi} \quad (\text{III.28})$$

$$S_{\text{moy}} = \frac{2S_m}{\pi} \quad (\text{III.29})$$

For the current $i(t)$ in the load we deduce its value as:

$$I_{\text{moy}} = \frac{2I_m}{\pi} \quad (\text{III.30})$$

7.3.2 Form factor

The effective S_{eff} values of the signals $s(t)$ and $i(t)$ are determined by:

$$S_{\text{eff}} = \sqrt{\frac{1}{T} \int_0^T s(t)^2 dt} = \sqrt{\frac{2}{T} \int_0^{\frac{T}{2}} s(t)^2 dt}$$

$$I_{\text{eff}} = \sqrt{\frac{1}{T} \int_0^T i(t)^2 dt} = \sqrt{\frac{2}{T} \int_0^{\frac{T}{2}} i(t)^2 dt}$$

Either

$$S_{\text{eff}} = \frac{S_m}{\sqrt{2}} \quad (\text{III.31})$$

$$I_{\text{eff}} = \frac{S_m}{\sqrt{2}} \quad (\text{III.32})$$

From equation III.17 we take F as being:

$$S_{\text{eff}} = \frac{S_m}{\sqrt{2}}$$

$$F = \frac{\frac{S_m}{\sqrt{2}}}{\frac{2S_m}{\pi}} = \frac{\pi}{2\sqrt{2}} \quad (\text{III.33})$$

Either :

$$F = 1,11 \quad (\text{III.34})$$

7.3.3 Ripple rate

In order to determine the ripple rate for full-wave rectification, we use its definition given by expression III.22.

Let us calculate the effective value of the ripple. The ripple is expressed by: S_0

$$s_{\text{ond}} = s(t) - S_{\text{moy}}$$

$$S_0 = \sqrt{\frac{1}{T} \int_0^T (s(t) - S_{\text{moy}})^2 dt}$$

$$S_0 = \frac{1}{T} \left[\int_0^T s(t)^2 dt - \int_0^{\frac{T}{2}} s(t) S_{\text{moy}} dt - \int_{\frac{T}{2}}^T s(t) S_{\text{moy}} dt + \int_0^T S_{\text{moy}}^2 dt \right]$$

Where does it come from?

$$S_0 = \sqrt{\frac{S_m^2}{2} - \frac{4S_m^2}{\pi^2}} \quad (\text{III.35})$$

Which allows us to determine the value of the ripple rate β from the formula:

$$\beta = \frac{S_0}{S_{moy}} \quad (III.36)$$

Either :

$$S_0 = \sqrt{\frac{\pi^2}{8} - 1} = 0,48 \quad (III.37)$$

7.3.4 Performance

From expression III.28 giving the definition of the yield η we deduce:

$$\eta = \frac{RI_{moy}^2}{RI_0^2} \quad (III.38)$$

$$\eta = \frac{R \frac{4I_m^2}{\pi^2}}{R \frac{I_m^2}{2}} = \frac{8}{\pi^2} = 0,81 \quad (III.39)$$

Either

$$\eta = 81\% \quad (III.40)$$

We end this part of the rectification with table II.1 which summarizes all the characteristics of the three assemblies.

	ITS		DA with transformer at midpoint		DA with a diode bridge	
	average	max	average	max	average	max
We	$\frac{E_m}{\pi}$	E_m	$\frac{2E_m}{\pi}$	$2E_m$	$\frac{E_m}{\pi}$	E_m
Id	$\frac{I_m}{\pi}$	I_m	$\frac{2I_m}{\pi}$	$2I_m$	$\frac{I_m}{\pi}$	I_m
F	157%		111%		111%	
β	121%		48%		48%	
η	41%		81%		81%	
Vcr	$\cong 0.6V$		$\cong 0.6V$		$\cong 1.2V$	
Cost	Cheaper		More expensive			
Clutter			The transformer			

Table-II.1 Comparative table between the three rectifier circuits

V_i : reverse voltage across the blocked diodes.

I_d : direct current flowing through the passing diodes.

F: form factor.

β : ripple rate.

η : yield.

V_{cr} : voltage drop due to the rectifier.

8 Zener diode

The Zener diode is a PN junction diode that is operated in reverse. Indeed, if a PN junction is reverse biased, the intensity of the internal electric field increases. At a certain value, this field will be able to break covalent bonds and thus release electron-hole pairs, this phenomenon is known as the ZENER effect. Under the effect of the high intensity of the internal electric field, the electron-hole pairs will be accelerated which, after collisions with the atoms of the crystal, will in turn release other charge carriers, which corresponds to an AVALANCHE effect. The main thing to remember from these two phenomena is the sudden increase in the reverse current. To avoid destroying the junction and to be able to exploit this ZENER phenomenon, it is enough to keep the reverse current within a very limited range.

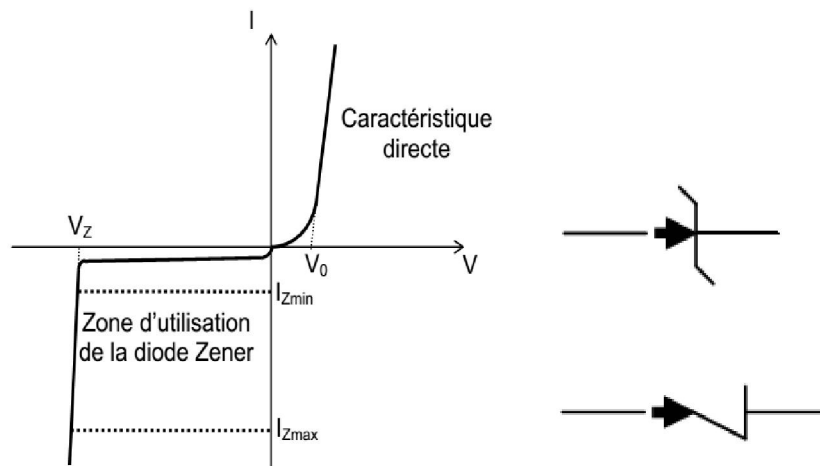


Figure III.21. The zener diode is operated in the reverse direction.

The lower limit I_{Zmin} determines the condition necessary for the zener diode to have a voltage V_Z between its terminals. The upper limit I_{Zmax} determines the maximum value of the reverse current in the diode that must not be exceeded.

From the Figure III.21, we note that in direct the zener diode behaves like an ordinary rectifier diode. On the other hand, in the reverse direction and as long as the current is between I_{Zmax} and I_{Zmin} , the voltage V_Z between the cathode and anode of the diode will be kept constant, hence its main function. As seen previously, there are two phenomena associated with the reverse bias of diodes: the zener effect which appears first followed by the avalanche effect. Indeed, there are two main categories of zener diodes: those with a low V_Z value and those with a high V_Z value.

- In the first category, it is said that the Zener effect is predominant. So if the temperature increases, it promotes the breaking of covalent bonds and consequently reduces the V_Z voltage. Zener diodes with low V_Z values ($V_Z < 6V$) are said to have a negative temperature coefficient.

- In the second category, it is said that the avalanche effect is predominant. So if the temperature increases, the oscillation of the atoms is accentuated, which reduces the mobility of the charge carriers. Consequently V_Z increases. Zener diodes with large V_Z values ($V_Z > 10V$) are said to have a positive temperature coefficient.

If the temperature factor is critical in the case of high zener voltage, it will be better to use two zener diodes in series instead of one: one with a positive temperature coefficient and the second with a negative temperature coefficient, like that the temperature effect will be cancelled.

8.1 Principle of voltage regulation by zener diode

In a circuit, voltage regulation can be defined as maintaining a voltage as invariant as possible for a given variation pattern of the other elements of the same circuit.

From its characteristic given in figure III.21, we see that for a current I maintained between I_{Zmin} and I_{Zmax} the zener diode can be used as a voltage regulator. However, for loads that require a large current the zener diode can only be a poor regulator.

Studying the circuit of Figure III.22 where the diode DZ plays the role of a voltage regulator for the R_C load.

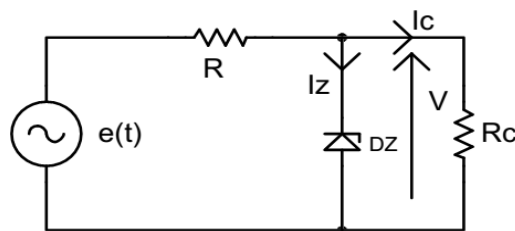


Figure III.22. The load R_C is supplied by the voltage V across DZ . As long as the current I_Z satisfies the condition $I_{Zmin} < I_Z < I_{Zmax}$ the voltage V will be constant and equal to V_Z .

In this case, for the DZ diode to work as a regulator, the following two conditions must be satisfied:

- $e(t) > \text{whatever } t.V_Z$

• $I_Z > I_{Zmin}$ the current in DZ must exceed the lower limit set by the manufacturer. A third condition to be satisfied is not to exceed the maximum current I_{Zmax} that DZ can support and which is given by the manufacturer.

For the study we consider two cases. The first case concerns a fluctuation of $e(t)$ with fixed RC. The second case is RC which fluctuates but $e(t)$ is kept fixed.

Case-1: $e(t)$ fluctuates between two limit values E_{min} and E_{max} and RC fixed. E_{min}

For it to be regulated $V = V_Z$ it is necessary to give a value to the resistance R so that:

$$V = V_Z \quad (III.41)$$

$$I_Z > I_{Zmin} \quad (III.41)$$

$$I_Z < I_{Zmax} \quad (III.42)$$

From the circuit of figure III.22 we can draw the following relations:

$$I_Z = I - I_C \quad (III.43)$$

$$I_C = \frac{V_Z}{R_C} \quad (III.44)$$

$$I_C = \frac{e(t) - V_Z}{R_C} \quad (III.45)$$

For the lower limit of , the worst case corresponds to the smallest value E_{min} of $e(t)$ from which: I_Z

$$I_C = \frac{E_{min} - V_Z}{R} - \frac{V_Z}{R_C} > I_{Zmin} \Rightarrow R < \frac{E_{min} - V_Z}{V_Z - R I_{Zmin}} R_C \quad (III.46)$$

Concerning the upper limit the unfavorable case occurs for the maximum value of $e(t)$ hence: $I_{Zmax} I_Z E_{max}$

$$I_C = \frac{E_{max} - V_Z}{R} - \frac{V_Z}{R_C} < I_{Zmax} \Rightarrow R < \frac{E_{max} - V_Z}{V_Z + R I_{Zmax}} R_C \quad (III.47)$$

Case-2: RC can take values between and $R_{cmin} R_{cmax}$ and $e(t)$ fixed at E. In this case, when there is regulation, the total current remains constant while the current varies according to the variation of $I_C R_C$

- If R_c decreases it increases and $R_c I_C I_Z$ decreases.

- If increases decreases and increases. $R_c I_C I_Z$

Therefore, the series resistance must be determined according to the two conditions: R

$$\frac{E - V_Z}{R} - \frac{V_Z}{R_{cmin}} > I_{zmin} \Rightarrow R < \frac{E - V_Z}{V_Z + R_{cmin} I_{zmin}} R_{cmin} \quad (III.48)$$

$$\frac{E - V_Z}{R} - \frac{V_Z}{R_{cmax}} < I_{zmax} \Rightarrow R > \frac{E - V_Z}{V_Z + R_{cmax} I_{zmax}} R_{cmax} \quad (III.49)$$

9. Some special diodes

Although their operating principles are based on the rectification effect, some diodes are designed for specific applications. These applications include: detection – switching – oscillation. etc.

9.1 Spiked diode

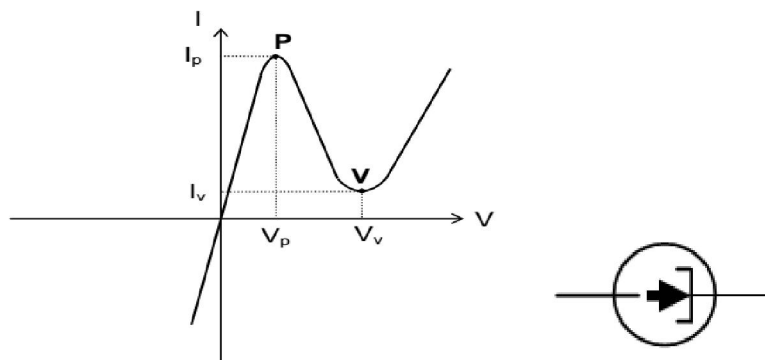
The tip diode is a metal-semiconductor junction. It is obtained by placing a fine tip in contact with a doped semiconductor substrate. Because of their chemical stability, gold, tungsten and platinum are the most commonly used metals. The use of a fine tip has the effect of reducing the dimensions of the junction, hence the name microjunction diode. Microjunction diodes

Germanium tips have a voltage threshold that can reach a few tenths of a millivolt. These diodes because of their low threshold are used in detection.

9.2 Tunnel diode

The tunnel diode is designed in the same way as a regular rectifier diode. The only difference is the doping rate, a tunnel diode has an impurity concentration that can reach 10⁵ times that of a normal diode. This high doping rate allows for very small dimensions of the transition zone. It has been found that in the case of a narrow transition zone, charge carriers cross the potential barrier without acquiring sufficient energy.

Charge carriers that do not have enough energy to cross the junction use a sort of tunnel to pass from one region to another. Referring to Figure III.23, we see that in the region the diode has a negative resistance. This particularity allows the tunnel diode to work as an oscillator, as an amplifier.



Tunnel diode symbol

Figure III.23. Characteristic and symbol of a tunnel diode. In the region of the characteristic limited by P and V the diode has a negative resistance.

9.3 Schottky diode

It is obtained by the formation of a metal-semiconductor junction. The semiconductor is silicon or gallium arsenide, usually N-doped. The metal is gold, silver, platinum, titanium or palladium. The main characteristic of a Schottky diode is its low voltage threshold and the absence of reverse current due to minority charge carriers.

The Schottky diode whose symbol is given in figure III.24 is used mainly in switching.

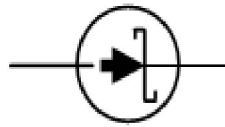


Figure III.24. Schottky diode symbol

9.4 Diode gunn

Gunn diodes have a structure identical to that of other diodes. They are obtained by sandwiching a GaAs N-type layer between two others of the same nature but heavily doped as shown in Figure III.25.

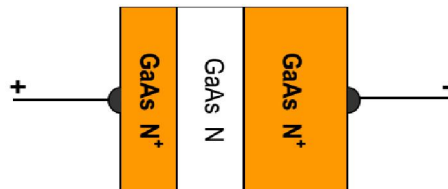


Figure III.25. Semiconductor structure of a Gunn diode. The + and – terminals correspond respectively to the anode and cathode of an ordinary diode.

Chapter IV : Bipolar Transistors

1.Introduction

The transistor is the basic element of all electronic components ranging from a small amplifier to integrated circuits. It is the union of two diodes, one is forward biased and the other reverse biased to ensure the normal operation of the transistor. It is called bipolar because the electrical conduction is done by electrons and holes. The static study is done to impose the type of operation of the transistor from the position of the rest point. The dynamic study is done by determining the parameters: the input impedance, the output impedance, the voltage and current gain. The values of these quantities determine the characteristics of the transistor and consequently its applications.

2. General information on bipolar transistors

The bipolar transistor has three input-outputs which are: the base, the emitter and the collector.

There are two types of bipolar transistors, PNP and NPN. The NPN transistor is described and symbolized as follows:

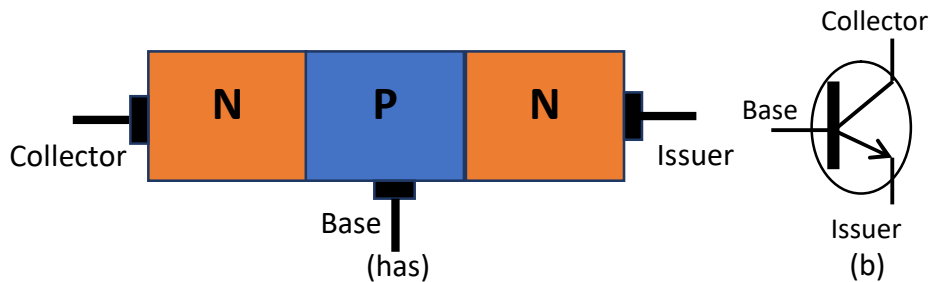


Figure IV.1. NPN transistor (a) NPN junction (b) NPN transistor symbol

The arrow in the symbol indicates the direction of the emitter current, the base and collector currents are incoming here.

Similarly the PNP transistor is described and symbolized as follows:

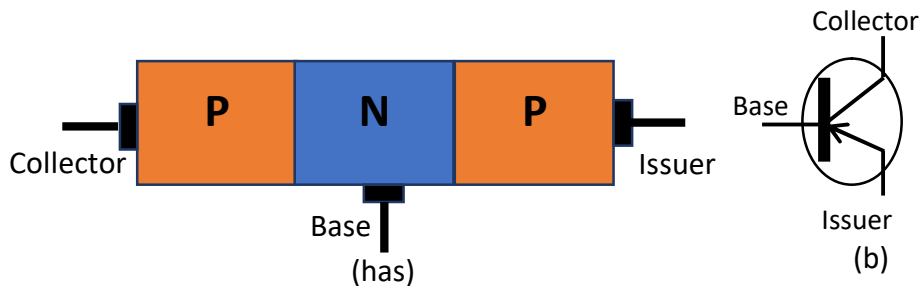


Figure IV.2. PNP transistor (a) PNP junction (b) PNP transistor symbol

The arrow in the symbol indicates the direction of the emitter current, the base and collector currents are outgoing here.

3. Transistor effect

The emitter-base NP junction is forward biased as shown in Figure IV.3 and allows the emission of a large number of electrons from the emitter. The base-collector junction is reverse biased; a space charge region (free carrier void) is then induced on either side of the junction (in dark gray in Figure IV.3) with its electric field E .

An electrostatic force of type . is then exerted on the emitted electrons present in this zone, thus drawing them towards the collector. $F = qE$

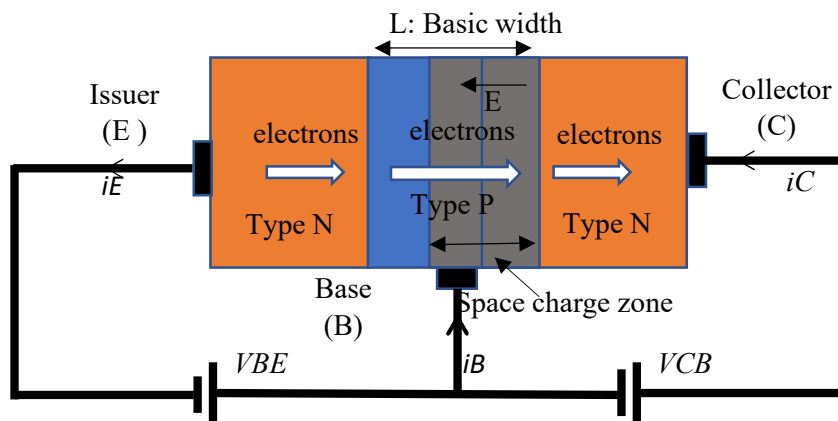


Figure IV.3. Transistor effect

The electrons cross the base all the more easily and quickly, first by diffusion and then by the entrainment effect of the electric field, as the width of the base L is narrow.

Ultimately, most of the emitted electrons are collected in the collector and the collected current is proportional to the emission current. With α denoting the proportionality coefficient less than 1 but close to 1, we have an equation that summarizes the transistor effect. $I_C = \alpha \cdot I_E$

The emitted electrons are largely recovered in the collector. A small part of the electrons joins the base to create the current I_B .

We have :

$$I_E = I_C + I_B \quad (IV.1)$$

And

$$I_C = \alpha \cdot I_E \quad (IV.2)$$

SO

$$\frac{I_C}{\alpha} = I_C + I_B \Rightarrow$$

$$I_C = \frac{\alpha}{1-\alpha} I_B \quad (IV.3)$$

And

We pose

$$\beta = \frac{\alpha}{1-\alpha} \quad (IV.4)$$

SO

$$I_C = \beta I_B \quad (IV.5)$$

And

$$I_E = (\beta + 1) I_B \approx \beta I_B \quad (IV.6)$$

Since $\beta \gg 1$

We therefore have an equation which sums up the transistor effect well: The small current injected into the base (mostly electrons here) controls the collector current which is much larger and proportional to . is the result of the amplification of (current gain) β being the current proportionality coefficient. $I_C = \beta I_B$

Order of magnitude: , $\beta \approx$ approximately 100, and in practice . $\alpha \approx 0,99$ $I_C \approx I_E$

Figure IV.4. (a) shows on the symbol of the NPN transistor the voltages V_{BE} at the input and V_{CE} at the output while Figure IV.4. (b) shows the two internal junctions of the transistor represented here in the form of two diodes.

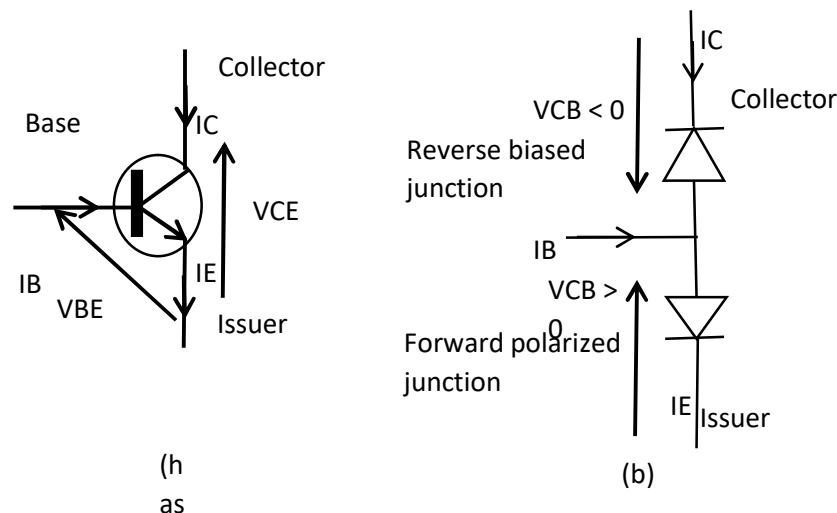


Figure.IV.4. (a) NPN transistor (b) Equivalent static diagram

For the PNP transistor, the majority carriers are not electrons but holes, whose mobility is lower under the effect of an electric field. NPN transistors will therefore be preferred to PNP in terms of speed.

4.Static model of the transistor

Modeling allows us to predict the behavior of the transistor first in static mode (DC mode) with its imposed DC voltages allowing the transistor to operate correctly then in variable dynamic mode (AC mode) around the operating point. The DC voltages imposed on the base, the collector and the emitter are essential to operate the transistor correctly: this is the polarization of the transistor. The transistor can then also operate in variable (dynamic) mode around the operating point set by the static mode. The circuit below represents the simple standard model of the NPN transistor (T model).

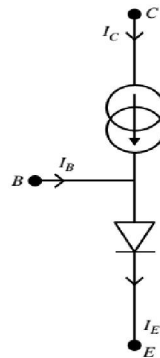


Figure IV.5. The simple standard model of an NPN transistor

Noticed : for a PNP transistor the current source is directed upwards and the diode also has its direction reversed. When the base-emitter junction is forward biased with a silicon transistor we have $V_{BE} \approx 0.6 \text{ V}$, so the diode in the model can be replaced by a constant voltage source V_{BE} .

5. Basic assemblies

In order to facilitate the study of the transistor in electronic circuits, the latter is transformed into a quadropole by pooling one of the three connections, we therefore obtain three fundamental assemblies:

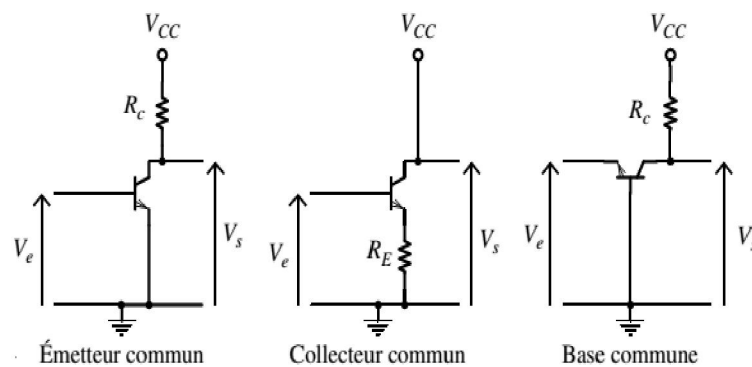


Figure.IV.6. Fundamental assemblies based on a NPN bipolar transistor

6. Types of bias circuits of a bipolar transistor

There are different types of transistor bias circuits while connecting it to continuous sources so that the transistor effect is always present. For this purpose, resistors will be associated with the bias circuits to limit the currents at each terminal of the transistor, they also allow to choose the operating point of the transistor.

7 Polarization by base resistance

7.1 Without emitter resistor RE

a) Without emitter resistor RE

- determination of the operating point

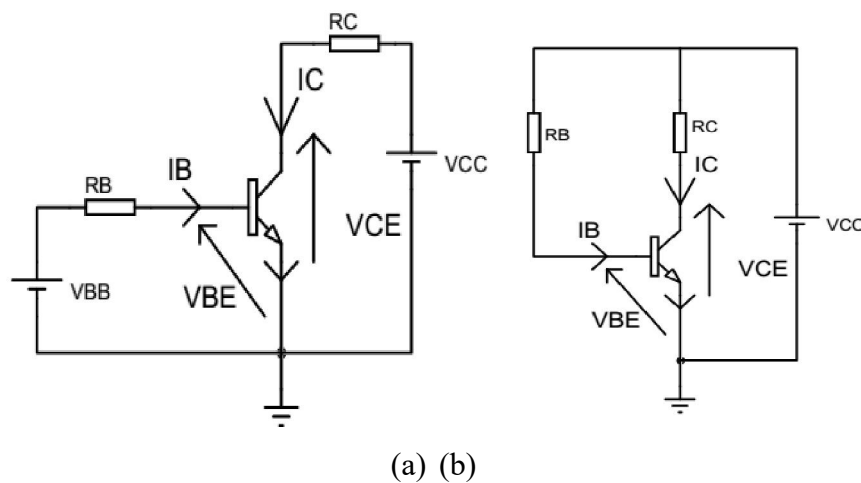


Figure IV.7. Resistance bias assembly on the base

Knowing the operating state of a circuit requires knowledge of the variables I_B , V_{BE} , I_C and V_{CE} which correspond respectively to the coordinates, in the plane $V_{CE} - I_C$ (current I_C , voltage V_{CE}), attack and load bias points.

For assembly (a):

$$V_{BB} = R_B I_B + V_{BE}$$

$$V_{CC} = R_C I_C + V_{CE}$$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

With

Equation (10) is called the static attack line. $I_B = f(V_{BE})$

Equation (11) is called the static load line. $I_C = f(V_{CE})$

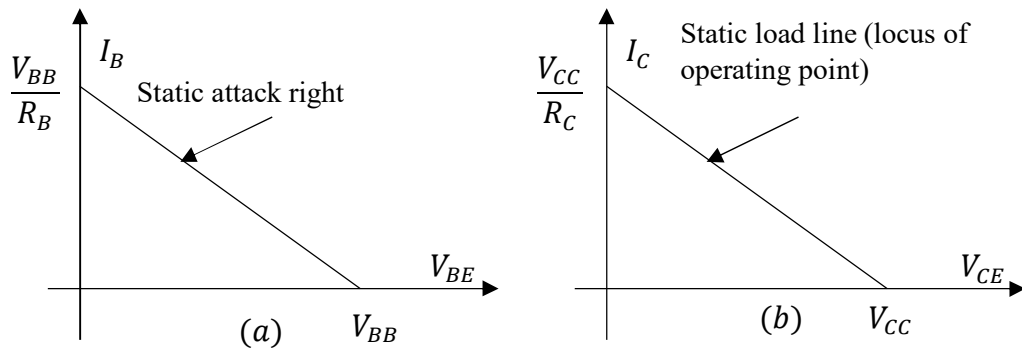


Figure IV.8. (a) static attack line, (b) static load line

For assembly (b):

$$V_{CC} = R_B I_B + V_{BE}$$

$$V_{CC} = R_C I_C + V_{CE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

Equation (10) is called the static attack line. $I_B = f(V_{BE})$

Equation (11) is called the static load line. $I_C = f(V_{CE})$

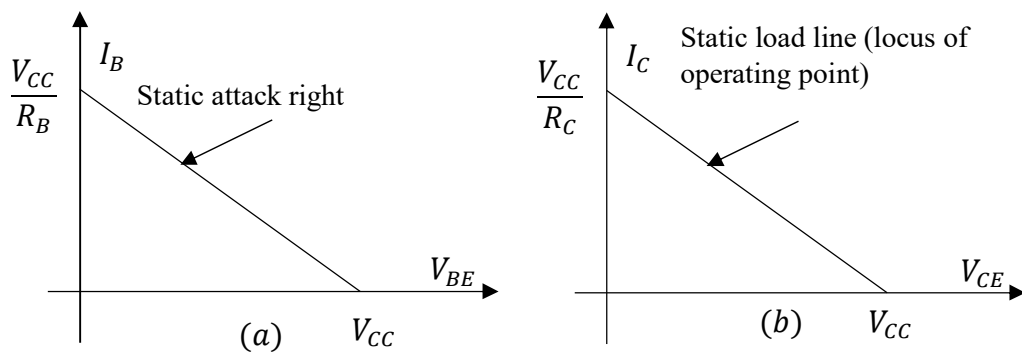


Figure IV.9. (a) static attack line, (b) static load line

Note that the coordinates (V_{BE}, I_B) and (V_{CE}, I_C) represent the operating points at the input and output respectively. The polarization problem can be posed in two ways:

- Knowing the values of the circuit components, we must determine the coordinates of the operating point Q (V_{CE} , I_C).
- Knowing the characteristics of the transistor (type and β) and the location of the operating point on the load line, we must determine the values to be given to the different resistances of the bias circuit. The operating point can also be determined graphically, simply plot the load line in the quadrant (I_C, V_{CE}) of Figure IV.10 and the intersection with the curve, for a previously determined I_B , defines the operating point.

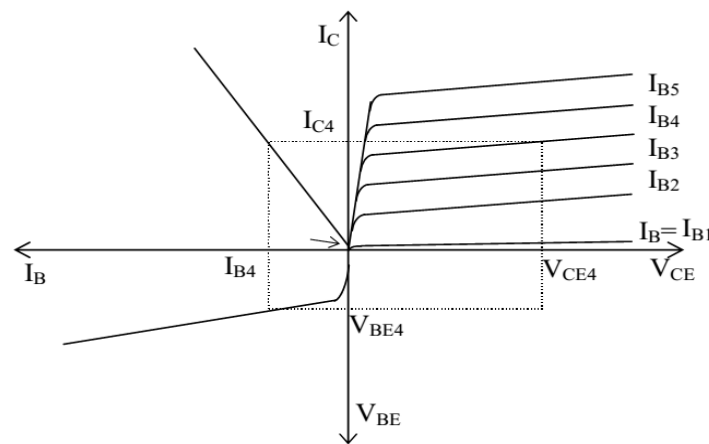


Figure IV.10. Characteristics of a common emitter transistor

Thermal Stability

We will take the case of a common emitter transistor assembly with:

$$I_C = \beta I_B + (\beta + 1) I_{CB0} \quad (IV.7)$$

I_{CB0} : Leakage current (emitter in air)

β : the current gain

The temperature rise results in the increase of multiplied by $(\beta+1)$ it causes not only a cumulative effect which produces thermal runaway and destroys the transistor but also the instability of the operating point. It is therefore necessary to stabilize it with respect to the temperature variation. I_{CB0}

If ΔI_C is the variation of I_C under the effect of temperature ΔI_C is mainly due to ΔI_{CB0} but also to ΔV_{BE}

In this case, the stability factors are defined as follows:

$$S_1 = \left. \frac{\Delta I_C}{\Delta I_{CB0}} \right|_{V_{BE}=cte} \quad (IV.8)$$

$$S_2 = \left. \frac{\Delta I_C}{\Delta V_{BE}} \right|_{I_{CB}=cte} \quad (IV.9)$$

S1 is the most important factor because it depends on minority charge carriers whose origin is the temperature effect.

$S_2(\text{mA/V}) < 0$ Therefore the stability will be all the greater as the stability factors have low absolute values.

In the case of the circuit in Fig. 2 the coefficients of thermal stability are obtained by the following calculation principle

$$I_C = \beta I_B + (\beta + 1)I_{CB0} \Rightarrow \Delta I_C = \beta \Delta I_B + (\beta + 1)\Delta I_{CB0}$$

From the equation (), $V_{BE} = -R_B I_B + V_{BB} \Rightarrow \Delta V_{BE} = -R_B \Delta I_B$

$$\Rightarrow \Delta I_B = -\frac{\Delta V_{BE}}{R_B}$$

SO

$$\Delta I_C = -\frac{\beta}{R_B} \Delta V_{BE} + (\beta + 1)\Delta I_{CB0}$$

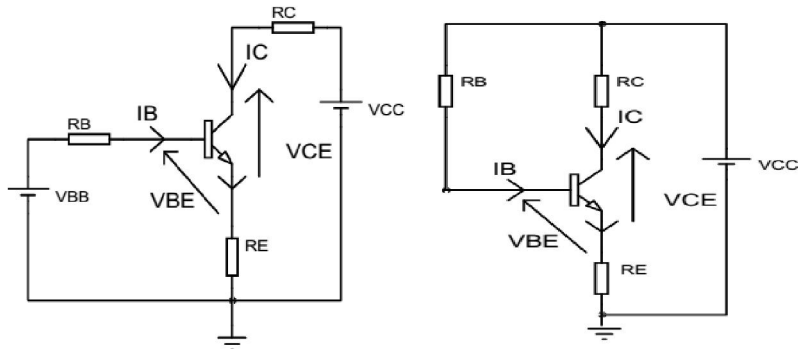
By identification with equations (13) and (14) we have:

$$S_1 = (\beta + 1)$$

$$S_2 = -\frac{\beta}{R_B}$$

This assembly is not stable because it is very high while it can be very low for very large values. $S_1 S_2 R_B$

7.2 Polarization by base resistance with RE



(a) (b)

Figure IV.11. Basic polarization setup with a RE

The principle of calculating the operating point is done in the same way as in the previous cases where we must first find the expressions of the equations of the attack line and the load line.

Assembly (a):

$$V_{BB} = R_B I_B + R_E I_E + V_{BE}$$

We have

$$I_E = (\beta + 1) I_B \approx \beta I_B$$

SO

$$V_{BB} = R_B I_B + R_E \beta I_B + V_{BE}$$

$$V_{BB} = (R_B + \beta R_E) I_B + V_{BE}$$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B + \beta R_E}$$

From the output mesh we have:

$$V_{CC} = R_C I_C + R_E I_E + V_{CE}$$

We have

$$I_E \approx I_C$$

SO

$$V_{CC} = R_C I_C + R_E I_C + V_{CE}$$

$$V_{CC} = (R_C + R_E) I_C + V_{CE}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E}$$

$$I_C = f(V_{CE}) = -\frac{V_{CE}}{R_C + R_E} + \frac{V_{CC}}{R_C + R_E}$$

This last equation is called the static load line.

Assembly (b):

$$V_{CC} = R_B I_B + R_E I_E + V_{BE}$$

We have

$$I_E = (\beta + 1)I_B \approx \beta I_B$$

SO

$$V_{CC} = R_B I_B + R_E \beta I_B + V_{BE}$$

$$V_{CC} = (R_B + \beta R_E) I_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_E}$$

From the output mesh we have:

$$V_{CC} = R_C I_C + R_E I_E + V_{CE}$$

We have

$$I_E \approx I_C$$

SO

$$V_{CC} = R_C I_C + R_E I_C + V_{CE}$$

$$V_{CC} = (R_C + R_E) I_C + V_{CE}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E}$$

$$I_C = f(V_{CE}) = -\frac{V_{CE}}{R_C + R_E} + \frac{V_{CC}}{R_C + R_E}$$

This last equation is called the static load line.

Thermal stability

A similar calculation gives:

$$I_C = \beta I_B + (\beta + 1)I_{CB0} \Rightarrow \Delta I_C = \beta \Delta I_B + (\beta + 1)\Delta I_{CB0}$$

From the equation (), $V_{BE} = -R_B I_B + V_{BB} - R_E (I_B + I_C) \Rightarrow \Delta V_{BE} = -(R_B + R_E)\Delta I_B - R_E \Delta I_C$

$$\Rightarrow \Delta I_B = -\frac{\Delta V_{BE} + R_E \Delta I_C}{R_B + R_E}$$

SO

$$\Delta I_B = -\frac{\beta}{R_B + R_E(\beta + 1)} \Delta V_{BE} - (\beta + 1) \frac{R_B + R_E}{R_B + R_E(\beta + 1)} \Delta I_{CB0}$$

By identification with the equations

SO

$$\Delta I_C = -\frac{\beta}{R_B} \Delta V_{BE} + (\beta + 1)\Delta I_{CB0}$$

By identification with equations (13) and (14) we have:

$$S_1 = -(\beta + 1) \frac{R_B + R_E}{R_B + R_E(\beta + 1)}$$

$$S_2 = -\frac{\beta}{R_B + R_E(\beta + 1)}$$

Digital application:

For $\beta=100$, $R_B=100K\Omega$

$R_E=1K\Omega \Rightarrow S_1=50$

$R_E=10K\Omega \Rightarrow S_1=10$

As a conclusion we can remember that the more it increases and the more it decreases, the more the circuit is thermally stable. $R_E S_1$

I-3-2 Polarization by resistances between base and collector

This polarization can be done by the following typical assembly:

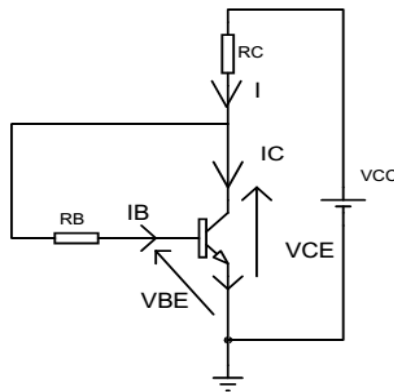


Figure IV.12. Polarization by resistance between base and collector

$$V_{CC} = R_C I + R_B I_B + R_E I_E + V_{BE}$$

$$I_E = (\beta + 1) I_B \approx \beta I_B$$

And

$$I = I_C + I_B \approx I_C = \beta I_B$$

Since

$$I_C \gg I_B$$

$$V_{CC} = R_C I + R_B I_B + R_E \beta I_B + V_{BE}$$

$$V_{CC} = \beta R_C I_B + R_B I_B + R_E \beta I_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + R_C + R_E}$$

From the output mesh we have:

$$V_{CC} = R_C I + R_E I_E + V_{CE}$$

We have

$$I_E \approx I_C \approx I$$

SO

$$V_{CC} = R_C I_C + R_E I_C + V_{CE}$$

$$V_{CC} = (R_C + R_E) I_C + V_{CE}$$

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + R_E}$$

$$I_C = f(V_{CE}) = -\frac{V_{CE}}{R_C + R_E} + \frac{V_{CC}}{R_C + R_E}$$

This last equation is called the static load line.

Thermal stability

A similar calculation gives:

$$I_C = \beta I_B + (\beta + 1) I_{CB0} \Rightarrow \Delta I_C = \beta \Delta I_B + (\beta + 1) \Delta I_{CB0}$$

From the circuit we derive the expression of V_{BE} as a function of the currents and I_B, I_C

$$V_{BE} = -R_B I_B + V_{BB} - R_C (I_B + I_C) \Rightarrow \Delta V_{BE} = -(R_B + R_C) \Delta I_B - R_C \Delta I_C$$

$$\Rightarrow \Delta I_B = -\frac{\Delta V_{BE} + R_C \Delta I_C}{R_B + R_C}$$

SO

$$\Delta I_B = -\frac{\beta}{R_B + R_C(\beta + 1)} \Delta V_{BE} - (\beta + 1) \frac{R_B + R_C}{R_B + R_C(\beta + 1)} \Delta I_{CB0}$$

$$S_1 = -(\beta + 1) \frac{R_B + R_C}{R_B + R_C(\beta + 1)}$$

$$S_2 = -\frac{\beta}{R_B + R_C(\beta + 1)}$$

In the case where $\beta \gg 1$, this leads to ≈ 1 a significant improvement in thermal stability is noted. $R_B R_C S_1$

7.3 Polarization by a divider bridge

In this case we can use the assembly below

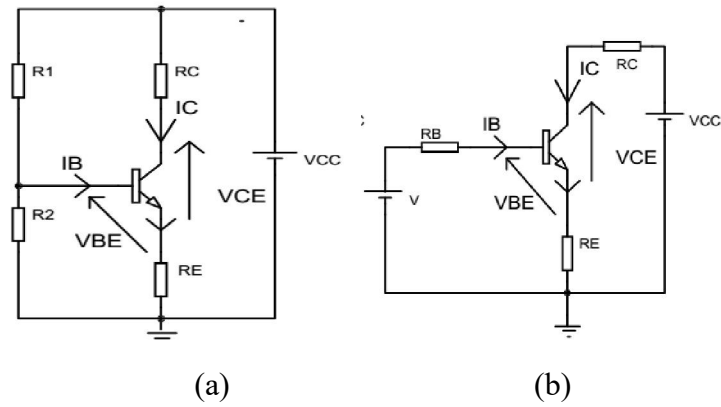


Figure IV.13. Polarization by a divider bridge

The assembly of figure (a) can be replaced by its Thevenin equivalent seen by the resistor R2 or seen by the base. We will have a voltage divider as shown in the following figure:

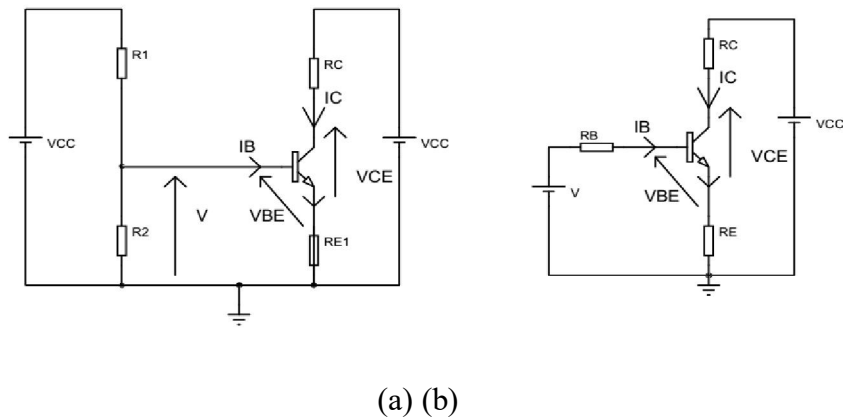


Figure IV.14. Simplification of the divider bridge assembly

The voltage divider can give us

$$V = \frac{R_2}{R_1 + R_2} V_{CC}$$

We short-circuit the generator V_{CC} ; then the Thevenin resistance seen by R2 will be

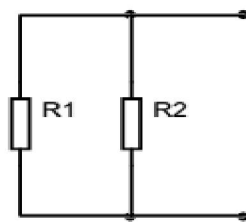


Figure IV.15. Thevenin resistance

Then the Thevenin resistance will be:

$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

The equivalent circuit of the divider bridge is similar to that of the bias circuit by a base resistor with a resistor at the emitter.

Assembly (a):

$$V = R_B I_B + R_E I_E + V_{BE}$$

We have

$$I_E = (\beta + 1) I_B \approx \beta I_B$$

SO

$$V = R_B I_B + R_E \beta I_B + V_{BE}$$

$$V = (R_B + \beta R_E) I_B + V_{BE}$$

$$I_B = \frac{V - V_{BE}}{R_B + \beta R_E}$$

From the output mesh we have:

$$V_{CC} = R_C I_C + R_E I_E + V_{CE}$$

We have

$$I_E \approx I_C$$

SO

$$V_{CC} = R_C I_C + R_E I_C + V_{CE}$$

$$V_{CC} = (R_C + R_E) I_C + V_{CE}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E}$$

$$I_C = f(V_{CE}) = -\frac{V_{CE}}{R_C + R_E} + \frac{V_{CC}}{R_C + R_E}$$

This last equation is called the static load line.

Thermal stability

A similar calculation gives:

As can be seen, the calculation of the stability coefficients is obtained in an identical way to those obtained in the case of figure 2, it suffices to replace in both expressions and the resistance R_B by the equivalent resistance of Thevenin. We will have $S_1 S_2 R_{th}$

$$\Delta I_B = -\frac{\beta}{R_{th} + R_E(\beta + 1)} \Delta V_{BE} - (\beta + 1) \frac{R_{th} + R_E}{R_{th} + R_E(\beta + 1)} \Delta I_{CB0}$$

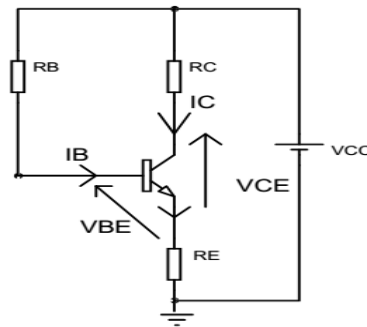
$$S_1 = (\beta + 1) \frac{R_{th} + R_E}{R_{th} + R_E(\beta + 1)}$$

$$S_2 = -\frac{\beta}{R_{th} + R_E(\beta + 1)}$$

Exercises

Exercise 1:

Given the circuit in the figure below



The transistor is made of silicon and has a static current gain $\beta=100$. We give

$R_B=220K$; $R_C=1.2K$; $R_E=0.47K$; $V_{CC}=15V$. We ask to:

1. Determine the operating point Q.
2. plot the static load line as well as the static attack line.

Correction 1:

In order to work easily and not to drag the numerical values, let's give letters to the different resistances and electrical quantities of the circuit.

From the input mesh we have:

$$V_{CC} = R_B I_B + R_E I_E + V_{BE}$$

We have

$$I_E = (\beta + 1)I_B \approx \beta I_B$$

SO

$$V_{CC} = R_B I_B + R_E \beta I_B + V_{BE}$$

$$V_{CC} = (R_B + \beta R_E)I_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_E}$$

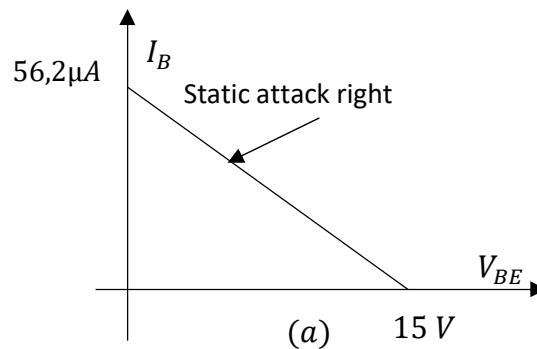
$$I_B = -\frac{V_{BE}}{R_B + \beta R_E} + \frac{V_{CC}}{R_B + \beta R_E}$$

$$I_B = -\frac{V_{BE}}{220000 + 100 \times 0,47 \times 1000} + \frac{15}{220000 + 100 \times 0,47 \times 1000}$$

$$I_B = -\frac{V_{BE}}{267000} + \frac{15}{267000}$$

This last equation and the static attack line

Representation of the static attack line



AN:

The silicon transistor then we take $V_{BE} = 0,6$

$$I_B = \frac{15 - 0,6}{220000 + 100 \times 0,47 \times 1000} = \frac{14,4}{220000 + 100 \times 0,47 \times 1000} = 53,9 \mu A$$

From the output mesh we have:

$$V_{CC} = R_C I_C + R_E I_E + V_{CE}$$

We have

$$I_E \approx I_C$$

SO

$$V_{CC} = R_C I_C + R_E I_C + V_{CE}$$

$$V_{CC} = (R_C + R_E) I_C + V_{CE}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E}$$

Calculation of V_{CE}

$$I_C = \beta I_B$$

AN:

$$I_C = 100 \times 53,9 \times 10^{-6} = 5,39 \text{ mA}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E} =$$

SO

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

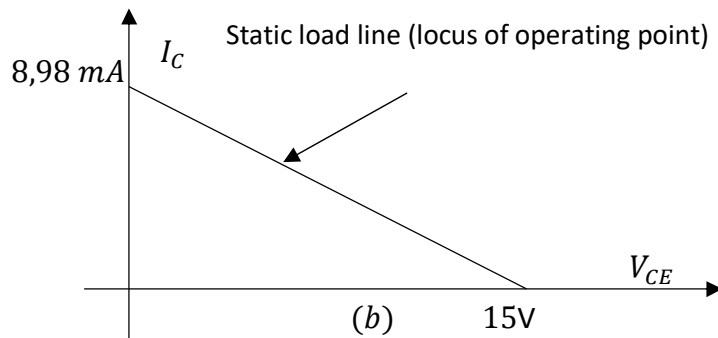
AN:

$$V_{CE} = 15 - 5,39 \times 10^{-3}(1,2 \times 10^3 + 0,47 \times 10^3) = 6 \text{ V}$$

$$I_C = f(V_{CE}) = -\frac{V_{CE}}{R_C + R_E} + \frac{V_{CC}}{R_C + R_E}$$

$$I_C = -\frac{V_{CE}}{1,67 \times 10^3} + \frac{15}{1,67 \times 10^3}$$

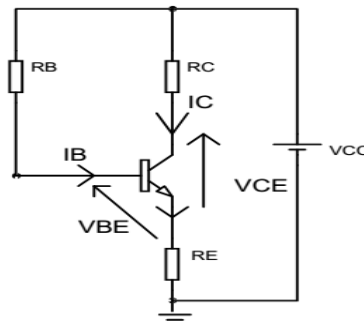
This last equation is called the static load line.



The operating point is Q (6V, 5.39mA)

Exercise 2:

In the circuit in the figure below, the transistor is biased by a base resistor. The silicon transistor with a static current gain $\beta=150$.



We give $R_C=2\text{K}$; $R_E=1\text{K}$; $V_{CC}=12\text{V}$. We are asked to determine the value that must be given to the base resistance R_B so that the operating point is in the middle of the static load line.

Corrected

From the output mesh we have:

$$V_{CC} = R_C I_C + R_E I_E + V_{CE}$$

We have

$$I_E \approx I_C$$

SO

$$V_{CC} = R_C I_C + R_E I_C + V_{CE}$$

$$V_{CC} = (R_C + R_E) I_C + V_{CE}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E}$$

$$I_C = -\frac{V_{CE}}{R_C + R_E} + \frac{V_{CC}}{R_C + R_E}$$

$$I_C = -\frac{V_{CE}}{2 \times 10^3 + 1 \times 10^3} + \frac{12}{2 \times 10^3 + 1 \times 10^3}$$

$$I_C = -\frac{V_{CE}}{3 \times 10^3} + \frac{12}{3 \times 10^3}$$

For we will have $I_C = 0$ $V_{CE} = 12$ V

For we will have $V_{CE} = 0$ $I_C = 4$ mA

The operating point is at the midpoint of the static load line i.e. $Q\left(\frac{V_{CE}}{2}, \frac{I_C}{2}\right) = Q(V_{CE} = 6V, I_C = 2mA)$.

Calculation of I_B

$$I_C = \beta I_B \Rightarrow I_B = \frac{1}{\beta} I_C = \frac{1}{150} 2 \times 10^{-3}$$

AN:

$$I_B = 13,3 \times 10^{-6} = 13,3 \mu A$$

From the input mesh we have

$$V_{CC} = R_B I_B + R_E \beta I_B + V_{BE}$$

$$V_{CC} = (R_B + \beta R_E) I_B + V_{BE}$$

$$R_B + \beta R_E = \frac{V_{CC} - V_{BE}}{I_B}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} - \beta R_E$$

$$R_B = \frac{12 - 0,6}{13,3 \times 10^{-6}} - 150 \times 1 \times 10^3 = 100,7142 k\Omega$$

8. Transistors dynamic study

In the field of electronics, frequency is a very important parameter. In the design of circuits, this parameter must always be taken into consideration. Electronic components are generally characterized by their values, their powers, the range of working temperatures and especially by the frequency band of use. In this course, we limit the study to small signals so that transistor-based circuits operate in linear mode. In the linear regime, the study of an amplifier circuit becomes very simple by applying the superposition theorem. Thus, the study will be separated into a static study and a dynamic study.

Static study = transistor polarization; static charge line and calculation of the operating point.

Dynamic study = Calculation of voltage gain, current gain, input impedance, output impedance etc.

In this chapter we study the dynamic aspect of a bipolar transistor while finding its schematic parameters and the effect of each element on the proper operation of the transistor.

Firstly, the hybrid elements of the transistor are determined as well as its equivalent diagram in dynamics or for small signals. Secondly, the effect and conditions of installing several amplification stages in cascade are demonstrated as well as the parameters to be checked to improve the efficiency of each stage and subsequently of the entire assembly. Finally, the three fundamental assemblies are detailed, which are the common emitter assembly, the common collector assembly and the common base assembly.

8.1 Equivalent diagram of a transistor in dynamic mode (AC).

Let us take as an example the common emitter assembly as shown in the figure below.

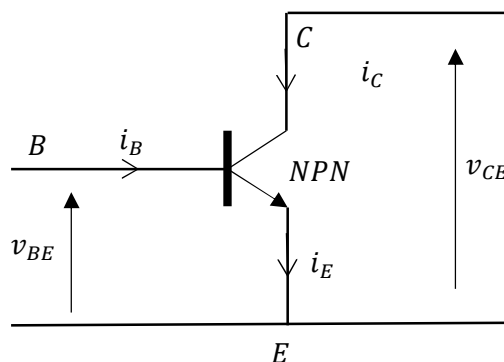


Figure IV.16. Common emitter transistor

The electrical quantities (voltage and current) found at the different terminals of the transistor are actually composed of two components. A continuous component due to the bias circuit and

an alternating component due to the useful signal. So we can represent these different electrical quantities as:

$$v_{BE} = v_{be} + V_{BE} \text{ Voltage between base and emitter}$$

$$i_B = i_b + I_B \text{ Base current}$$

$$v_{CE} = v_{ce} + V_{CE} \text{ Voltage between collector and emitter}$$

$$i_C = i_c + I_C \text{ Collector current}$$

With and continuous components V_{BE}, I_B, V_{CE}, I_C

v_{be}, i_b , and alternative components v_{ce}, i_c

We also have a dependence between these electrical quantities which can be given by:

$$v_{BE} = f(i_B, v_{CE})$$

$$i_C = g(i_B, v_{CE})$$

By differentiating these two quantities we obtain:

$$\Delta v_{BE} = \frac{\partial f}{\partial i_B} \Delta i_B + \frac{\partial f}{\partial v_{CE}} \Delta v_{CE}$$

$$\Delta i_C = \frac{\partial g}{\partial i_B} \Delta i_B + \frac{\partial g}{\partial v_{CE}} \Delta v_{CE}$$

Knowing that

$$\Delta v_{BE} = v_{be} \text{ et } \Delta i_B = i_b$$

$$\Delta v_{CE} = v_{ce} \text{ et } \Delta i_C = i_c$$

So the equations become

$$v_{be} = \frac{\partial f}{\partial i_B} i_b + \frac{\partial f}{\partial v_{CE}} v_{ce}$$

$$i_c = \frac{\partial g}{\partial i_B} i_b + \frac{\partial g}{\partial v_{CE}} v_{ce}$$

By analogy with the study of quadrupoles, the vectors are linked together by a matrix H such that: $\begin{bmatrix} v_{be} \\ i_c \end{bmatrix}$ et $\begin{bmatrix} i_b \\ v_{ce} \end{bmatrix}$

$$\begin{cases} v_{be} = h_{11} i_b + h_{12} v_{ce} \\ i_c = h_{21} i_b + h_{22} v_{ce} \end{cases}$$

With

$$h_{11} = \frac{\partial f}{\partial i_B} = \left. \frac{\Delta v_{BE}}{\Delta i_B} \right|_{v_{CE}=cte} \quad h_{12} = \frac{\partial f}{\partial v_{CE}} = \left. \frac{\Delta v_{BE}}{\Delta v_{CE}} \right|_{i_B=cte}$$

$$h_{21} = \frac{\partial g}{\partial i_B} = \left. \frac{\Delta i_C}{\Delta i_B} \right|_{v_{CE}=cte} \quad h_{22} = \frac{\partial g}{\partial v_{CE}} = \left. \frac{\Delta i_C}{\Delta v_{CE}} \right|_{i_B=cte}$$

From the system of equations given by equations (4) and (5), we can deduce the equivalent circuit of a transistor for small signals by studying the input and output characteristics:

8.2 Input characteristics

From equation -5- we deduce that the input is equivalent to a single mesh circuit with i_b as mesh current, mesh resistance h_{11} while $h_{12}v_{ce}$ is a controlled voltage source; h_{12} represents the internal reaction coefficient of the transistor ($h_{12} \approx 0$). Therefore, between base and emitter the transistor can be seen as the circuit of figure 2.

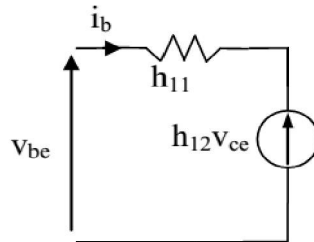


Figure IV.17. Equivalent circuit seen from the input

8.3 Output characteristics

From equation -6- we deduce that the output is equivalent to a single-node circuit with two branches having i_c as the total current, resistance of one branch across which we have the voltage v_{ce} while the second branch is a controlled current source whose electromotive current is given by $h_{21}i_b$; h_{21} represents the current gain of the transistor in common emitter (h_{21} is generally very large). Therefore, between collector and emitter the transistor can be seen as the circuit of figure 3. h_{22}^{-1}

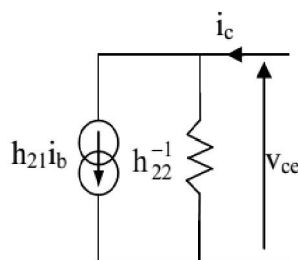


Figure IV.18. Equivalent circuit seen from the output

Thus the association of the two characteristics (input and output) gives us the overall diagram following figure 4.

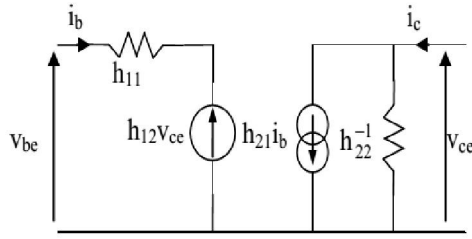


Figure IV.19. Equivalent AC circuit of a transistor in small signal mode (Linear mode)

The coefficient h_{12} is generally taken as zero for its very small values which considerably simplifies the equivalent circuit of the transistor in linear mode, the circuit of figure 4 will be replaced in this case by the circuit of figure 5.

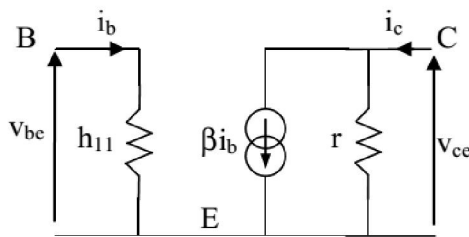


Figure IV.20. Equivalent diagram of a transistor with $h_{12}=0$ and $r=1/h_{22}$

8.4 Different basic assemblies of a bipolar transistor

8.4.1 Common emitter with decoupled RE

Let us take as a circuit a common emitter assembly with decoupled RE; RE intervenes in static but not in dynamic where it is short-circuited by the capacitor CE whose impedance at the working frequency is considered to be zero.

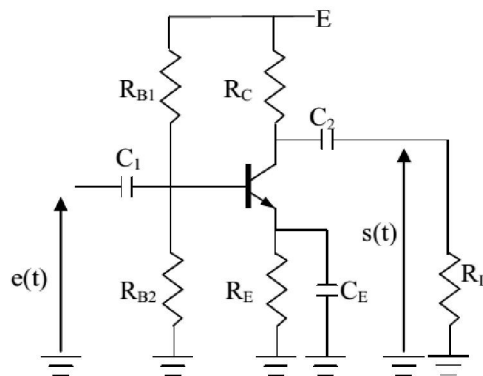


Figure IV.21. Schematic of a common emitter stage

Figure 6 shows the schematic of a single-stage low-frequency amplifier loaded by an RL resistor. It is essential to determine the maximum output variation range during the design stage of an amplifier in order to avoid the distortion problem. Therefore, the plotting of the dynamic

load line is essential. The load line is the locus of variation of the output signal around the operating point, and it is defined by the linear relation $i_c = f(v_{ce})$.

Let us take the case of the amplifier in Figure IV.21 whose AC output only ($E = 0$) gives us Figure IV.22 where:

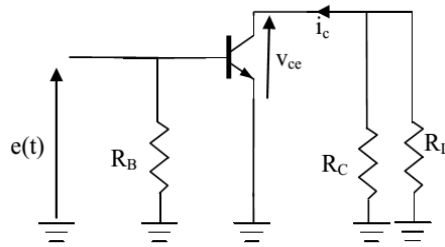


Figure IV.22. Equivalent alternative diagram of assembly 6 to determine the dynamic load line

We assume that the static study is already done, the static load line of the circuit concerned is given by

$$I_C = -\frac{V_{CE}}{R_C + R_E} + \frac{E}{R_C + R_E}$$

The operating point calculated in statics is given by $Q(I_0, V_0)$. In this case, let us move on to plotting the dynamic load line, the equation of which is:

$$i_c = -\frac{v_{ce}}{R_C // R_L}$$

This is the equation of a straight line passing through the origin which is here the operating point $Q(V_0, I_0)$. To draw the two static and dynamic load lines in the same plane and relative to the origin 0; let us show the translations I_0 and V_0 in the equation.

$$i_c - I_0 = -\frac{v_{ce} - V_0}{R_C // R_L}$$

$$i_c = -\frac{v_{ce} - V_0}{R_C // R_L} + \frac{V_0}{R_C // R_L} + I_0$$

It is a straight line that passes through the operating point. This operating point determined in statics, defines the point of intersection of the two static and dynamic load lines whose plots for the circuit of the Figure IV.21 are given in the Figure IV.23.

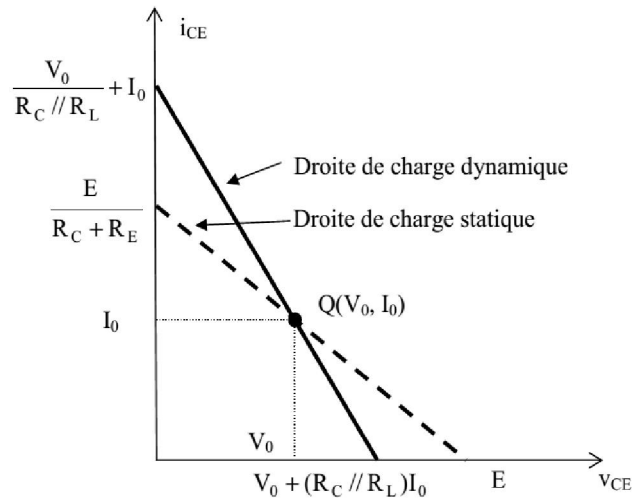


Figure IV.23. Plotting the static and dynamic load lines

As we can see, the load intervenes in the dynamic study, something that is not done during the static study in the case of capacitive coupling. Before determining these characteristics, we must first replace the transistor with its equivalent AC circuit (we short-circuit the DC voltage source ($E=0$) and leave the AC excitation $e(t)$) as shown in Figure IV.24.

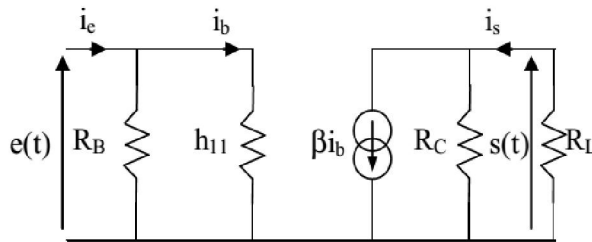


Figure IV.24. Equivalent diagram for small signals of circuit 6

The coupling capacitors (such as C_1 and C_2) and decoupling capacitors (such as C_E) are calculated so that their impedances are negligible at the minimum working frequency. Therefore, all capacitors will be replaced, in AC, by short-circuit capacitors.

Voltage gain

The voltage gain is given by:

$$A_v = \frac{s}{e}$$

$$s = -(R_C // R_L) \cdot \beta \cdot i_b$$

$$e = h_{11} i_b$$

More precisely we find:

$$A_v = -\frac{\beta(R_C // R_L)}{h_{11}}$$

Current gain

The current gain is given by:

$$A_i = \frac{i_s}{i_e}$$

$$i_s = \frac{\beta R_C}{R_C + R_L} i_b$$

$$i_s = \frac{R_B + h_{11}}{R_B} i_b$$

$$A_i = \frac{\beta R_C}{R_C + R_L} \frac{R_B}{R_B + h_{11}}$$

• **Input impedance**

This is the ratio between the input voltage and the input current:

$$Z_e = \frac{e}{i_e}$$

$$i_e = \frac{e}{R_B} + \frac{e}{h_{11}}$$

$$Z_e = R_B // h_{11} = \frac{R_B h_{11}}{R_B + h_{11}}$$

• **Output impedance**

This is the ratio of output voltage to output current with the input shorted. This is what is translated by the equation below:

$$Z_s = \left. \frac{s}{i_s} \right|_{e=0}$$

Let us carry the condition $e(t)=0$ into the circuit and disconnect the load from the circuit because it is the latter which sees its driver circuit as being a voltage source of impedance Z_S , in the case of Thevenin's theorem or a current source of impedance Z_S , in the case of the Norton generator.

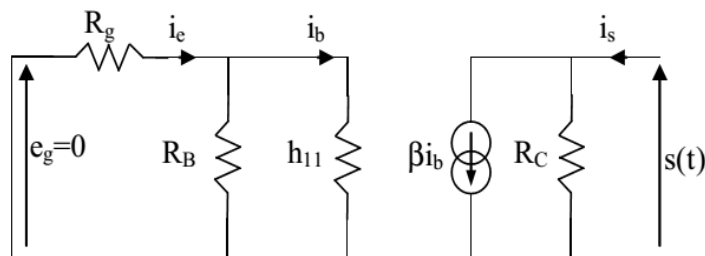


Figure IV.25. Diagram of theFigure IV.22with $e(t)=0$

Applying the mesh law on the input side for the circuit in figure 10 we find:

$$i_b = 0$$

On the output side of the same circuit, applying the law of nodes:

$$i_s = \frac{s}{R_C} + \beta i_b$$

And as we have $i_b = 0$

$$i_s = \frac{s}{R_C}$$

$$SOZ_s = R_C$$

8.4.2 Common emitter with uncoupled RE

Let's take the same circuit as that given by the Figure IV.21. with this time the decoupling capacity CE is omitted. The circuit thus obtained is shown in the Figure IV.26.

For the dynamic study and applying the superposition theorem (only $e(t)$ is applied \Rightarrow let's impose 0 at E). The circuit equivalent in dynamics of the assembly of figure 11 becomes that of figure 12.

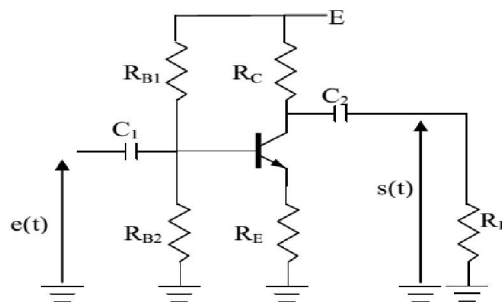


Figure IV.26. Common emitter assembly with uncoupled RE

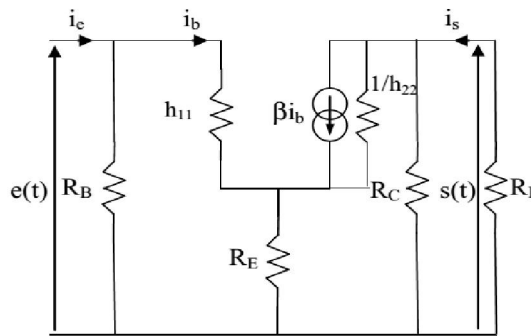


Figure IV.27. Equivalent diagram for small signals of the circuit of the Figure IV.26.

Voltage gain

We adopt the following equivalent diagram

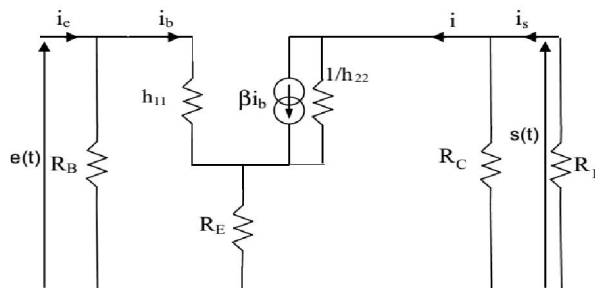


Figure IV.28. Equivalent diagram for small signals of the circuit of the Figure IV.26

The voltage gain is given by:

$$A_v = \frac{s}{e}$$

We pose

$$R_S = R_C // R_L$$

And

$$\rho = \frac{1}{h_{22}}$$

$$s = -R_S i \Rightarrow i = -\frac{s}{R_S}$$

$$e = h_{11} i_b + R_E i$$

By converting the current source into a voltage source we will have $\beta \cdot i_b$

$$s = -\rho \cdot \beta \cdot i_b + (\rho + R_E) i$$

We replace i with its value we will have

$$\begin{cases} e = h_{11} i_b + R_E \left(-\frac{s}{R_S} \right) \\ s = -\rho \cdot \beta \cdot i_b + (\rho + R_E) \left(-\frac{s}{R_S} \right) \end{cases}$$

By eliminating the two equations we will have i_b

More precisely we find:

$$A_v = -\frac{\beta(R_C // R_L)}{h_{11}(R_C // R_L + \rho + R_E) + \rho \cdot \beta \cdot R_E}$$

Yes and very big then ρ

$$A_v = -\frac{\beta(R_C // R_L)}{h_{11} + \beta \cdot R_E}$$

Current gain

The current gain is given by:

$$A_i = \frac{i_s}{i_e}$$

It is assumed that and very large then ρ

$$i_s = \frac{R_C}{R_C + R_L} \beta i_b$$

$$i_e = \frac{R_B + (h_{11} + (\beta + 1)R_E)}{R_B} i_b$$

$$A_i = \frac{\beta R_C}{R_C + R_L} \frac{R_B}{R_B + (h_{11} + (\beta + 1)R_E)}$$

Input impedance

This is the ratio between the input voltage and the input current:

$$Z_e = \frac{e}{i_e}$$

$$i_e = \frac{e}{R_B} + \frac{e}{(h_{11} + (\beta + 1)R_E)}$$

$$Z_e = R_B // (h_{11} + (\beta + 1)R_E) = \frac{R_B(h_{11} + (\beta + 1)R_E)}{R_B + (h_{11} + (\beta + 1)R_E)}$$

Output impedance

We short-circuit the input and we will have the diagram below

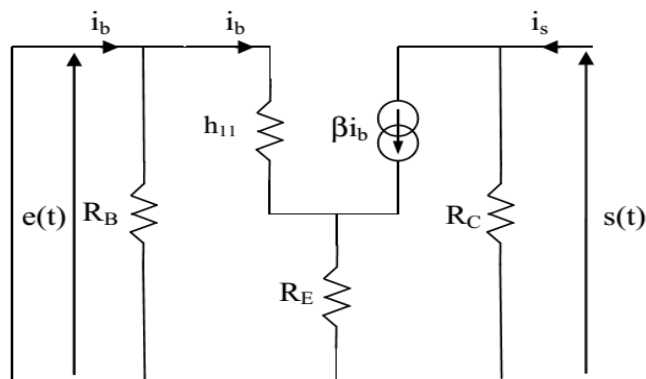


Figure IV.29. Schematic of Figure IV.26 with $e(t)=0$

It is the ratio of the output voltage when the input is short-circuited to the output current when the output is open-circuited:

$$Z_s = \left. \frac{s}{i_s} \right|_{e=0}$$

Applying the mesh law on the input side for the circuit in Figure 10 we find:

$$i_b = 0$$

On the output side of the same circuit, applying the law of nodes:

$$i_s = \frac{s}{R_C} + \beta i_b$$

And as we have $i_b = 0$

$$i_s = \frac{s}{R_C}$$

SO

$$Z_s = R_C$$

8.4.3 Common collector

As can be seen, the type of assembly can always be determined by considering the AC. We must first determine the terminals where the excitation is applied, on the input side, and where the output signal is taken. The terminal that remains then defines the common terminal of the assembly.

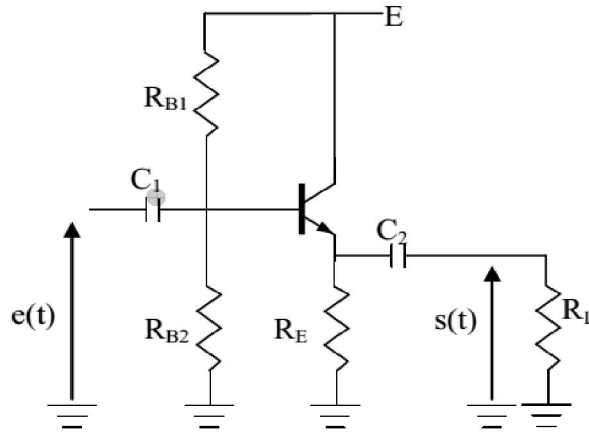


Figure IV.30. Common collector assembly

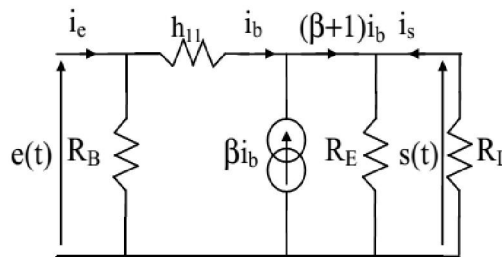


Figure IV.31. Equivalent diagram for small signals of the circuit Figure IV.30.

In the case of the assembly of Figure IV.30, the input is applied at the base B, the output is taken at the emitter E, so the assembly is a Common Collector.

Voltage gain

The voltage gain is given by:

$$A_v = \frac{s}{e}$$

$$s = (R_E // R_L)(1 + \beta)i_b$$

$$e = h_{11}i_b + (R_E // R_L)(1 + \beta)i_b$$

More precisely we find:

$$A_v = -\frac{(1 + \beta)(R_C // R_L)}{h_{11} + (R_E // R_L)(1 + \beta)}$$

Current gain

The current gain is given by:

$$A_i = \frac{i_s}{i_e}$$

By applying the current divider, at the output we draw as: i_s

$$i_s = -\frac{R_E}{R_E + R_L}(1 + \beta)i_b$$

At the entrance we have:

$$i_e = i + i_b = \frac{e}{R_B} + \frac{e}{h_{11} + (R_E // R_L)(1 + \beta)}$$

From this equation we can see that the current divides into two currents along two branches of resistances respectively and $i_e R_B h_{11} + (R_E // R_L)(1 + \beta)$

Then applying the current divider:

$$i_e = \frac{R_B + h_{11} + (R_E // R_L)(1 + \beta)}{R_B} i_b$$

$$A_i = \frac{(1 + \beta)R_E}{R_E + R_L} \frac{R_B}{R_B + h_{11} + (R_E // R_L)(1 + \beta)}$$

• Input impedance

This is the ratio between the input voltage and the input current:

$$Z_e = \frac{e}{i_e}$$

$$i_e = \frac{e}{R_B} + \frac{e}{h_{11} + (R_E // R_L)(1 + \beta)}$$

$$i_e = \frac{e}{R_B} + \frac{e}{h_{11}}$$

$$Z_e = R_B // (h_{11} + (R_E // R_L)(1 + \beta)) = \frac{R_B(h_{11} + (R_E // R_L)(1 + \beta))}{R_B + h_{11} + (R_E // R_L)(1 + \beta)}$$

• Output impedance

This is the ratio of output voltage to output current with the input shorted. This is what is translated by the equation below:

$$Z_s = \left. \frac{s}{i_s} \right|_{e=0}$$

Let us carry the condition $e(t)=0$ into the circuit and disconnect the load from the circuit because it is the latter which sees its driver circuit as being a voltage source of impedance Z_S , in the case of Thevenin's theorem or a current source of impedance Z_S , in the case of the Norton generator.

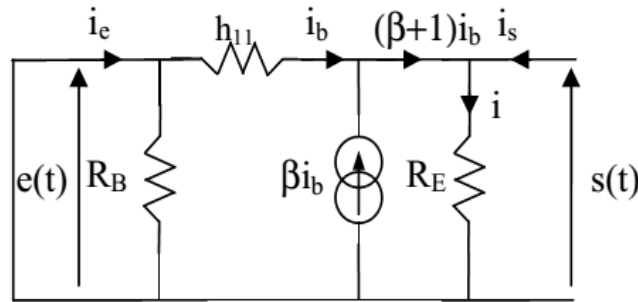


Figure IV.32. Schematic of figure 9 with $e(t)=0$

From the circuit of the Figure IV.32 the expression will be given by: On the output side of the same circuit, by applying the law of nodes: i_s

$$i_s = i - (1 + \beta)i_b$$

$$i_s = \frac{s}{R_E} + (1 + \beta) \frac{s}{h_{11}}$$

$$i_s = \frac{s}{R_E} + \frac{s}{\frac{h_{11}}{(1 + \beta)}}$$

$$Z_s = R_E // \frac{h_{11}}{(1 + \beta)}$$

Since h_{11} represents the dynamic resistance of a passing diode (small resistance) and β the static current gain (usually very large), the output impedance is in most cases approximated by: Z_s

$$Z_s = \frac{h_{11}}{(1 + \beta)}$$

8.4.4 Common base

For a Common Base (CB) circuit, the excitation is done by the emitter and the output is taken at the collector. The circuit in Figure IV.33 shows the case of a Common Base circuit.

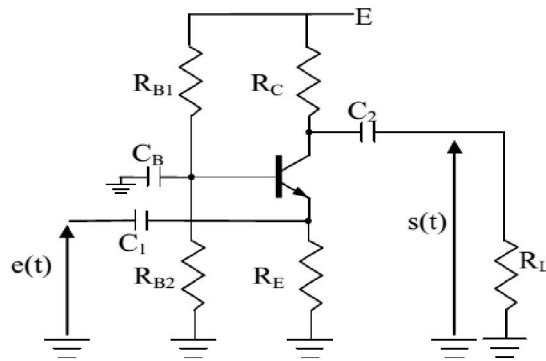


Figure IV.33. Common base assembly

In AC, with $E = 0$, the capacitors are replaced by zero impedances while the transistor is replaced by its equivalent diagram. The circuit obtained is given in Figure 18.

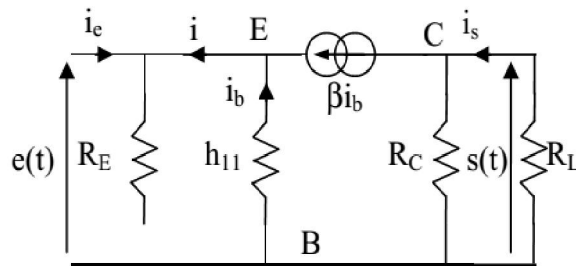


Figure IV.34. Equivalent diagram for small signals corresponding to the circuit Figure IV.33

Voltage gain

$$A_V = \frac{s}{e}$$

$$e = -h_{11}i_b$$

$$s = -(R_C // R_L)\beta i_b$$

SO

$$A_V = \beta \frac{(R_C // R_L)}{h_{11}}$$

• Current gain

The current gain is given by:

$$A_i = \frac{i_s}{i_e}$$

$$i_s = \frac{R_C}{R_C + R_L} \beta i_b$$

$$i_e = \frac{e(t)}{R_E} - i$$

We have and $i = (1 + \beta)i_b$ $i_b = -\frac{e(t)}{h_{11}}$

replacing i as a function of i_b in the expression of i_e we obtain:

$$i_e = \frac{e(t)}{R_E} + \frac{e(t)}{\frac{h_{11}}{(1 + \beta)}}$$

from this expression, we can easily see that the current is divided over two resistances and .

Therefore, by applying the principle of the current divider we will have: $i_e = \frac{R_E}{R_E + \frac{h_{11}}{(1 + \beta)}} i$

$$i_e = -\frac{R_E + \frac{h_{11}}{(1 + \beta)}}{R_E} i$$

by replacing, in this expression, i as a function of i_b Knowing that $i = (1 + \beta)i_b$

We will have:

$$i_e = -\frac{(1 + \beta)R_E + h_{11}}{R_E} i_b$$

This allows us to derive the expression for the current gain:

$$A_i = -\frac{R_E}{(1 + \beta)R_E + h_{11}} \times \frac{\beta R_C}{R_C + R_L}$$

• Input impedance

This is the ratio between the input voltage and the input current:

$$Z_e = \frac{e(t)}{i_e}$$

We have previously

$$i_e = \frac{e(t)}{R_E} + \frac{e(t)}{\frac{h_{11}}{(1 + \beta)}}$$

SO

$$Z_e = R_E // \left(\frac{h_{11}}{(1 + \beta)} \right)$$

Output impedance

It is the ratio of the output voltage when the input is short-circuited to the output current when the output is open-circuited:

$$Z_s = \frac{s(t)}{i_s} \Big|_{e(t)=0}$$

In this case the circuit will be as follows:

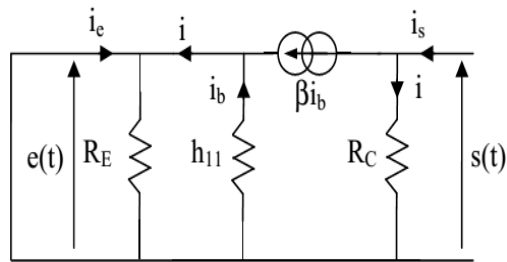


Figure IV.35. Schematic of Figure IV.34 with $e(t)=0$

$e(t) = 0$ allows us to see that $i_s = 0$

So we will have

$$Z_s = R_C$$

8.5. Comparison between the three possible assemblies

We summarize the main characteristics of the different assemblies in the table below.

Settings	Common Emitter	Common Collector	Common base
Z_e	average	big	small
Z_s	average	small	average
G_v	big	Unit (≈ 1)	big
G_i	big	big	Unit
G_p	big	AVERAGE	AVERAGE

The power gain can be calculated by:

$$G_p = \frac{P_s}{P_e} = G_v \times G_i$$

Chapter V: Operational Amplifiers

1. Introduction

Among the first integrated circuits to appear on the market since the birth of monolithic technology, operational amplifiers have been very successful. They have taken an important place thanks to their wide field of application. The operational amplifier had been originally designed, as its name indicates, to perform operations on analog quantities such as summation, multiplication, derivation, integration, etc. This is why it is considered the basic cell in analog computers.

Currently, the field of application of these circuits is constantly growing, they are now found as basic elements in circuits: multivibrators, comparators, amplifiers, active filters, signal generators, etc.

From a practical point of view, the operational amplifier can be considered as a simple active component in the same way as a transistor. The user of this component does not need to know its internal architecture to be able to use it. He just needs to carefully study the characteristics indicated on a technical sheet, given by its manufacturer, to exploit it properly.

2. Characteristics of an operational amplifier

In general, an operational amplifier is symbolized in electronic diagrams by a triangle following the representation given in figure 1 and figure 2.

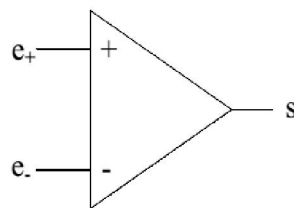


Figure.V.1. Common reference output

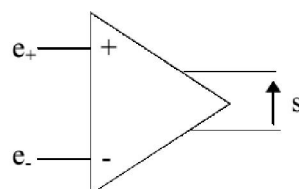


Figure V.2. Floating output

The amplifier symbolized by Figure V.1 is said to have a common reference output. In this case, the inputs and the output are taken relative to the same reference. On the other hand, the one in

Figure V.2 is said to have a floating output where the reference of the output is different from that of the inputs.

The definitions of the characteristics of an operational amplifier are given to allow it to be understood well and especially to be able to use it and to analyze the circuits around which it is built. It is of great importance to differentiate between the characteristics of the operational amplifier as a component and those corresponding to the circuit in which it is located.

3. A0 voltage amplification

The voltage amplification A_0 , is expressed by the relation which gives the output voltage as a function of the input voltage. It can be given from the relation:

$$s = A_0(e_+ - e_-) \quad (V.1)$$

With output signals

From this expression we can see that in the case where only is applied the output will be in phase with, on the other hand if only is applied the output is in phase opposition with This is why the inputs of an operational amplifier are differentiated from each other by a + sign and a - sign. - *and* +

e_+ Non-inverting input.

e_- Inverting input.

Due to the lack of ideal symmetry of the input stages of an operational amplifier, the two inputs will be amplified with different gains. Therefore, for this case equation (V.2), gives the relationship between the output s of the amplifier and its two inputs ($e_+, -e_-$).

$$s = A_1e_+ + A_2e_- \quad (V.2)$$

With A_1 negative and A_2 positive.

In the ideal case, equation (V.1) can be deduced from equation (V.2) by simply replacing A_1 and A_2 by A_0 . Knowing that the input stage of an operational amplifier is constituted by a differential amplifier, it would then be interesting to highlight the term ($e_+, -e_-$) in the relation given by equation (V.2).

Either:

$$\text{Differential input} \quad e_d = e_+ - e_- \quad (V.3)$$

$$\text{Common mode input} \quad e_c = \frac{e_+ + e_-}{2} \quad (V.4)$$

From equation (4)

$$\Rightarrow 2e_c = e_+ + e_- \quad (V.5)$$

(V.3) + (V.5) \Rightarrow

$$e_+ = \frac{e_d + 2e_c}{2} = \frac{e_d}{2} + e_c$$

(V.5) - (V.3) \Rightarrow

$$e_- = \frac{2e_c - e_d}{2} = e_c - \frac{e_d}{2}$$

Let us replace e_+ and e_- by their expressions in equation (2)

$$s = A_1 \left(\frac{e_d}{2} + e_c \right) + A_2 \left(e_c - \frac{e_d}{2} \right) = \frac{A_1 - A_2}{2} e_d + (A_1 + A_2) e_c \quad (\text{V.6})$$

Finally we can deduce that in the real case the output of an operational amplifier is expressed as a function of the inputs as follows:

$$s = A_d e_d + A_c e_c \quad (\text{V.7})$$

With

$$A_d = \frac{A_1 - A_2}{2} \quad \text{Differential amplification.}$$

$$A_c = (A_1 + A_2) \quad \text{Common mode amplification.}$$

We can thus see that:

$$\text{If } e_+ = e_-$$

The output is far from zero, it all depends on the value of A_c . In practice, the amplification is not given. Only A_d expressing the open-loop amplification (A_0) of the operational amplifier is given. This open-loop amplification, A_0 , is generally considered, in circuit analyses, to be infinite.

4. Differential input impedance Z_{ed}

The differential impedance Z_{ed} of an operational amplifier is defined as the impedance seen by a driver generator connected between the two inputs e_+ and e_- as shown in Figure V.3. It is this input impedance given by the manufacturer and whose value can be considered infinite in certain cases. The differential input impedance constitutes an important characteristic of the quality of the operational amplifier

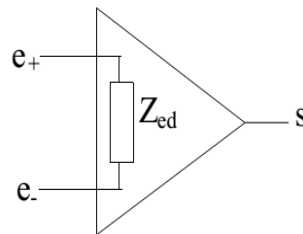


Figure.V.2. Differential impedance

5. Common mode input impedance Z_{ec}

The common mode input impedance represents the impedance seen by a drive generator connected to one of the two inputs (e_+, e_-) with the other input connected to the output. Z_{ec} .

In this case we will have two impedances and respectively the common mode input impedance for the inverting input and the common mode input impedance for the non-inverting input. Figure V.3 shows the circuits that allow the measurement or calculation of the common mode input impedance.

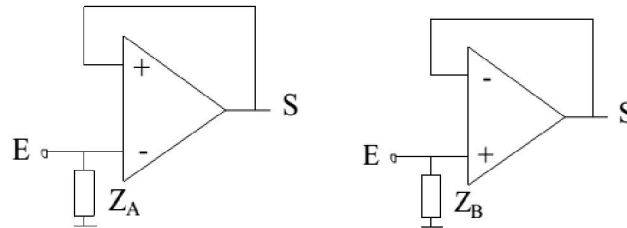


Figure.V.3. Common mode input impedance

In addition to its real parameters, in reality the Operational Amplifier has defects: offset currents and offset voltage at the input, TRMC (Common Mode Rejection Ratio), output impedance, gain frequency variation.

6. Output impedance Z_{S0}

The output impedance Z_{S0} corresponds to the impedance seen by a load connected to the output of the operational amplifier, as illustrated in Figure V.5. It can also be defined as the internal impedance of the Thevenin generator, equivalent to the operational amplifier circuit, seen by the load connected to its output. In practice Z_{S0} and for a first approximation the value of can be considered as zero.

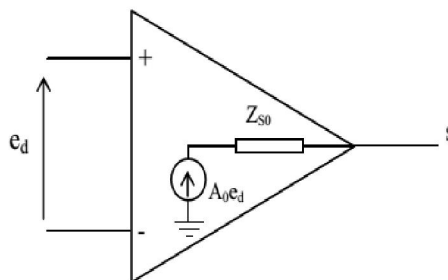


Figure.V.4. Output impedance

In summary, the real operational amplifier can be represented by its equivalent circuit given in Figure.V.5.

In the study of operational amplifier based circuits, an ideal operational amplifier is assumed with infinite DC gain, infinite input impedance and zero output impedance as characteristics. In reality, this assumption hides many defects including the input offset voltage, an input offset current, the influence of the common mode input, the gain dependence on the frequency variation, the rise time which also depends on the component supply voltage.

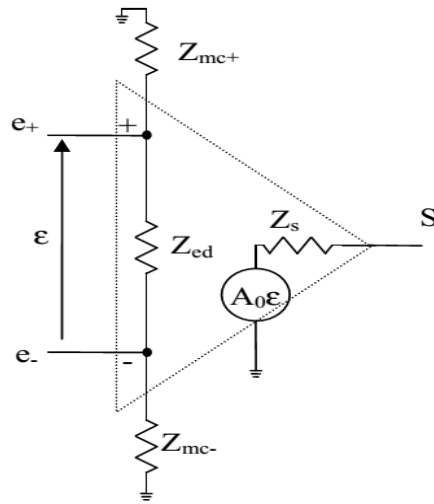


Figure.V.5. Model of a real operational amplifier

7. Common mode rejection ratio TRMC

The common mode rejection ratio expresses the order of magnitude of the common mode amplification relative to the differential mode amplification.

Equation (V.6) given by:

$$s = A_d e_d + A_c e_c$$

We shoot

$$s = A_d e_d \left(1 + \frac{A_c e_c}{A_d e_d} \right)$$

We pose

$$r = \frac{A_c}{A_d}$$

r : Common Mode Rejection Ratio (CMRR).

Then the output voltage s will be:

$$s = A_d e_d \left(1 + \frac{e_c}{r e_d} \right) \quad (\text{V.8})$$

In the ideal case the common mode rejection ratio r is taken as infinite. Equation (V. 8) becomes the same as that given by equation (1):

$$s = A_d e_d \quad (\text{V.9})$$

In the practical case the approximation can be made according to the order of magnitude of r with respect to such that: e_c/e_d

$$1 \gg \frac{e_c}{re_d} \Rightarrow r \gg \frac{e_c}{e_d} \Rightarrow s = A_d e_d$$

8. Input offset voltage (Or offset) VD

The input offset voltage is defined as the DC voltage that must be applied to the input of an operational amplifier so that the voltage at its output is zero. Some operational amplifiers have two terminals that are used to inject a DC offset adjustment voltage.

9. Input offset current ID

It corresponds to the direct current that must be injected at the input of the operational amplifier to have a zero voltage at its output. It is also defined as the association of two polarization currents.

10. IP bias current

The bias current is defined as the current that must be injected into one of the two inputs with the other input to ground, to have a zero output voltage. Thus we can notice that there are two bias currents:

I_{P+} Current on the non-inverting input with the inverting input at ground.

I_{P-} Current on the inverting input with the non-inverting input at ground.

The offset current can be expressed as a function of the bias currents by the relation:

$$I_D = I_{P+} - I_{P-} \quad (V.10)$$

The two inputs given on the schematic of an operational amplifier actually define the inputs of a differential amplifier which constitutes its input stage. This is why we found it useful to give a general overview of the differential amplifier.

3. Differential amplifier

The schematic diagram of a differential amplifier is given in Figure V.6 where the two transistors and the other elements associated with them must be as identical as possible.



Figure.V.6. Schematic diagram of a differential amplifier

3.1. Static study

The circuit is linear, so we can separate the static study from the dynamic study based on the superposition theorem.

Static study \Rightarrow E and applied $-E$ are alone ($e_1 = e_2 = 0$)

$$I_0 = I_{E1} + I_{E2} \quad (V.11)$$

With the approximation

$$I_{C1} = I_{E1} \text{ et } I_{C2} = I_{E2} \quad (V.12)$$

$$I_0 = I_{C1} + I_{C2} \quad (V.13)$$

$$I_0 = \frac{V_N - (-E)}{R_0} \Rightarrow$$

$$I_0 = \frac{V_N + E}{R_0} \quad (V.14)$$

We have

$$V_N = -V_{BE1} = -V_{BE2} = -0.6V$$

In the general case

$$E \gg V_{BE} \Rightarrow I_0 = \frac{E}{R_0}$$

Very good symmetry is always sought in the design of differential amplifiers. For the circuit studied we must have:

$$R_{C1} = R_{C2} = R_C$$

The two transistors T1 and T2 are identical, in this case we can write

$$I_{C1} = I_{C2} = \frac{I_0}{2} = \frac{E}{2R_0} \quad (V.15)$$

And

$$V_{CE1} = V_{CE2} = E - R_C I_C \quad (V.16)$$

$$V_{CE1} = V_{CE2} = E - \frac{R_C}{2R_0} E = E \left(1 - \frac{R_C}{2R_0}\right) \quad (V.17)$$

From the result obtained at (V.17) we see that the operating point can be determined by the choice of the ratio of the two resistances and R_C and R_0

3.1.1 Basic circuits of the operational amplifier

The main function of an operational amplifier is amplification. However, the gain of this component is considered to be very large in real mode and infinite in ideal mode hence its characteristic shown in Figure V.7.

Case of a counter reaction

It is known that negative feedback allows to stabilize a circuit by decreasing its gain and widening its bandwidth. Studying the circuit of the Figure.V.8.

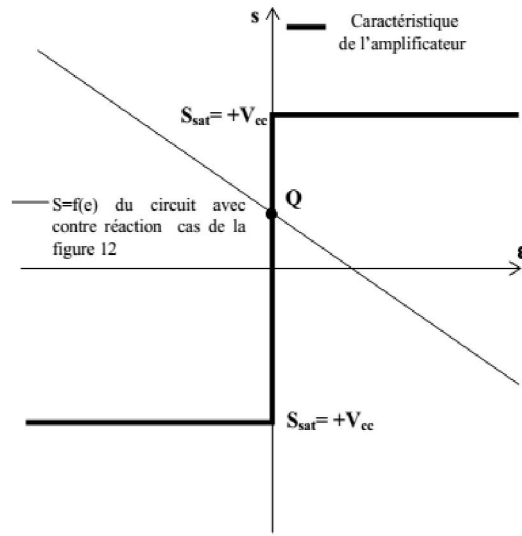


Figure.V.7. Output characteristic of an operational amplifier.

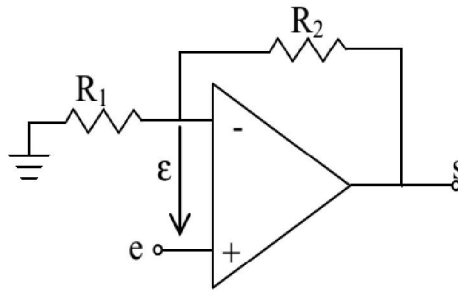


Figure.V.8. Operational amplifier assembly with a feedback resistor on the inverting input.

In the circuit in the figure, the operational amplifier is considered ideal. This is what allows us to derive the expressions (V.18 - V.20) from the assumption (inverting and non-inverting input current). $i_+ = 0$ and $i_- = 0$

$$v_- = \frac{R_1}{R_1 + R_2} s \quad (V.18)$$

$$\varepsilon = e - v_- = e - \frac{R_1}{R_1 + R_2} s \quad (V.19)$$

$$s = \frac{R_1 + R_2}{R_1} e - \frac{R_1 + R_2}{R_1} \varepsilon \quad (V.20)$$

We can clearly see the expression (V.19) that the feedback chain has led to a relationship between ε and s ; which is nothing other than a straight line whose plot intersects the characteristic of the amplifier at a single point Q as shown by the Figure.V.7. Point Q is unique

and corresponds to the linear regime; its abscissa corresponds to $\varepsilon = 0$ from which the relation of s as a function of e will be:

$$s = \frac{R_1 + R_2}{R_1} e \quad (\text{V.21})$$

Let us make a simple study on the stability of this circuit. Let us take equation 28 expressing ε as a function of e and s . We see that if s increases slightly, it will cause a decrease in ε which brings s back to its previous value. The circuit is stable.

Case of a reaction

Let us do the same study as in the case of the previously studied counter reaction, but this time for the case of a reaction between s and the non-inverting input as shown by the Figure.V.9.

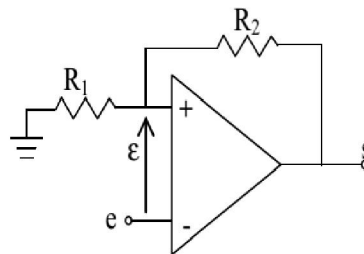


Figure.V.9. Operational amplifier assembly with a feedback resistor on the non-inverting inverter.

$$V_+ = \frac{R_1}{R_1 + R_2} s \quad (\text{V.22})$$

$$\varepsilon = V_+ - e = \frac{R_1}{R_1 + R_2} s - e \quad (\text{V.23})$$

$$s = \frac{R_1 + R_2}{R_1} e + \frac{R_1 + R_2}{R_1} \varepsilon \quad (\text{V.24})$$

If we plot the operational amplifier characteristic and s as a function of ε we will obtain the Figure.V.10.

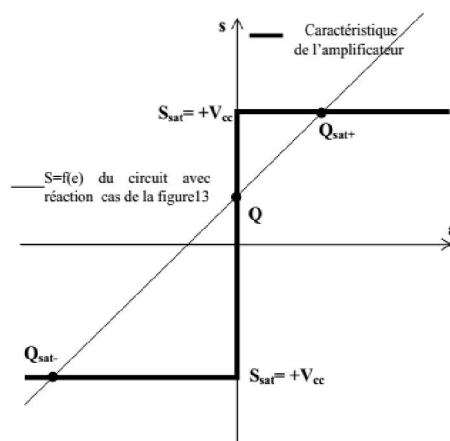


Figure.V.10. Output characteristic of an operational amplifier.

A similar reasoning to the previous one shows that if we fix the operating point in Q (linear regime) then a slight increase in s leads to an increase in ε which further favors the increase of s towards saturation. As a result, we arrive at the conclusion of non-stability of Q for this assembly case.

4. Inverting amplifier

The inverting amplifier is the most used assembly, Figure.V.11. It is simple in its assembly and it constitutes the basic circuit for other assemblies based on operational amplifier. This amplifier has the disadvantage of its input impedance which is not large and which depends on the passive components added to the circuit.

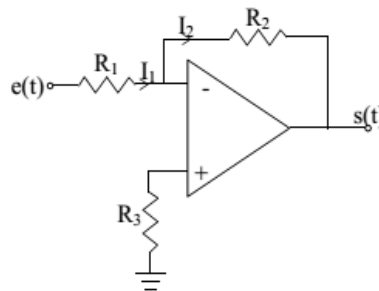


Figure.V.11. Inverting amplifier

The calculation of the input impedance, seen by the attack generator whose emf corresponds to $e(t)$, is given by the expression.

$$Z_e = \frac{e(t)}{I_1} = R_1 \quad (V.25)$$

The voltage amplification is expressed by

$$A = \frac{e(t)}{s(t)} \quad (V.26)$$

$$I_1 = I_2 \Rightarrow \frac{e(t)}{R_1} = -\frac{s(t)}{R_2} \Rightarrow \frac{s(t)}{e(t)} = -\frac{R_2}{R_1}$$

$$A = -\frac{R_2}{R_1} \quad (V.27)$$

The (-) sign indicates that the input signal and the output signal are in phase opposition. We can see that there is amplification and inversion of the input signal.

Noticed

The resistor R3 is used to minimize the effect of the polarization current and especially for temperature stability. Its value can be calculated as follows:

Let the circuit of the Figure.V.12. where $e(t) = 0$. At the two inputs of the operational amplifier we find two currents and which are respectively the bias current of the non-inverting input and the bias current of the inverting input such that:

$$I_p = I_{p+} - I_{p-} \quad (V.28)$$

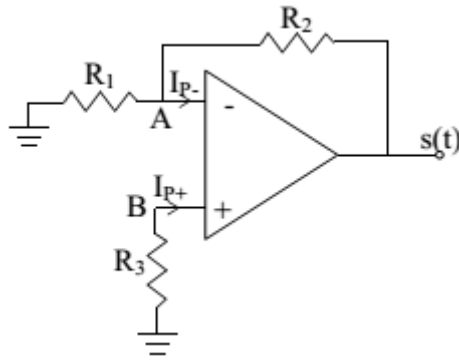


Figure.V.12. Scheme for calculating the effect of R3

At node A we have:

$$\frac{0-V_A}{R_1} e + \frac{V_0-V_A}{R_2} = I_{P-} \quad (V.29)$$

$$\Rightarrow V_A = \left(\frac{V_0}{R_2} - I_{P-}\right) \frac{R_1 R_2}{R_2 + R_1} \quad (V.30)$$

And

$$V_B = -R_3 I_{P+} \quad (V.31)$$

And as we have

$$V_0 = A(V_B - V_A) \quad (V.32)$$

With the assumption that A is very large we will have

$$V_A = V_B \Rightarrow -R_3 I_{P+} = \left(\frac{V_0}{R_2} - I_{P-}\right) \frac{R_1 R_2}{R_2 + R_1} \quad (V.33)$$

We will have

$$V_0 = -R_2 I_{P-} - \frac{R_3}{R_1} (R_2 + R_1) - I_{P+} \quad (V.34)$$

Knowing that the input stage of an operational amplifier is a differential amplifier whose branches which constitute it are as symmetrical as possible, then $I_{P+} \cong I_{P-}$ 'owhereso that the V_0 giveseand by l'eequation is as small as possible it is necessary that:

$$R_3 = \frac{R_1 R_2}{R_2 + R_1} \quad (V.35)$$

And so

$$V_0 = -R_2 (I_{P-} - I_{P+}) \quad (V.36)$$

5. Non-inverting amplifier

The non-inverting amplifier is used in the case where the output signal must be in phase with the input signal. This circuit can be realized by the cascade association of two inverting amplifiers in the case where a very high input impedance is not sought. In the case where a high input impedance is required, we use the circuit of theFigure.V.13.

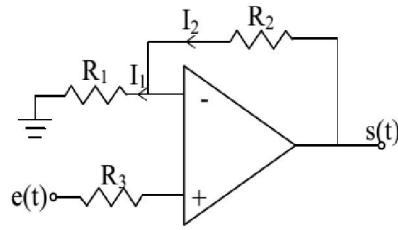


Figure.V.13. Non-inverting amplifier

Input impedance of the assembly

According to the diagram of the Figure.V.13. The drive generator sees the input impedance of the operational amplifier itself in series with R. The input impedance is then very large.

Amplification of assembly A

Since the amplification and input impedance of the operational amplifier are very large we have:

$$e(t) = e_- = e_+ \tag{V.37}$$

$I_1 = I_2 \Rightarrow R_1$ And R_2 are in series

\Rightarrow by applying the voltage divider divider
$$e_+ = \frac{R_1}{R_1+R_2} s(t)$$

And as

$$e(t) = e_+ \Rightarrow A = \frac{s(t)}{e(t)} = 1 + \frac{R_2}{R_1} \tag{V.38}$$

The amplification is positive so $s(t)$ is in phase with $e(t)$, and it is at least equal to unity.

6. Differential amplifier

The circuit given on the Figure.V.14. illustrates the schematic of a differential amplifier. Each input line has its own drive generator. The latter sees a load impedance which depends on the passive components associated with the circuit.

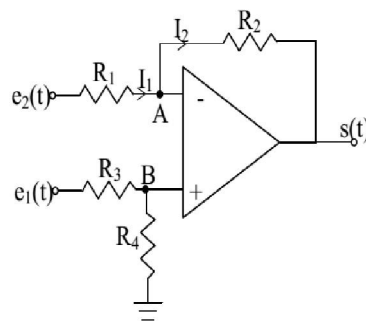


Figure.V.14. Differential amplifier

The open loop gain of the operational amplifier is:

$$V_A = V_B$$

$$V_B = \frac{R_4}{R_4+R_3} e_1(t) \quad (V.39)$$

$$I_1 = I_2 \Rightarrow \frac{e_1(t)-V_A}{R_1} = -\frac{s(t)-V_A}{R_2} \quad (V.40)$$

$$\frac{e_2(t)}{R_1} - V_A \left(\frac{R_1+R_2}{R_1 R_2} \right) = -\frac{s(t)}{R_2} \quad (V.41)$$

Replacing the expression of with the expression of V_A and V_B

$$\frac{e_2(t)}{R_1} - \frac{R_4}{R_4+R_3} \left(\frac{R_1+R_2}{R_1 R_2} \right) e_1(t) = -\frac{s(t)}{R_2} \quad (V.42)$$

$$s(t) = -\frac{R_1}{R_2} e_2(t) - \frac{R_4}{R_4+R_3} \frac{R_1+R_2}{R_1 R_2} e_1(t) \quad (V.43)$$

With and we get $R_4 = R_2, R_3 = R_1$

$$s(t) = \frac{R_1}{R_2} (e_1(t) - e_2(t)) \quad (V.44)$$

7. Logarithmic amplifier

On the Figure.V.15. transistor T, mounted in the feedback, is used as a diode. The collector of this transistor is short-circuited with the base. It can therefore be replaced by a simple diode.

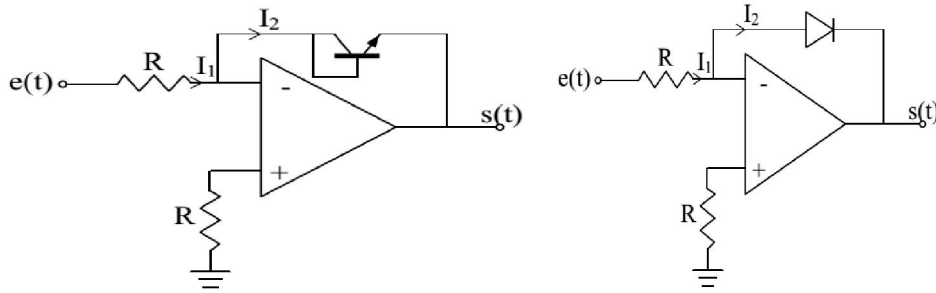


Figure.V.15. Logarithmic amplifier

The current I_2 is the forward current in the diode and $-s(t)$ the voltage between its anode and cathode. We can then express this current as a function of $-s(t)$

$$I_2 = I_0 e^{-\frac{q}{KT} s(t)} \quad (V.45)$$

$$I_2 = I_1 \quad (V.46)$$

$$I_1 = \frac{e(t)}{R} \Rightarrow \frac{e(t)}{R I_0} = e^{\frac{q(-s(t))}{KT}} \quad (V.47)$$

$$\text{Log} \frac{e(t)}{R I_0} = -\frac{q}{KT} s(t) \quad (V.48)$$

$$s(t) = -\frac{q}{KT} \text{Log} e(t) + \frac{q}{KT} \text{Log} R I_0 \quad (V.49)$$

$$s(t) = -\frac{q}{KT} \text{Log} e(t) + \text{cte} \quad (V.50)$$

8. Exponential amplifier

Like logarithmic amplifier, exponential amplifier and nonlinear amplifier, Figure.V.16. They are used especially when the amplification must depend on the order of magnitude of the signal to be amplified. They also constitute a basic element in circuits for multiplying analog quantities.

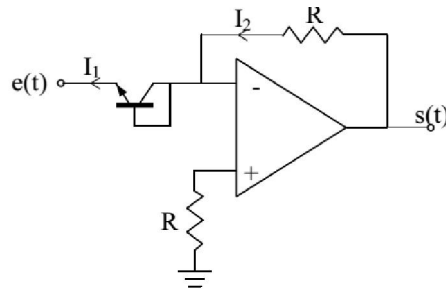


Figure.V.16. Exponential amplifier

$$I_2 = I_0 e^{-\frac{q}{kT}e(t)} \quad (V.51)$$

$$I_2 = I_1 \quad (V.52)$$

$$I_1 = \frac{S(t)}{R} \quad (V.53)$$

$$s(t) = RI_0 e^{-\frac{q}{kT}e(t)} \quad (V.54)$$

9. Integrator

The operational amplifier-based integrator circuit, Figure V.17, not only allows the integration of an analog signal but also with controlled attenuation or amplification. Something that cannot be achieved by a simple RC-type integrator.

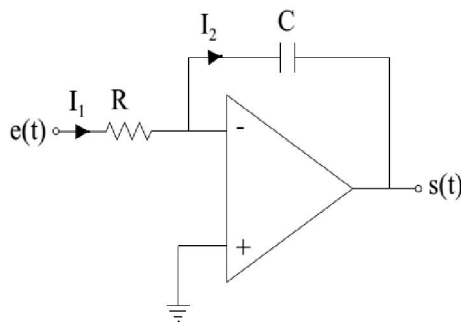


Figure.V.17. Inverting integrator

$$I_1 = \frac{e(t)}{R} \quad (V.55)$$

$$I_2 = -C \frac{ds(t)}{dt} \quad (V.56)$$

$$I_1 = I_2 \Rightarrow \frac{e(t)}{R} = -C \frac{ds(t)}{dt} \quad (V.57)$$

$$\frac{ds(t)}{dt} = -\frac{e(t)}{CR} \quad (\text{V.58})$$

$$s(t) = -\frac{1}{CR} \int e(t) dt \quad (\text{V.59})$$

10. Derivative

The derivator is a circuit that allows to obtain the derivative of an analog signal applied to the input. These two circuits, integrator and derivator, generally constitute the basic elements of analog computers. The Figure.V.18. presents the electrical diagram of an inverting derivator.

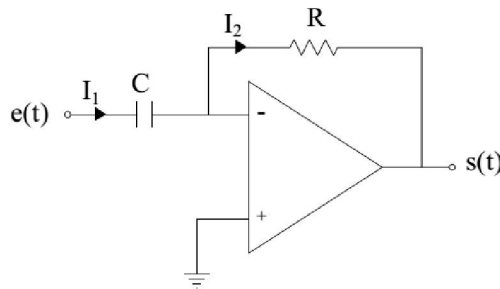


Figure.V.18. Inverter derivator

$$I_1 = C \frac{de(t)}{dt} \quad (\text{V.60})$$

$$I_2 = -\frac{s(t)}{R} \quad (\text{V.61})$$

$$I_1 = I_2 \Rightarrow -\frac{s(t)}{R} = C \frac{de(t)}{dt} \quad (\text{V.62})$$

$$\frac{ds(t)}{dt} = -\frac{e(t)}{CR} \quad (\text{V.63})$$

$$s(t) = RC \frac{de(t)}{dt} \quad (\text{V.64})$$

11. Adder

An operational amplifier whose characteristics approach those of ideal values such as:

$R_i = \infty$ Input resistance.

$A_0 = \infty$ Open loop gain.

$R_s = 0$ Output resistance.

It can be used as a precise adder of analog signals applied to its input. Figure.V.19. represents the assembly used for the realization of an adder. The choice of resistors depends on the coefficients with which it is necessary to multiply the terms to be added.

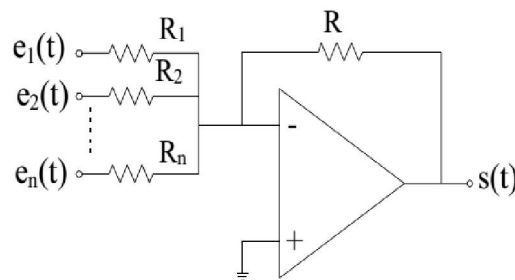


Figure.V.19. Inverting adder

$$I_1 + I_2 + \dots + I_n = I \quad (V.65)$$

$$\left. \begin{array}{l} I_1 = \frac{e_1(t)}{R_1} \\ I_2 = \frac{e_2(t)}{R_2} \\ \vdots \\ I_n = \frac{e_n(t)}{R_n} \end{array} \right\} \Rightarrow \frac{e_1(t)}{R_1} + \frac{e_2(t)}{R_2} + \dots + \frac{e_n(t)}{R_n} = -\frac{s(t)}{R} \quad (V.66)$$

From where

$$s(t) = -\left(\frac{R}{R_1} e_1(t) + \frac{R}{R_2} e_2(t) + \dots + \frac{R}{R_n} e_n(t)\right) \quad (V.67)$$

If

$$R = R_1 = R_2 = \dots = R_n \quad (V.68)$$

SO

$$s(t) = -(e_1(t) + e_2(t) + \dots + e_n(t)) \quad (V.69)$$

12. Comparator

The use of an operational amplifier as a comparator is widely used, especially in control chains. In the catalogs of linear circuits we find operational amplifiers divided into categories according to their main functions such as amplifiers, comparators. etc.

The schematic diagram of a comparator is illustrated in Figure V.20. In this diagram the amplifier exploits its maximum gain A_0 (open loop gain).

The output $s(t)$ is always given by:

$$s(t) = A_0(e(t) - V_{ref}) \quad (V.70)$$

So we can see two cases:

$$e(t) - V_{ref} > 0 \text{ given } s(t) = +V_{cc}$$

$$e(t) - V_{ref} < 0 \text{ given } s(t) = -V_{cc}$$

Where $+V_{cc}$ and $-V_{cc}$ represent the comparator bias voltages.

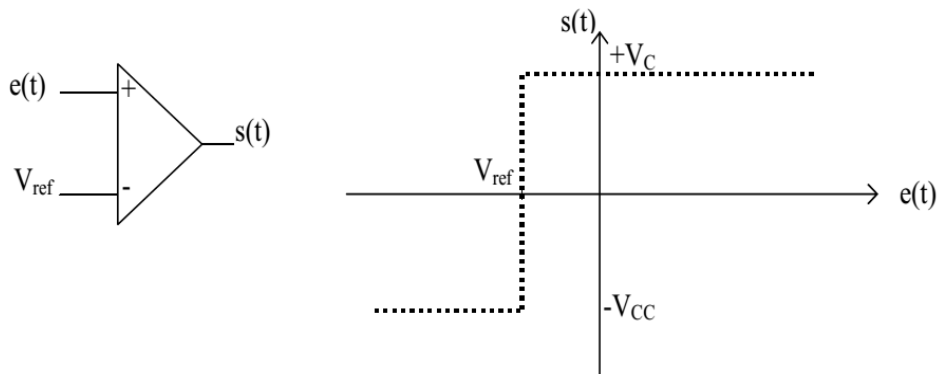


Figure.V.20. Comparator without hysteresis

13. Comparator with hysteresis

In this type of comparators, the reference is also swapped between two values. This reference depends on the direction of variation of the signal to be compared. As can be seen in Figure V.21, it is linked to the output signal by the relation:

$$V_{\text{ref}} = \frac{R_1}{R_1 + R_2} s(t) \quad (\text{V.71})$$

This circuit is also called Schmitt Trigger.

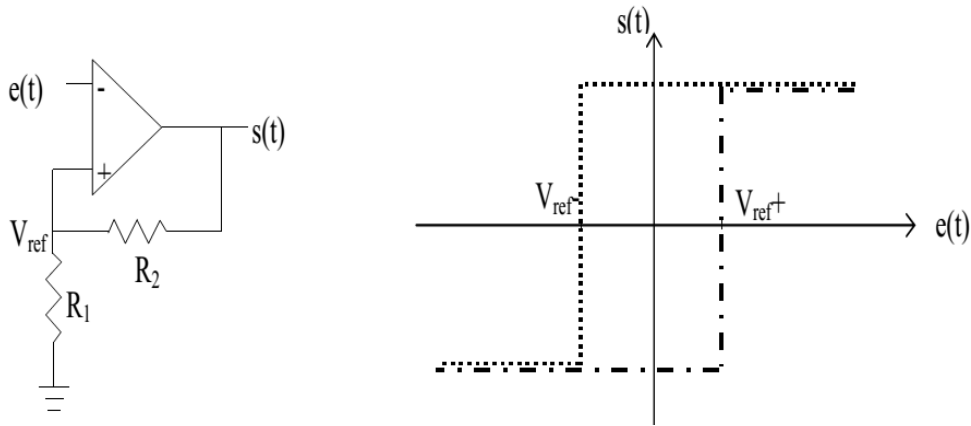


Figure.V.21. Comparator with hysteresis

On the timing diagram in Figure V.21, representing the response of the comparator, the values taken by the reference are expressed by:

$$V_{\text{ref}+} = \frac{R_1}{R_1 + R_2} (+V_{\text{CC}}) \quad (\text{V.72})$$

And

$$V_{\text{ref}-} = \frac{R_1}{R_1 + R_2} (-V_{\text{CC}}) \quad (\text{V.73})$$