REPUBLIQUE ALGERIENNE DEMOCRATIQUE ET POPULAIRE
MINISTERE DE L'ENSEIGNEMENT SUPERIEUR ET DE LA RECHERCHESCIENTIFIQUE
UNIVERSITE MOHAMED BOUDIAF - M'SILA

FACULTE DE SCIENCES ET TECHNOLOGIES
DEPARTEMENT DE GENIE ELECTRIQUE
N° : ER-06

DOMAINE :SCIENCES ET TECHNOLOGIE
FILIERE : Electrotechnique
OPTION : Commande Electrique

Mémoire présenté pour l'obtention
Du diplôme de Master Académique
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Intitulé

SIL and PIL Simulation of Second Order SMC of HVDC Systems

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Année universitaire : 2019/ 2020

'I remember Tom [Edison] telling them that direct current was like a river flowing peacefully to the sea, while alternating current was like a torrent rushing violently over a precipice. Imagine that! Why they even had a professor named Harold Brown who went around talking to audiences... and electrocuting dogs and old horses right on stage, to show how dangerous alternating current was.'

George Westinghouse

Acknowledgements

First and foremost, all praise is to ALLAH Who gave us the guidance and the power to carry on this study.

We would, first of all, like to thank and offer our greatest gratitude and appreciation to our supervisors Mr.Reguig Berra Ahmed and Mr. Barkat Said who have been extremely helpful with their priceless support and guidance throughout this work. and for providing us with valuable comments and suggestions during the development of this work. Moreover, we would like to acknowledge our honest appreciation to our supervisors for investing a lot of time and work on us and providing us with consistent consultations for which we were able to earn enough insight into the thesis subject. we also would like to offer our sincere thanks to Mr. Youcefa Khalil for his priceless help. And extend that thanks and recognition to Mr. Bedboudi Mohamed.

Our thanks go to the members of the board of examiners for accepting to read, evaluate, and comment on this thesis.

Also, we would like to acknowledge our sincere appreciation and deepest gratitude for everyone who helped, supported, and encouraged us in words, in actions, or even in a simple smile that pushed us forward to finish this work.

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Nomenclature

C	DC capacitance
f_k	Frequency
f_s	Switching Frequency
t	Time
k_{pi}	Proportional gain
k_{ii}	Integrator gain
$i_{ak},\ i_{bk},\ i_{ck}$	Three-phase currents
$i_{dk},\ i_{qk}$	*dq*-axes currents
i_{dck}	DC current
i_{abck}	Phase currents
i_{dkref}	*d*-axis reference current
i_{qkref}	*q*-axis reference current
i_{line}	DC line current
L_k	Line inductance
R_k	Line resistance
P	Active power
Q	Reactive power
P_{sref}	Reference active power
Q_{sref}	Reference reactive power
V_{mk}	Amplitude of the phase voltage
$v_{sak}, v_{sbk}, v_{sck}$	Three- phase voltages at the PCC
v_{tabck}	Instantaneous phase voltages at the VSC's terminal
$v_{sdk}; v_{sqk}$	*dq*-axes voltages
$v_{sqref}; v_{sdref}$	Reference *dq*-axes voltage
v_{dck}	DC-bus voltage
v_{DCref}	DC-bus reference voltage
θ_{PLL}	PLL output angle
P_{line}	DC line active power
P_{dck}	VSC DC side active power
P_{sk}	Grid side active power
P_{tk}	VSC terminal active power
r	Relative degree
u	Control Vector
T_h	Sampling period
ξ	Damping factor

ω_k	Angular frequency
ω_n	Natural frequency
HVDC	High Voltage Direct Current
HVAC	High Voltage Alternative Current
CCHT	Courant Continu Haute Tension
VSC	Voltage Source Converter
LCC	Line Commutated Circuit
CSC	Current Source Control
PLL	Phase Locked Loop
SVPWM	Space Vector Pulse Width Modulation
IGBT	Insulated Gate Bipolar Transistor
SMC	Sliding Mode Control
PCC	Point of Common Coupling
STA	Super Twisting Algorithm
ISMC	Integral Sliding Mode Control
ESO	Extended State Observer
PI	Proportional-Integral Control
SIL	Software In the Loop
PIL	Processor In the Loop

General Introduction

The global need for reliable energy and electricity is growing fast. The International Energy Agency (IEA) predicts that, by 2030, global electricity consumption will be near to 30,000 TWh a year [1]. Thermal power plants combusting fossil fuels are still the main source of power production worldwide. On the other hand, there are important international efforts to control emissions and prevent a global climate crisis because planet earth is fronting some dangerous climatological issues linked to the continuously expanding level of greenhouse-gas emissions.

On the other hand, various remote areas throughout the world need adequate access to electricity. However, utilities cannot provide the huge demand for power by building extra power stations due to the before mentioned environmental causes. Those facts may support the urge for a transfer from fossil-fuel-based power generation to a future with higher levels of renewable energy sources (RES) in combination with other energy sources with less emission. The persistent rise in the need for electric power requires more reliable power networks. So, as more renewable and alternate production is integrated into the power system, exceptionally stable and efficient transmission system of electrical power from these new sources to the main power grid is indispensible[2].This passes necessarily by increasing the effectiveness of transmission lines by controlling the power flow. One attractive technology that enables the control of power flow in the system is High Voltage Direct Current (HVDC) transmission.

HVDC systems are essentially employed as a reliable solution for transferring power across lengthy distances, asynchronous interconnection of power grids that work on distinctive frequencies; and power flow control[1].Various technologies have been early adopted to design HVDC systems including line-commutated converter (LCC) based HVDC systems, capacitor-commutated converter (CCC) based HVDC (CCC-HVDC) systems, or controlled series commutated converter (CSCC) based HVDC systems [3].These conventional thyristors based HVDC systems are not fully controllable and have some limitations and unwanted characteristics such as being physically bulky, they are characterized by unidirectional direct current flow, and the direction of active power flow is determined by DC voltage [4].Also, another downfall that they can reverse the active and reactive power flow by reversing the DC current and without reversing the DC voltage polarity. Furthermore, conventional HVDC converters consume reactive power; therefore, they require a strong AC network for commutations. Due to the inherent limitations of conventional HVDC systems voltage source converter based HVDC (VSC-HVDC) systems, employing insulated gate bipolar transistor (IGBT) technology, has brought growing attention. The main feature of the VSC-HVDC system is that no external voltage source is needed for communication, while active and reactive powers at each AC grid can be independently controlled [5, 6]. Also, VSC-HVDC transmission technology is ideal for linking remote offshore wind-power plants to mainland networks as it overcomes the limitations of long-distance HVAC transmission while ensuring robust performance and minimal electrical losses [7].

Conventionally, control of the VSC-HVDC system employs vector oriented control (VOC) strategy based on linear proportional-integral (PI) schemes [8],whose control performance may be degraded with the variance of functioning conditions as its control parameters are tuned from one-point linearization model [9]. As VSC-HVDC systems are highly nonlinear resulting from converters and also operate in power systems with modeling uncertainties, many advanced control strategies are developed to give a consistent control performance under different operation circumstances. Indeed, a linear matrix inequality (LMI)-based robust control was developed in [10].Nonlinear control schemes were proposed in[11][12][13][14]. Nonlinear backstepping control techniques were designed in [15][11].In [5, 6], power-synchronization control was employed to greatly increase the short-circuit capacity to the AC system. Sliding Mode Control (SMC) strategy adopted in [14][11][] is the most attractive solution due to its simplicity and robustness.

Sliding-mode control (SMC) is a powerful and high-frequency switching control for nonlinear systems with modeling uncertainties and time-varying perturbations. It emphasizes the easy implementation, disturbance rejection, quick response, and reliable robustness. In order to reduce the influence of the chattering phenomenon several approaches by using integral law, fuzzy logic controller, and high order sliding mode (HOSM) approach have been proposed [16][14][17]. Using HOSM approach the main advantages of the standard SMC are kept, the chattering effect is reduced, and higher-order precision is provided. As a special case of HOSM methods, the second-order sliding mode algorithms are characterized by a finite time convergence[17].

In modern decades, digital processor technology has developed quickly and has had an influence on many fields. More specifically, the digital signal processor (DSP) is one of the most developed processors; it was involved in the implementation of voluminous numerical control algorithms, complex and fast relating to the field of power electronics. On the other hand, thecontrol dynamics often cannot be sufficiently captured by the methodology of traditional simulation based only on software. For this reason, building a test prototype is more than necessary to validate the performance of a given system. However, this approach involves long design processes term, cost increases, and sometimes the risk of damage to researchers. An effective way to bridge the gap between difficult implementation and numerical simulation consists in using the SIL and PIL co-simulation techniques[18].

Model-based design is notably different from conventional design methodology. Rather than employing complex structures and large software code, the control engineer can apply model-based design to define plant models with advanced functional characteristics using continuous-time and discrete-time building blocks. These built models employed with simulation tools such as Matlab/Simulink that can lead to rapid prototyping, control design testing, and verification through the software in the loop SIL and processor in the loop PIL simulations [19].

In this dissertation, nonlinear control strategy based on second order sliding mode control is adopted for the control of both point-to-point and back-to-back VSC-based HVDC systems. The main purpose here is to enhance the performance of the VSC-HVDC systems by controlling the active and reactive powers and DC-link voltage using second order sliding mode control instead of conventional control. In order to validate the proposed control system, software in the loop (SIL) and processor in the loop (PIL) simulations are performed to make sure that the control part is ready for eventual real time implementation.

In order to achieve these research objectives, this dissertation is divided into four chapters, which are summarized as follows:

The first chapter will have two essential parts. The first part will be devoted to the discussion of the different HVDC technologies as well as a brief comparison between the HVDC and the HVAC transmission. Also some of the HVDC applications and several configurations suitable for each use with their advantages will be detailed.

The first part of the second chapter will be dedicated to the modeling of the VSC based HVDC. The second part will be consecrated on an oriented vector control of HVDC systems based on three kinds of PI-based controllers. The first uses a traditional PI regulator, the second combines a PI regulator with a nonlinear feed-forward, and the third introduces an extended state observer to compensate for disturbances and enhance the DC voltage regulation loop.

The third chapter will be aimed to enhance the HVDC systems control by applying the first order sliding mode control as well as the second order sliding mode control based on super twisting algorithm. At last, a comparison between these two control techniques will be also considered.

The fourth chapter will be reserved first to detail the model-based design approach and its application in the Simulink environment. After that, SIL and PIL simulations will be performed in order to test and validate the second order sliding mode controller designed in the previous chapter.

Chapter I

VSC-HVDC Systems Presentation

I.1 Introduction

Nowadays, electrical energy production plants based on energy sources are more and more widespread and distant from load centers. So, it is imperative to obtain a suitable way of transmission to transmit energy from the power plants to AC systems [20]. From a technical and economical perspective, the VSC-HVDC transmission is a possible solution since it has multiple advantages. In fact, the VSC-HVDC system can alone manage active and reactive powers and conduct flow reversal power without altering the polarity of the voltage. It can also operate without large AC filters [20]. In addition, it can also be used easily in multiple locations to link the main grid with large offshore farms, onshore wind farms, or solar power plants.

This chapter is an outline of the VSC-based HVDC transmission systems. First of all, the chapter will present a comparison between HVDC and HVAC transmission systems. Moreover, it will briefly display multiple basic applications where the HVDC transmission systems are convenient. The chapter will then resume with a presentation of the VSC-based HVDC transmission systems. And later, the benefits of such systems and their configurations are also debated.

I.2. Introduction to HVDC Transmission System

The comparison between the HVDC transmissions and the HVAC transmission can be viewed by two perspectives: from the transmission costs or the technical point of views. By analyzing the transmission costs of the two systems, the following advantages of HVDC transmission systems over the HVAC transmission systems can be established [21]:

- Regarding similar insulating requirements for maximum voltage levels, a DC cable carries the same amount of power with two conductors as an AC cable with three conductors; and thus, for the same power level, an HVDC transmission system, compared to a classical HVAC transmission, will require smaller Right-of-Way, simpler towers as well as lower conductor and insulator costs;

- The absence of the skin effect in the use of an HVDC transmission can be noticed. Also, the dielectric and corona losses are kept at a low level, thus the efficiency of the transmission is increased;
- The power transmission losses (conductor losses) are lowered by approximately two-thirds when the AC option is replaced with the DC one;
- The drawback of the HVDC transmissions regarding the costs is due to the use of power converters and filters.

In conclusion, it can be said that the HVAC transmissions are more economical than HVDC transmissions when used for small distances. Once the breakeven distance is reached the DC alternative becomes more economical fact, which may be observed from Figure (I.1).

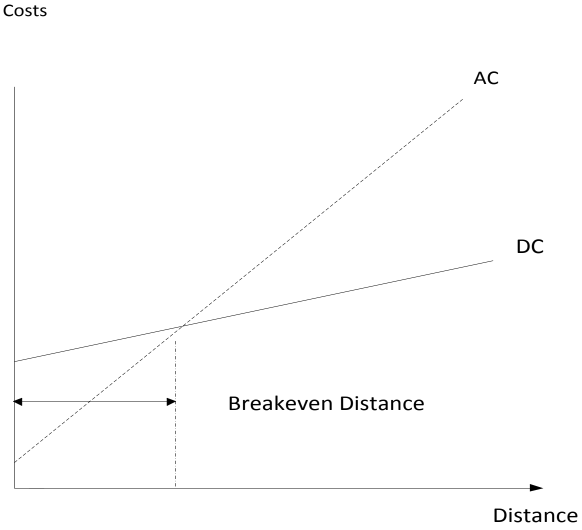


Figure (I.1): Comparison of AC/DC lines - breakeven distance

In the case of the overhead lines, the breakeven distance can vary between 400 to 700 km, depending on the per-unit line costs, while if a cable system is used the breakeven distance varies between 25 and 50 km [21]. The typical breakeven distance for overhead lines is 500 km [22]. Analyzing the two transmission systems, from the technical point of view, the HVDC transmissions overcome some of the problems, which are usually associated with the AC transmissions. Thus, the stability limits are overcome when an HVDC transmission is used since the power carrying ability of DC lines is not affected by the transmission distance. In the case of the HVAC transmission, the power transfer in the AC lines depends on the phase angle, which increases with the distance, and thus the power transfer is limited. The second problem, which is solved by using the DC transmission instead of the AC transmission, is the line charging. In the case of an HVAC transmission, line compensation (using STATCOMs, SVCs, etc.) is used to solve the line charging issue, while in the case of DC lines such compensation is not required [21], [22]. Due to this issue, in the case of HVAC transmission, the breakeven distance is reduced to 50 km. Moreover, the asynchronous interconnection of two AC power systems can be realized using HVDC technology.

I.3 HVDC Systems Applications

- Stabilization of power flows in integrated power systems

According to [21], due to the fast controllability of DC energy, strategically installed DC lines can solve issues like power flow in AC ties, which can be uncontrollable and can lead to overloads and stability problems. One example of using HVDC transmission systems in such a project is the Intermountain Power Project (IPP) link in the USA [21].

- Offshore transmission

Because of its benefits, such as self-commutation, black-start capability, and dynamic voltage control, VSC-based HVDC transmissions can be used to serve isolated loads on islands or offshore platforms [23]. Moreover, VSC-based HVDC transmission systems can provide reactive power support to wind farms as well as interconnection points.

I.4. HVDC System Configurations

Based on the functions and the locations of the converter station, four main HVDC system configurations are used in power system transmissions. These configurations can be used for both VSCs and CSCs converter topologies [24].

I.4.1.Monopolar HVDC System

In this configuration, two converters separated by a single-pole line are used. Positive or negative DC voltage can be used, but in the case of using negative polarity, the corona effects in the DC line are less [21]. Depending on the application, in the case of the monopolar configuration, ground or a metallic conductor can be used as a return path, as illustrated in Figure (I.2).

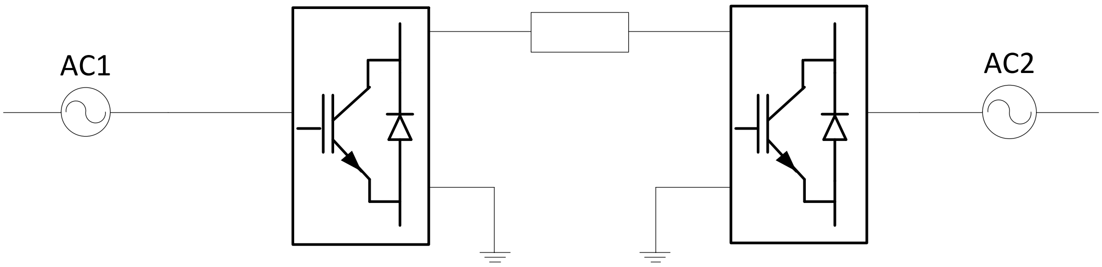


Figure (I.2): Monopolar HVDC system

This configuration is usually preferred in the case of cable transmissions with submarine connections [24].

I.4.2. Bipolar HVDC System

In this case, the configuration uses two conductors, one positive and the other negative. The connection between the two sets of the converter is grounded at one or both ends [21]. The bipolar system consists of two monopolar systems. The advantage of this configuration is given by the fact that one of the poles can continue to transmit power in case the other one is out of service [21], [24]. Thus, the two poles may be used independently, if both neutral points are grounded [25]. The bipolar HVDC system configuration is illustrated in Figure (I.3).

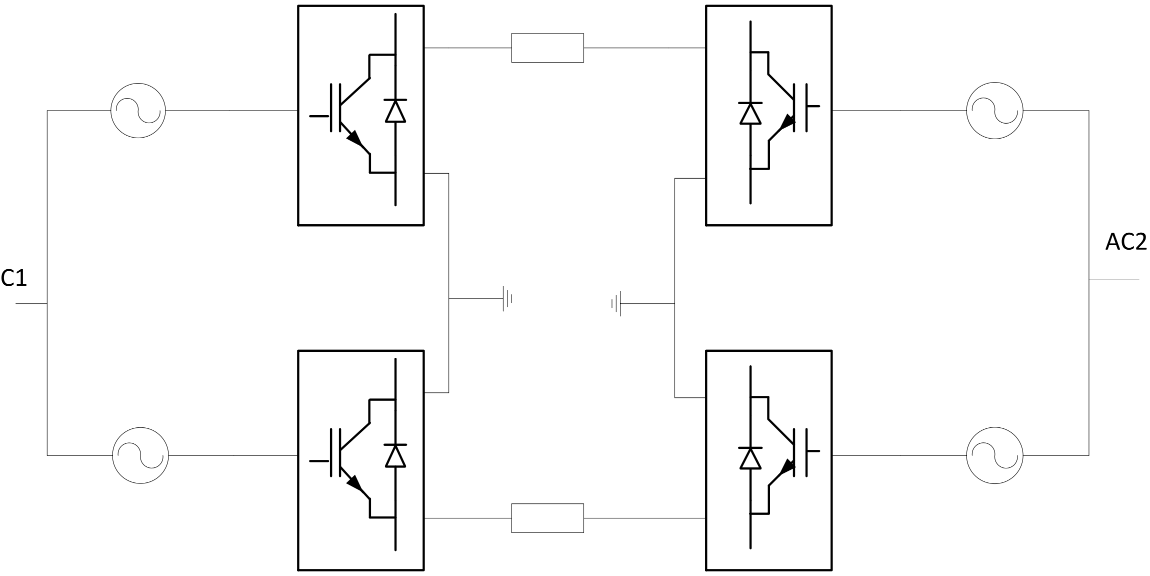


Figure (I.3): Bipolar HVDC system

Theoretically the ground current is zero in this configuration since both poles operate with equal current [21], [24]. Based on the above presented points, this is the most common configuration for modern HVDC transmission lines [23], [24].

I.4.3. Back-to-Back HVDC System

The two converters stations in this configuration are placed at the same site and there is no transmission of power with a DC link over a long distance [24]. The block diagram of a back-to-back system is presented in Figure (I.4).

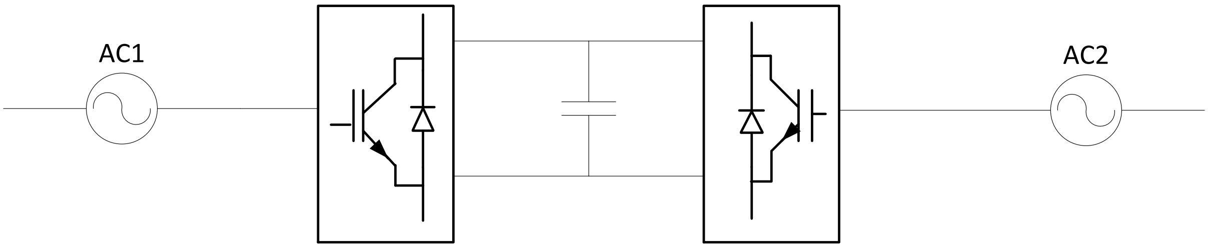


Figure (I.4): Back-to-back HVDC System

The back-to-back HVDC system is used two interconnect two AC systems, which may have different frequencies (asynchronous interconnection) [23].

I.4.4. Multi-terminal HVDC System

A multi-terminal HVDC transmission system consists of three or more converter substations, some of them working as inverters while the other ones as rectifiers [26]. Depending on the positioning of the converter substations, two basic arrangements of the multi-terminal HVDC system can be obtained: series multi-terminal HVDC system and parallel multi-terminal HVDC system. These two arrangements are presented in Figure (I.5).

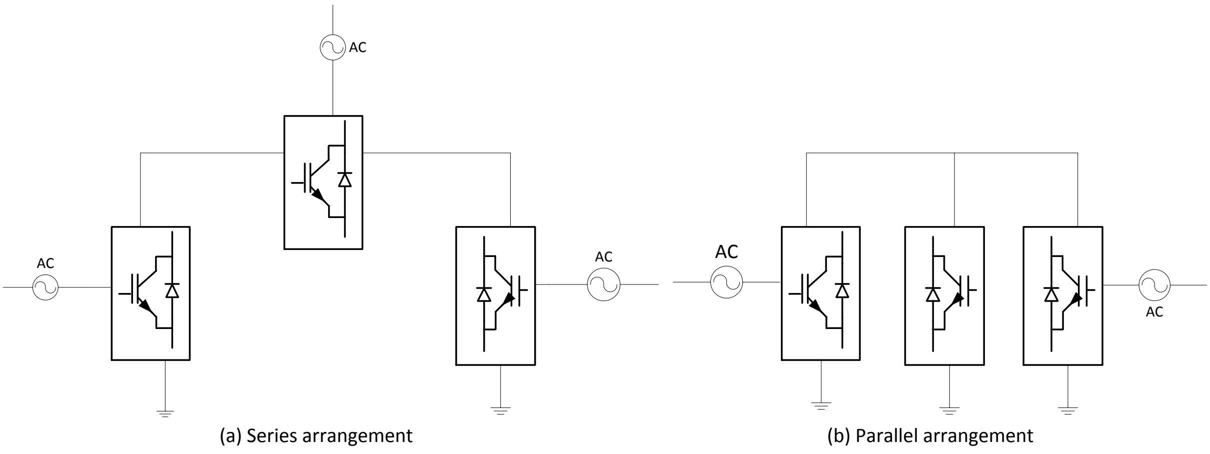


Figure (I.5): Multi-terminal HVDC systems

A combination of series and parallel connections of the converters forms a hybrid multiterminal HVDC transmission system.

I.5. VSC Based HVDC Transmission System

The HVDC can be classified into two subcategories: LCC HVDC and VSC HVDC. The former is the "classic" HVDC technology, using power thyristors as the main components for converting AC to DC and vice versa[11] [27].

The VSC HVDC technology was developed during the 1990s, and the earliest commercial transmission link was approved in 1997, also on the Swedish island of Gotland in the Baltic Sea[11]. VSC is based on power transistors, IGBTs (Insulated Gate Bipolar Transistors), as the converting components. IGBTs, being more controllable devices than thyristors, make VSC HVDC a more flexible technology than LCC HVDC, and efficiently adaptable for transmissions from renewable and variable power sources such as wind farms. VSC HVDC technology is also proper for developing DC grids, interconnecting groups of wind farms, or solar power installations for feeding mainland HVAC grids at various locations [22][27].

Both HVDC technologies are quite comparable, sharing the same familiarity base and the similar auxiliary subsystems. To put it clearly, VSC HVDC provides a flexible strategy to geographically dispersed production systems and for grid construction, while LCC HVDC has very high power transmission capability, supplying power over large distances from large hydropower plants to population and industrial centers. HVDC equipment and know-how is commercially available from several manufacturers[27].

I.5.1. Advantages of VSC-based HVDC Systems

By analyzing the operation of both classic HVDC technology and VSC-based HVDC technology, the main difference can be considered as: the controllability. In the case of VSC-based HVDC technology, the controllability is higher compared with the one of the earlier developed technology. Thus, if VSCs are used instead of line-commutated LCCs several benefits can be noted, some of which are stated below:

- VSC converter technology supply fast and independent control of active and reactive powers without requiring additional compensating equipment; the reactive power can be controlled at both terminals independently of the DC transmission voltage level [21], [22], [23], [24];

- Self (forced) commutation with voltage source converters allows black start, which means that the VSC is used to synthesize a balanced set of three-phase voltages as a virtual synchronous generator [22], [23];
- Commutation failures due to disturbances in the AC network can be lessened or even avoided by the usage of VSC-HVDC technology [24];
- VSC-HVDC system can be connected to a ”weak” AC network or to a network where there are no available generation source (the VSC can work independently of any AC source), so the short circuit level is low [24];
- Because of its modular, compact and standardized build, the converter can be easily and quickly installed at the desired site [21];
- The VSCs do not have any reactive power demand, and they can control their reactive power to regulate the AC system voltage like a generator [23], contrarily to the classic HVDC system.

Nonetheless, the VSC-based HVDC technology has a few disadvantages, which include high cost (caused by the converter stations) and potentially high power losses compared with traditional HVDC technology.

I.5.2. Typical VSC-based HVDC Transmission System Configuration

The typical configuration of VSC-based HVDC transmission system is presented in Figure (I.6).

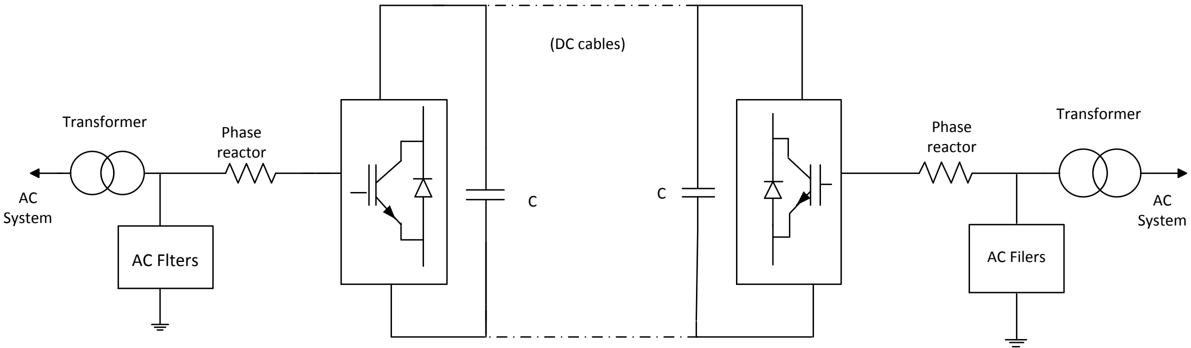
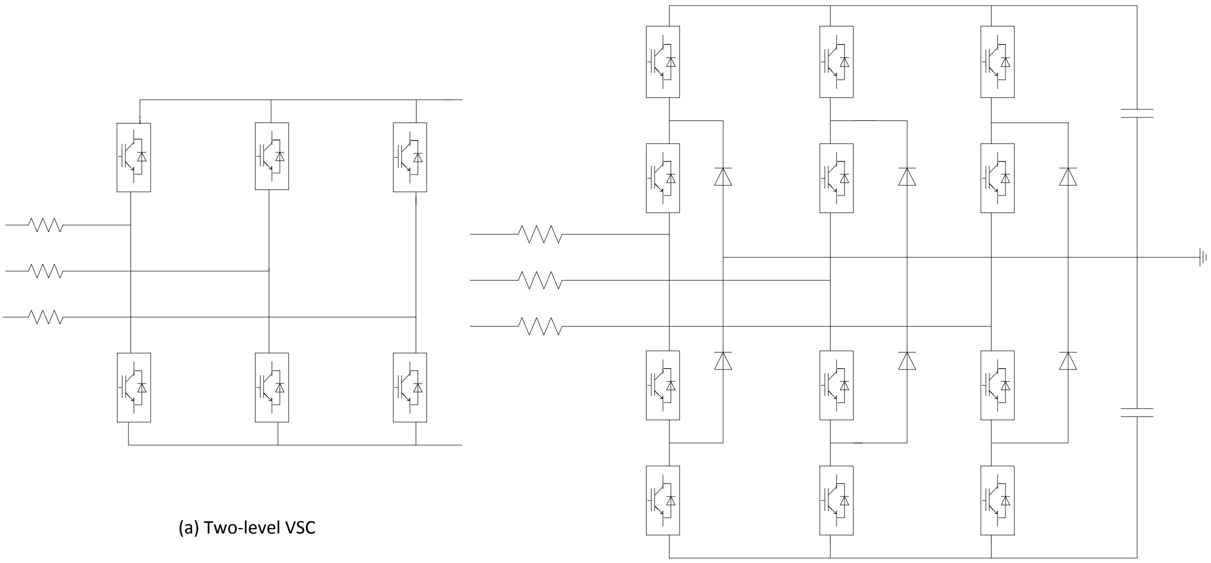


Figure (I.6): Typical VSC-HVDC system

This kind of transmission system includes two voltage source converters, transformers, phase reactors, AC filters, DC-link capacitors, and DC cables. Each of these components will be briefly introduced in the up-coming paragraphs.

I.5.2.1. Voltage Source Converter

The two VSCs can be considered the core of this transmission system topology. One of the VSCs serves as a rectifier, while the other one serves as an inverter, and both of them are based on IGBT power semiconductors. The two VSC stations are connected through an overhead line or a DC transmission line. Mainly, two basic configurations of VSCs are used on the HVDC transmission system; the two-level VSC converter, presented in Figure (I.7.a), and the three-level VSC converter, which is presented in Figure (I.7.b).



(a) Two-level VSC

(b) Three level VSC

Figure (I.7): Possible VSI topologies

The two-level VSC is the simplest configuration suitable for HVDC transmission. This converter consists of six valves (each valve consists of an IGBT and an anti-parallel diode) and can generate two voltage levels. In high power applications, the three-level VSC configuration (see Figure (I.7.b)) that consists of four valves per leg represents a reliable alternative to the two-level VSC configuration, since the phase potentials can be modulated between three voltage levels.

I.5.2.2. Transformer

In Figure (I.6), the transformers are used to interconnect the VSC with the AC network. The main function of the transformers is to adapt the voltage level of the AC network to a voltage level suitable to the converter. This voltage level can be controlled using a tap changer, which will maximize the reactive power flow [29].

I.5.2.3. Phase Reactor

The phase reactors, known also as converter reactors, are used to continuously control the active and reactive power flow. According to [27], phase reactors have three main functions:

- Providing low-pass filtering of the PWM pattern to get the desired fundamental frequency voltage;
- Providing active and reactive powers control; the active and reactive power flow between the AC and DC sides is defined by the fundamental frequency voltage across the reactors;
- Limiting the short-circuit currents.

Typically, the short-circuit voltage of the phase reactor is 15%.

I.5.2.4. AC Filter

The main goal of the AC filters is to eliminate the harmonic content, which was created by using the PWM technique, of the output AC voltage. Otherwise, if these harmonic components are not eliminated or reduced, malfunctioning in the AC grid will appear.

Typical requirements for AC filters are: individual harmonic distortion level (Dh ≈ 1%), total harmonic distortion (THD) level may vary between 1.5% and 2.5%, and telephone influence factor (TIF) between 40 and 50 [27].

Depending on the wanted filter performances or requirements, the filter configuration is deviating from application to application. In a typical HVDC Light scheme, the AC filter consists of two or three grounded /ungrounded tuned filter branches [27].

I.5.2.5. DC-link Capacitor

As shown in Figure (I.6), on the DC side, there are two capacitor stacks of the same power rating. The DC capacitor serves as an energy store and it decreases the harmonics ripple on the DC voltage. Depending on the size of the DC side capacitor, DC voltage variations caused by interruptions in the system (e.g. AC faults) can be limited [27].

I.5.2.6. DC Cable

Mainly, three types of DC cables are suitable for HVDC transmission systems. These are: the self-contained fluid-filled (oil-filled, gas-pressurized) cables, the solid cables, and XLPE cables polymer extruded cables. The last-mentioned type seems to be the preferred choice for the VSC-based HVDC transmission system, because of its mechanical strength, flexibility, and low weight [24].

I.6. Voltage Quality

Other important requirements imposed usually by transmission system operators (TSOs) concern the voltage quality aspects. In this case, requirements from three main topics have to be fulfilled:

- Rapid voltage changes

A rapid voltage change can be defined as a single rapid change of the RMS value of the voltage and it may occur in the wind farms due to the breaker switching [30].

- Voltage fluctuations and flicker

According to [30], the flicker contributions, P_{st} and P_{lt}, do not have to exceed some well established limits:

$$\begin{aligned} P_{st} &< 0.3 \\ P_{lt} &< 0.2 \end{aligned} \tag{I.1}$$

The flicker coefficient P_{st} is determined as a weighted average of the flicker contribution during ten minutes, while the coefficient P_{lt} is determined as a weighted average of the flicker contribution during two hours [30]. Both coefficients are defined in IEC/TR 61000-3-7 standard [31].

In [30], two main requirements regarding harmonics are stated. The harmonic disturbance for each individual harmonic, given by relation (I.2), shall be lower than 1 per cent for $1 < n < 51$ at PCC.

$$D_n = \frac{U_n}{U_l} \times 100\% \qquad \text{(I.2)}$$

The second requirement concerns the total harmonic distortion (THD) coefficient, given by(I.3), which must be smaller than 1.5 per cent.

$$THD = 100\sqrt{\sum_{n=2}^{50}\left(\frac{U_n}{U_l}\right)^2}\ \% \qquad \text{(I.3)}$$

I.7VSC-HVDC System Capability Diagram

Since active power and reactive powers are independent of each other, VSC can theoretically operate at any point on the *P*, *Q* plane. In this plane, Q is represented by a circle because of the ability to operate in one of the four quadrants. Factors affecting the range of operation of the converters are the maximum current passing through the converter switches and the maximum DC voltage value. A maximum current limitation is required to protect the inverter switches. Therefore, the VSC will operate in the nominal current corresponds to a circle of 1 pu [32].

Active power transfer capability, which requires a minimum voltage amplitude to be transmitted. The steady state and dynamic operation differ due to the parameters that limit the change in the diagram (*P*, *Q*) during operation. As analogy between the synchronous generator and the VSC capacity curve, the maximum current that can pass through the inverter switches is the induced current. The voltage limit of the converter corresponds to the maximum field current and finally the maximum power via the DC cable is the maximum power of the turbine. Figure (I.8) gives an idea about limiting factors. The first one is that the maximum current through the IGBT gives the maximum MVA circle. MVA capacity directly proportional to the alternating voltage. The second limiting factor is the maximum DC voltage that regulates the AC voltage via the converter. The reactive power exchange depends directly on the difference between the alternating voltage generated by VSC and the alternating network voltage. The third limiting factor is the maximum current in the DC cables. For low alternating voltage, the MVA limit is dominant but in case of high alternating voltage, the DC limit is quite restrictive[32].

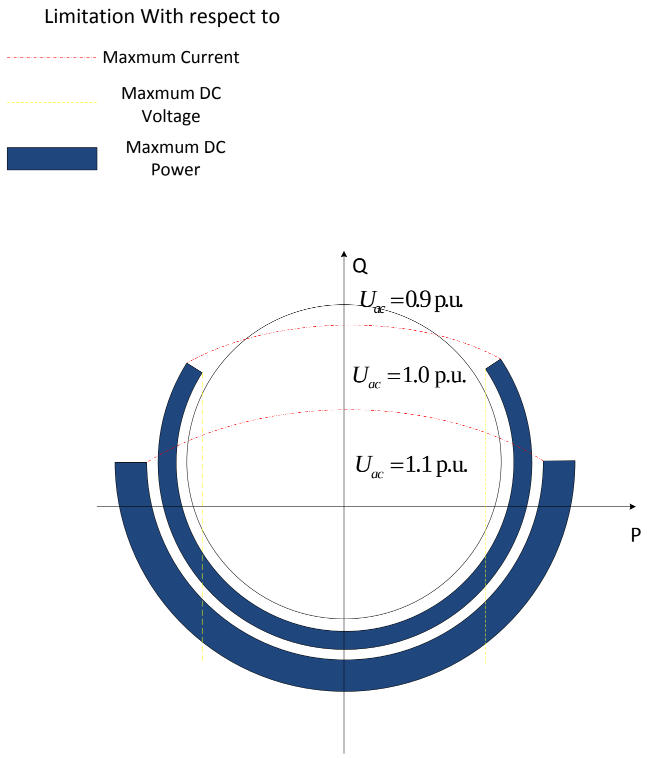


Figure (I.8):VSC-HVDC capability table

I.8 Conclusion

The purpose of this chapter was to introduce various aspects concerning HVDC systems in general and VSC-based HVDC transmission systems in particular. Thereby, the first part of this chapter was dedicated to the HVDC systems introduction. To show why the HVDC technology is more and more used in different applications, a comparison between HVAC transmissions and HVDC transmissions was presented and the advantages of the first technology were highlighted. These advantages make the HVDC transmission systems suitable for several applications, such as long-distance bulk power transmissions, the asynchronous connection of AC power systems, etc. The second topic addressed in this chapter was about basic HVDC system configurations. The four main configurations namely monopolar, bipolar, back-to-back, and multi-terminal were briefly explained. The VSC-based HVDC transmission system technology was the next topic explained and discussed. The advantages of this topology over the classic HVDC transmission topology were presented. The chapter ends with the basic configuration of a typical VSC-based HVDC system followed by a short description of each component.

Chapter II

Modeling and PI Based Control of HVDC Systems

II.1 Introduction

The demand for more manageable and reliable HVDC systems along with the remarkable potential of modern control and power electronics has directed to the development of the VSC based HVDC transmission grids. The advancement in power electronics converters is allowing technology to transform traditional power systems into modern HVDC since they allow controlling the power flows and bus voltages in the millisecond's range. In particular, VSC with bidirectional power capability is the key element in recent HVDC systems. The different configurations of the HVDC system need power converter structures based on two VSC converters. Each converter needs active power or DC voltage control capability to transmit high-quality power while exchanging the appropriate reactive power with the power grid. Thus the control of a VSC-HVDC system is essentially based on the control of energy transmission, aiming to control the transmitted power as well as the independent control of active and reactive powers[33].

In this chapter, after presenting the structure of the VSC based HVDC system, a mathematical model of the system based on two-level three-phase converters will be established. Based on the developed model, a control system is designed to control the power flow and regulate the DC bus voltage of two HVDC configurations namely back-to-back and point-to-point. Furthermore, with the aim of improving the dynamics of DC-link voltage, a PI controller based on extended sate observer and a nonlinear feed-forward compensation for the DC-link voltage regulation will be considered.

II.2 VSC-Based HVDC System Structure

Figure (II.1) illustrates a schematic diagram of a standard configuration of a VSC-based HVDC system (whether it is a point-to-point or a back-to-back configuration). The HVDC conversion system is composed of two VSCs; both VSCs employ the two-level VSC as their power converters labeled as VSC1 and VSC2. Figure(II.1) also shows that VSC1 (VSC2) is interfaced with an AC system, that is, Grid1 (Grid2), through an interface transformer at the point of common coupling PCC1 (PCC2). Also to lessen switching current/voltage harmonics, a shunt and well-tuned filter is connected to PCC1 (PCC2)[32],[14],[34].

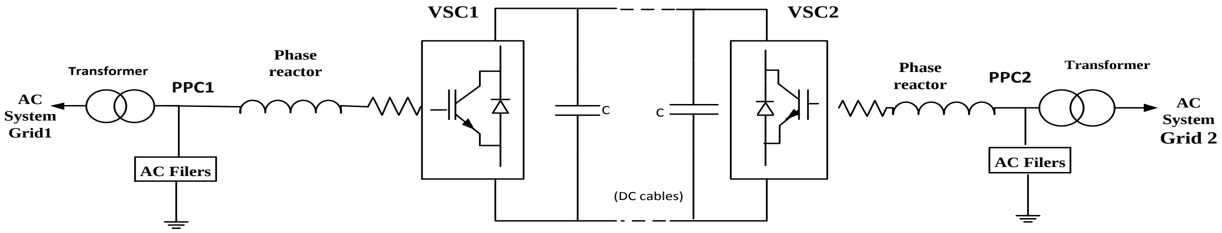


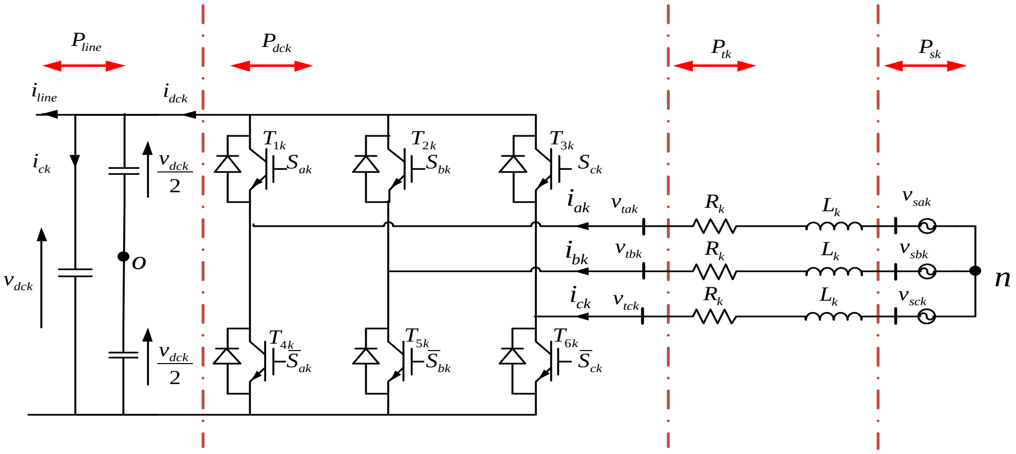
Figure (II.1): Schematic diagram of a standard configuration of a VSC-based HVDC system

In this chapter, each grid will be represented by a three-phase voltage source in series with equivalent impedance (phase reactor). The phase reactor is used to control the active and reactive powers by controlling the current passing through it.

II.3 Modeling of VSC-Based HVDC System

II.3.1 VSC Based HVDC System Description

Figure (II.2) presents a basic structure of VSC-HVDC substation, which consists of a source voltage converter connected to an AC network through a series *RL* phase reactor. The voltage level of the AC network must be suitable for the converter; otherwise a transformer is used to accomplish that. The converter DC side is connected in parallel with a capacitor that is capable of maintaining the DC-link voltage and attenuating high-frequency voltage ripples[32][34].



Figure(II.2):Basic structure of a VSC based HVDC substation

To avoid redundancy in mathematics formulations, quantities of the first converter and first grid system are indexed by "*k=1*", while those of second converter and second grid system are indexed by "*k=2*".

The three-phase voltages of each symmetrical AC system are defined as:

$$\begin{aligned} v_{sak} &= V_{mk}\sin\left(\omega_k t\right) \\ v_{sbk} &= V_{mk}\sin\left(\omega_k t - \frac{2\pi}{3}\right) \\ v_{sck} &= V_{mk}\sin\left(\omega_k t + \frac{2\pi}{3}\right) \end{aligned} \tag{II.1}$$

where V_{mk} represents the amplitude of the phase voltage, ω_k represents the angular frequency, $k = 1$ for the first AC alternative system 1 and $k = 2$ for the second AC system.

The converter can be considered as an equivalent AC voltage source where the amplitude, phase, and frequency can be controlled separately. Therefore the VSC bridge can be seen as a very fast controllable synchronous machine whose instantaneous phase voltages v_{tabck} , are described by [33]:

$$v_{tabck} = V_{mfk}\sin(\omega_{fk} t + \delta_k) + harmonics \tag{II.2}$$

where V_{mfk} is the peak value of the modulating wave, ω_{fk} is the fundamental frequency, and δ_k is the phase shift of the output voltage.

Variables V_{mfk} and δ_k can be regulated separately to achieve any combination of voltage amplitude and phase shift with the fundamental frequency voltage of the AC system. Therefore the voltage drop across the reactor *RL* can be alternated to control the active and reactive power flows[35].

The active power flow on the AC side is equivalent to the active power transmitted from the DC side in steady-state, neglecting the losses. This can be achieved if one of the two converters controls the active power transmitted and the other controls the direct voltage. The reactive power generated/consumed by the converter is adjusted to control the AC network voltage or/and reactive power injections [35].

II.3.2Modeling of VSC System

The two-level VSC consists of three identical half-bridge converters, with two semiconductors switches IGBT (Isolated Gate Bipolar Transistors) and anti-parallel diodes to ensure continuity of the current; thus it can provide a bidirectional power-flow path between the DC-side and the three-phase AC system. All of these elements are considered as ideal switches.

II.3.2.1Averaged VSC Model

The VSC converter is based on the discrete states resulting from the IGBTs switching, but for control design purposes it is useful to acquire a more simplified equivalent model. A simplified averaged converter model (a non-harmonic model), decoupling the DC and AC parts of the converter, can be derived as illustrated in Figure(II.3). The model is based on the power balance between the DC and AC sides. This model is described by a current source on the DC side with a value equal to the current required to reach the active power injected for a measured voltage and three controllable voltages sources with the instantaneous magnitude from the modulator. In another word, the current source in the DC side reflects the active power exchanged between the AC and the DC side and ensures the system power balance. The lossless model also includes the DC capacitor[33],[32].

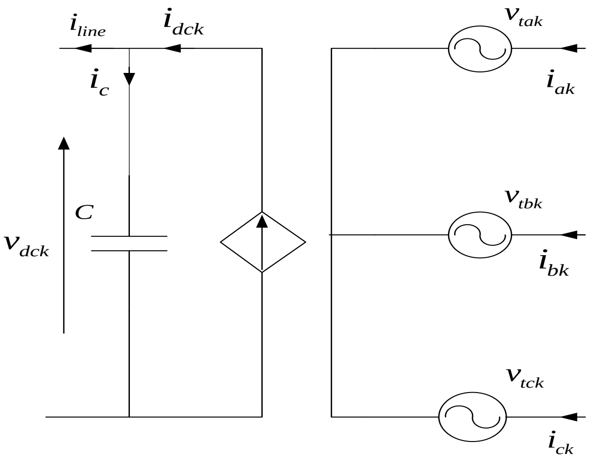


Figure (II.3): Averaged converter model circuit

The active power on the DC side is expressed as in equation (II.3) and the instantaneous active power on the converter AC side as in equation (II.4).

$$P_{dck} = v_{dck}\, i_{dck} \tag{II.3}$$

$$P_{tk} = v_{tak} i_{ak} + v_{tbk} i_{bk} + v_{tck} i_{ck} \tag{II.4}$$

If the converter and commutation losses are neglected, the DC side power is equal to the converter AC side terminal power P_{tk} and if the instantaneous power of the AC-side phase reactor is not considered, the converter AC-side terminal power P_{tk} is equal to the grid side power P_{sk}.

II.3.2.2Switched VSC Model

The two-level VSC shown in the Figure (II.2)operates based on the turn ON/OFF of the switching elements depending on the state of the control signals (S_{ak}, S_{bk}, S_{ck}) that are issued from PWM strategy.

The waveform of the AC side terminal voltage v_{txk} is independent of the polarity of i_{xk} and is uniquely determined by the switching functions defined by:

$$S_{xk} = \begin{cases} 1 & \text{if } \mathrm{T}_{xk} \text{ is close and } \mathrm{T}_{(x+3)k} \text{ is open} \\ 0 & \text{if } \mathrm{T}_{xk} \text{ is open and } \mathrm{T}_{(x+3)k} \text{ is close} \end{cases} \qquad x = a,b,c \tag{II.5}$$

From Figure (II.2), the voltages of the VSC can be derived as a function of the states of the switches, the potentials of the nodes a, b, and c of the converter with respect to the imaginary midpoint O are given by the equation (II.6):

$$\begin{cases} v_{aok} = \dfrac{v_{dck}}{2}(2S_{ak} - 1) \\ v_{bok} = \dfrac{v_{dck}}{2}(2S_{bk} - 1) \\ v_{cok} = \dfrac{v_{dck}}{2}(2S_{ck} - 1) \end{cases} \tag{II.6}$$

The line-to-line voltages of the converter are denoted as a function of the switch states as follows:

$$\begin{cases} v_{abk} = v_{aok} - v_{bok} = v_{dck}(S_{ak} - S_{bk}) \\ v_{bck} = v_{bok} - v_{cok} = v_{dck}(S_{bk} - S_{ck}) \\ v_{cak} = v_{cok} - v_{aok} = v_{dck}(S_{ck} - S_{ak}) \end{cases} \tag{II.7}$$

Line-to-line voltages can be expressed depending on the VSC line voltages as follows:

$$\begin{cases} v_{abk} = v_{ank} - v_{bnk} \\ v_{bck} = v_{bnk} - v_{cnk} \\ v_{cak} = v_{cnk} - v_{ank} \end{cases} \tag{II.8}$$

This gives:

$$\begin{cases} v_{abk} - v_{cak} = v_{ank} - (v_{bnk} + v_{cnk}) + v_{ank} \\ v_{bck} - v_{abk} = v_{bnk} - (v_{cnk} + v_{ank}) + v_{bnk} \\ v_{cak} - v_{bck} = v_{cnk} - (v_{ank} + v_{bnk}) + v_{cnk} \end{cases} \tag{II.9}$$

In a balanced three-phase system, the sum of the voltages is zero, so:

$$v_{ank} + v_{bnk} + v_{cnk} = 0 \tag{II.10}$$

From relation (II.9), one can write:

$$\begin{cases} v_{ank} = -(v_{bnk} + v_{cnk}) \\ v_{bnk} = -(v_{ank} + v_{cnk}) \\ v_{cnk} = -(v_{ank} + v_{bnk}) \end{cases} \tag{II.11}$$

By replacing (II.11) in (II.9), line-to-neutral voltages of the VSC as a function of the line-to-line voltages can be obtained as:

$$\begin{cases} v_{ank} = \dfrac{v_{abk} - v_{cak}}{3} \\ v_{bnk} = \dfrac{v_{bck} - v_{abk}}{3} \\ v_{cnk} = \dfrac{v_{cak} - v_{bck}}{3} \end{cases} \tag{II.12}$$

From (II.12) and (II.7), the line voltages of the converter can be written according to the states(S_{ak}, S_{bk},S_{ck}), and the DC-link voltage as follows:

$$\begin{cases} v_{tak} = \dfrac{v_{dck}}{3}(2S_{ak} - S_{bk} - S_{ck}) \\ v_{tbk} = \dfrac{v_{dck}}{3}(2S_{bk} - S_{ak} - S_{ck}) \\ v_{tck} = \dfrac{v_{dck}}{3}(2S_{ck} - S_{ak} - S_{bk}) \end{cases} \tag{II.13}$$

S_{ck}	S_{bk}	S_{ak}	v_{tak}	v_{tbk}	v_{tck}	$v_{\alpha k}$	$v_{\beta k}$	$\vec{v}_i$
0	0	0	0	0	0	0	0	$\vec{v}_0$
0	0	1	$\frac{-v_{dck}}{3}$	$\frac{-v_{dck}}{3}$	$\frac{2v_{dck}}{3}$	$\frac{-v_{dck}}{\sqrt{6}}$	$\frac{-v_{dck}}{\sqrt{2}}$	$\vec{v}_5$
0	1	0	$\frac{-v_{dck}}{3}$	$\frac{2v_{dck}}{3}$	$\frac{-v_{dck}}{3}$	$\frac{-v_{dck}}{\sqrt{6}}$	$\frac{v_{dck}}{\sqrt{2}}$	$\vec{v}_3$
0	1	1	$\frac{-2v_{dck}}{3}$	$\frac{v_{dck}}{3}$	$\frac{v_{dck}}{3}$	$-\sqrt{\frac{2}{3}}v_{dck}$	0	$\vec{v}_4$
1	0	0	$\frac{2v_{dck}}{3}$	$\frac{v_{dck}}{3}$	$\frac{v_{dck}}{3}$	$\sqrt{\frac{2}{3}}v_{dck}$	0	$\vec{v}_1$
1	0	1	$\frac{v_{dck}}{3}$	$\frac{-2v_{dck}}{3}$	$\frac{v_{dck}}{3}$	$\frac{v_{dck}}{\sqrt{6}}$	$\frac{-v_{dck}}{\sqrt{2}}$	$\vec{v}_6$
1	1	0	$\frac{v_{dck}}{3}$	$\frac{v_{dck}}{3}$	$\frac{-2v_{dck}}{3}$	$\frac{v_{dck}}{\sqrt{6}}$	$\frac{v_{dck}}{\sqrt{2}}$	$\vec{v}_2$
1	1	1	0	0	0	0	0	$\vec{v}_7$

Table (II.1): Possible voltage vectors of a VSC

The VSC can be described by eight possible switching states; six active and two null vectors. The possible switching states (S_{ak}, S_{bk}, S_{ck}), output three-phase voltages, and two-phase voltage vector components are given in Table (II.1). The switching polygon is illustrated in Figure (II.2)[37].

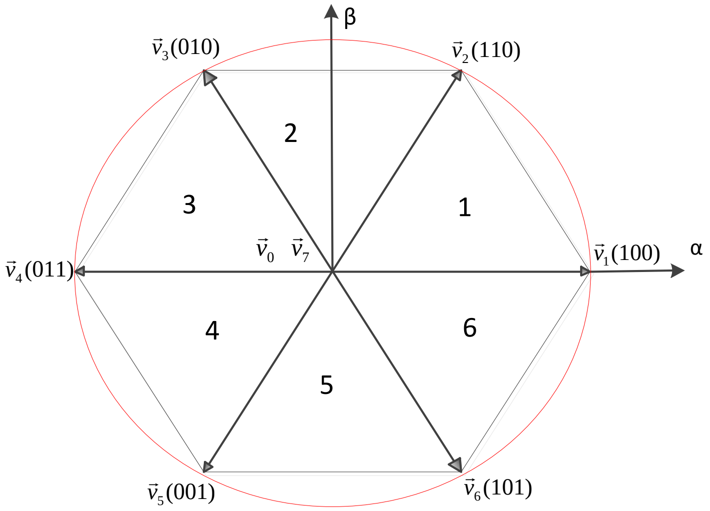


Figure (II.4): Representation of the switching polygon

By expressing (II.13) in a matrix form, the VSC conversion matrix is defined by the following equation:

$$\begin{bmatrix} v_{tak} \\ v_{tbk} \\ v_{tck} \end{bmatrix} = v_{dck} \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \end{bmatrix} \begin{bmatrix} S_{ak} \\ S_{bk} \\ S_{ck} \end{bmatrix} \tag{II.14}$$

The output current on the DC side is given by:

$$i_{dck} = \begin{bmatrix} S_{ak} & S_{bk} & S_{ck} \end{bmatrix} \begin{bmatrix} i_{ak} \\ i_{bk} \\ i_{ck} \end{bmatrix} \tag{II.15}$$

II.3.3 VSC AC Side Model in Natural Frame

By applying Kirchhoff's theorem, the current dynamics of the AC side can be written as follows:

$$L_k \frac{di_{abck}}{dt} + R_k i_{abck}(t) = v_{sabck} - v_{tabck} \tag{II.16}$$

where i_{abck} is the phase current; v_{sabck} is the grid voltage; v_{tabck} is the voltage at the PCC; R_k is the line resistance, and L_k is the line inductance.

Equation (II.16) represents a system, in which i_k is the state variable, v_{tk} is the control input, and v_{sk} is the disturbance input. The output of the system can, for example, be the power exchanged with the AC-side voltage source.

The equation (II.16) can be rewritten as:

$$\begin{aligned} L_k \frac{di_{ak}}{dt} &= -R_k i_{ak} + v_{sak} - v_{tak} \\ L_k \frac{di_{bk}}{dt} &= -R_k i_{bk} + v_{sbk} - v_{tbk} \\ L_k \frac{di_{ck}}{dt} &= -R_k i_{ck} + v_{sck} - v_{tck} \end{aligned} \tag{II.17}$$

The converter DC side is governed by:

$$C\frac{dv_{dck}}{dt} = (S_{ak} i_{ak} + S_{bk} i_{bk} + S_{ck} i_{ck}) - i_{line} \tag{II.18}$$

II.3.4 VSC AC Side Model in Stationary Frame

In order to simplify the previous VSC model, a transformation from the three-phase system to a virtual two-phase system is recommended. That gives:

$$\begin{cases} L_k \dfrac{di_{\alpha k}}{dt} = v_{s\alpha k} - v_{t\alpha k} - R_k i_{\alpha k} \\ L_k \dfrac{di_{\beta k}}{dt} = v_{s\beta k} - v_{tbk} - R_k i_{\beta k} \\ C\dfrac{dv_{dck}}{dt} = (S_{\alpha k} i_{\alpha k} + S_{\beta k} i_{\beta k}) - i_{line} \end{cases} \tag{II.19}$$

Where the source voltage vector components in the $\alpha\beta$ frame are given by the following expression:

$$\begin{bmatrix} v_{s\alpha k} \\ v_{s\beta k} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{sak} \\ v_{sbk} \\ v_{sck} \end{bmatrix} = \sqrt{\frac{2}{3}} V_{mk} \begin{bmatrix} \sin \omega_k t \\ \cos \omega_k t \end{bmatrix} \tag{II.20}$$

The converter terminal voltages in the $\alpha\beta$ frame are:

$$\begin{bmatrix} v_{t\alpha k} \\ v_{t\beta k} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{tak} \\ v_{tbk} \\ v_{tck} \end{bmatrix} \tag{II.21}$$

The currents are expressed in the same frame by:

$$\begin{bmatrix} i_{\alpha k} \\ i_{\beta k} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{ak} \\ i_{bk} \\ i_{ck} \end{bmatrix} \tag{II.22}$$

II.3.5 Model of Two-Level VSC in *dq*-Frame

In the rotating frame *dq*, the transformed converter model becomes:

$$\begin{cases} L_k \dfrac{di_{dk}}{dt} = v_{sdk} - v_{tdk} - R_k i_{dk} + \omega_k L_k i_{qk} \\ L_k \dfrac{di_{qk}}{dt} = v_{sqk} - v_{tqk} - R_k i_{qk} - \omega_k L_k i_{dk} \\ C \dfrac{dv_{dck}}{dt} = (S_{dk} i_{dk} + S_{qk} i_{qk}) - i_{line} \end{cases} \tag{II.23}$$

The transformation of the two-phase system (II.23) in the frame of reference *dq* requires having the transformation of the relationship between the voltages and currents within the two references.

The terminal converter voltages are transformed by:

$$\begin{bmatrix} v_{tdk} \\ v_{tqk} \end{bmatrix} = \begin{bmatrix} \cos\omega_k t & \sin\omega_k t \\ -\sin\omega_k t & \cos\omega_k t \end{bmatrix} \begin{bmatrix} v_{t\alpha k} \\ v_{t\beta k} \end{bmatrix} \tag{II.24}$$

The source voltages are transformed by:

$$\begin{bmatrix} v_{sdk} \\ v_{sqk} \end{bmatrix} = \begin{bmatrix} \cos\omega_k t & \sin\omega_k t \\ -\sin\omega_k t & \cos\omega_k t \end{bmatrix} \begin{bmatrix} v_{s\alpha k} \\ v_{s\beta k} \end{bmatrix} \tag{II.25}$$

Through substituting equation (II.20) in (II.25), it yields:

$$\begin{bmatrix} v_{sdk} \\ v_{sqk} \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{2}{3}} V_{mk} \\ 0 \end{bmatrix} = \begin{bmatrix} \sqrt{v_{s\alpha k}^2 + v_{s\beta k}^2} \\ 0 \end{bmatrix} \tag{II.26}$$

The currents are transformed by:

$$\begin{bmatrix} i_{dk} \\ i_{qk} \end{bmatrix} = \begin{bmatrix} \cos\omega_k t & \sin\omega_k t \\ -\sin\omega_k t & \cos\omega_k t \end{bmatrix} \begin{bmatrix} i_{\alpha k} \\ i_{\beta k} \end{bmatrix} \tag{II.27}$$

II.3.6 Instantaneous Powers in $\alpha\beta$ Frame

By considering balanced three-phase systems and by defining voltage and current phasors as $\overline{V}_{\alpha\beta} = v_\alpha + jv_\beta$ and $\overline{I}_{\alpha\beta} = v_\alpha + jv_\beta$,the power expression in $\alpha\beta$-frame can be expressed as[38]:

$$\overline{S} = P + jQ = \overline{\overline{V}_{\alpha\beta}\overline{I}_{\alpha\beta}}_{ref} = \left(v_\alpha + jv_\beta\right)\left(i_\alpha - ji_\beta\right) \tag{II.27}$$

By rearranging equation (II.27), it is possible to express the active and reactive powers as functions of voltages and currents in the $\alpha\beta$-frame as follows:

$$\begin{aligned} P &= v_\alpha i_\alpha + v_\beta i_\beta \\ Q &= v_\alpha i_\beta - v_\beta i_\alpha \end{aligned} \tag{II.28}$$

II.3.7 Instantaneous Powers in Synchronous Reference Frame

Similarly, by taking $\overline{V}_{dq} = v_d + jv_q$ and $\overline{I}_{dq} = v_d + jv_q$ as the voltage and current phasors in *dq* frame, the apparent complex power is[38]:

$$\overline{S} = P + jQ = \overline{V}_{dq}\overline{I}_{dqref} = \left(v_d + jv_q\right)\left(i_d - ji_q\right) \tag{II.29}$$

By reordering equation (II.29), active and reactive power can be expressed as:

$$\begin{aligned} P &= v_d i_d + v_q i_q \\ Q &= v_d i_q - v_q i_d \end{aligned} \tag{II.30}$$

II.4 Space Vector PWM

The utilization of self-commutating switches allows the voltage in a VSC to be modulated through the application of a high switching frequency Pulse Width Modulation (PWM) technique. In a PWM technique, the phase angle and magnitude can be instantaneously adjusted by changing the PWM pattern. The capability to change either the phase angle or magnitude implies that it is feasible to control the active and reactive power flow independently to achieve a power reversal. Among the different well-known modulation techniques is the Space Vector Modulation (commonly referred as SVM), which processes signals directly in the $\alpha\beta$ reference frame[37][39].

In two-level VSC, the different combinations (S_{ak},S_{bk},S_{ck}) can produce only eight possible space voltage vectors; two are zero vectors ($\vec{v}_0, \vec{v}_7$), and six have a module of $\sqrt{2/3}\,v_{dck}$, see Figure (II.5). To reproduce the reference vector, the $\alpha\beta$ plane is divided into six equal sectors. In each sector, the desired voltage vector is reconstructed by linear combination of the three adjacent vectors.

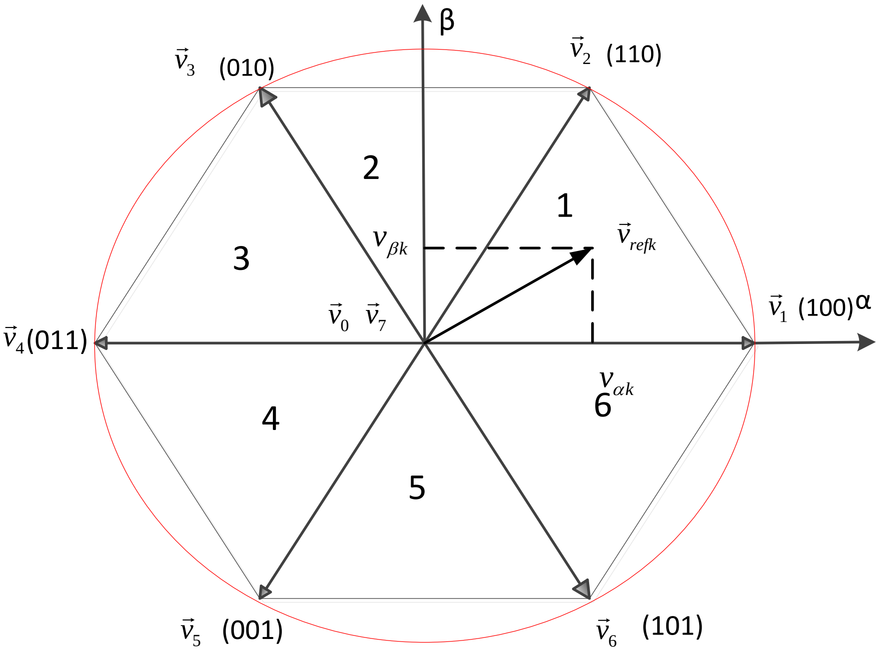


Figure (II.5):Converter voltage vectors diagram and the reference voltage vector

The SVM can be performed by achieving the following steps:

First step: Determination of the sector number (S)

The magnitude and the position of the reference voltage vector are determined from:

$$v_{refk} = \sqrt{v_{\alpha refk}^2 + v_{\beta refk}^2} \tag{II.31}$$

$$\vartheta = \tan 2^{-1}\left(\frac{v_{\beta refk}}{v_{\alpha refk}}\right) \tag{II.32}$$

Once the value of ϑ has been determined, the sector numbers are provided by:

$$S = ceil\left(\frac{\vartheta}{\pi/3}\right) \in (1,2,3,4,5,6) \tag{II.33}$$

Where *ceil* is a function that sets a given real number to an integer.

Second step: Calculation of application times

In the case where the reference vector is in the sector $S = i \in \{1,...,6\}$, the duration of application of the adjacent vectors $\vec{v}_{ik}$, $\vec{v}_{ik+1}$ are denoted by t_i , t_{i+1} , and by t_0 the duration of application of the null vectors. To ensure the equality of the average value of the voltage and its reference from an instant t , one must ensure that:

$$\frac{1}{T_h}\int_{t}^{t+T_h} \vec{v}_{refk}\,dt = \frac{1}{T_h}\left[\int_{t}^{t+t_1} \vec{v}_i\,dt + \int_{t+t_1}^{t+t_1+t_2} \vec{v}_{i+1}\,dt + \int_{t+t_1+t_2}^{t+T_h} \vec{v}_0\,dt\right] \tag{II.34}$$

In a very small sampling period T_h , the voltage v_{refk} is constant, the equation (II.34)can be simplified to:

$$\vec{v}_{refk} T_h = t_i \vec{v}_i + t_2 \vec{v}_{i+1} + t_0 \vec{v}_0 \tag{II.35}$$

For the sector $S = 1$, the reference voltage vector can be calculated using (II.35) as:

$$\vec{v}_{refk} = \frac{1}{T_h}\left(\vec{v}_1 t_1 + \vec{v}_2 t_2 + \vec{v}_0 t_0\right) \tag{II.36}$$

On the other hand, the reference voltage vector can be expressed as:

$$\vec{v}_{refk} = \vec{v}_{\alpha refk} + j\vec{v}_{\beta refk} \tag{II.37}$$

The voltage vectors $\vec{v}_0$, $\vec{v}_1, \vec{v}_2$ are:

$$\begin{cases} \vec{v}_0 = 0 \\ \vec{v}_2 = \sqrt{\dfrac{2}{3}} v_{dck} \left(\dfrac{1}{2} + j\dfrac{\sqrt{3}}{2}\right) \\ \vec{v}_1 = \sqrt{\dfrac{2}{3}} v_{dck} \end{cases} \tag{II.38}$$

By replacing(II.38)and(II.36)in(II.37) it results:

$$\begin{cases} v_{\alpha refk} = \sqrt{\dfrac{2}{3}} v_{dck} \dfrac{t_1}{T_h} + \dfrac{1}{\sqrt{6}} v_{dck} \dfrac{t_2}{T_h} \\ v_{\beta refk} = \dfrac{1}{\sqrt{2}} v_{dck} \dfrac{t_2}{T_h} \end{cases} \tag{II.39}$$

The solution of (II.39) gives:

$$\begin{cases} t_1 = \dfrac{\sqrt{6}v_{\alpha refk} - \sqrt{2}v_{\beta refk}}{v_{dck}} T_h \\ t_2 = \dfrac{\sqrt{2}v_{\beta refk}}{v_{dck}} T_h \\ t_0 = T_h - (t_1 + t_1) \end{cases} \tag{II.40}$$

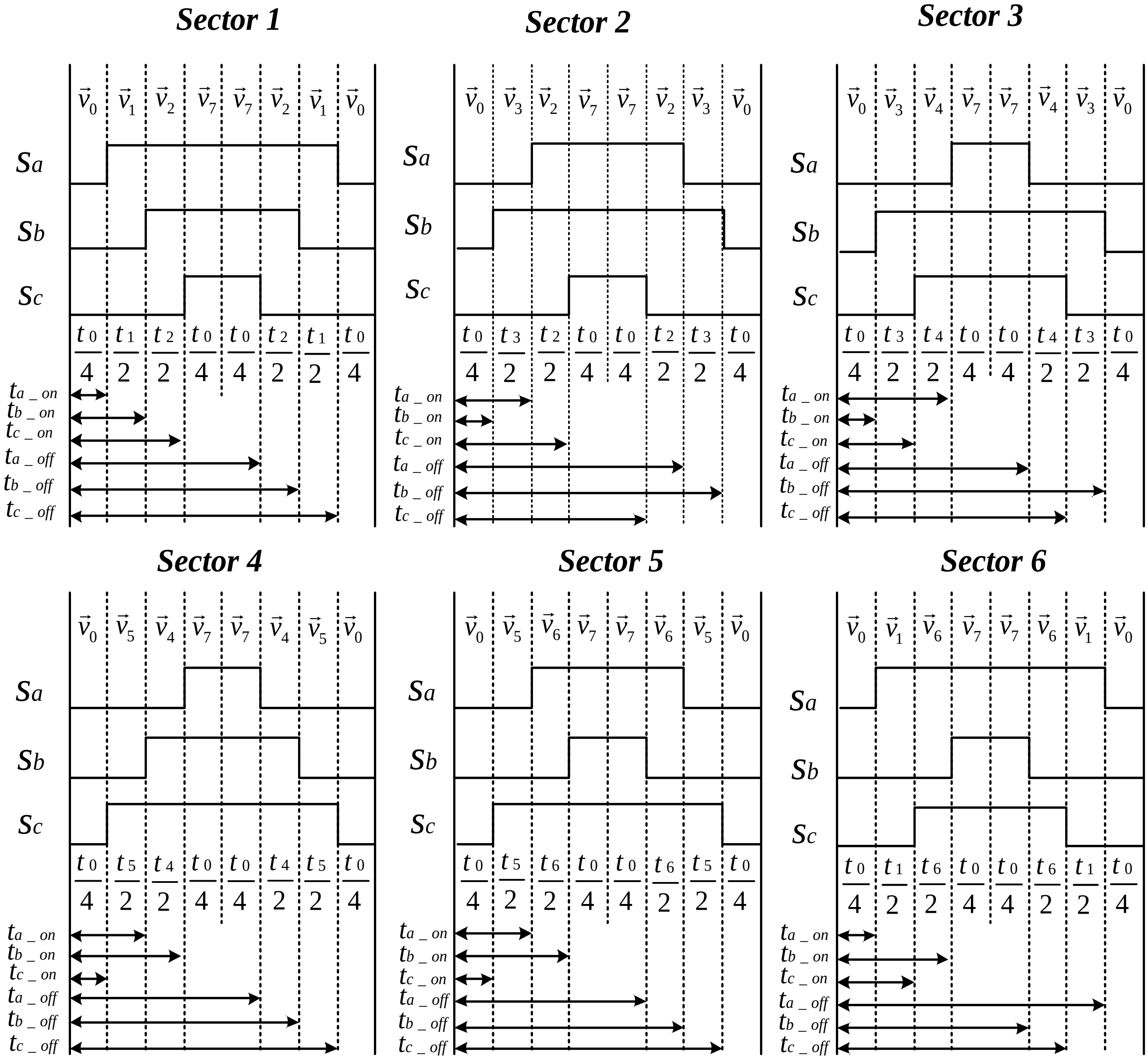
By doing the same calculation, we get the times corresponding to the voltage vectors that make up each sector. These times are summarized in the Table(II.2).

Sector S=1	$t_1 = \dfrac{\sqrt{6}v_{\alpha k} - \sqrt{2}v_{\beta k}}{2v_{dck}} T_h$	$t_2 = \dfrac{\sqrt{2}v_{\alpha k}}{v_{dck}} T_h$	$t_0 = T_h - (t_1 + t_2)$
Sector S=2	$t_2 = \dfrac{\sqrt{6}v_{\alpha k} + \sqrt{2}v_{\beta k}}{2v_{dck}} T_h$	$t_3 = \dfrac{-\sqrt{6}v_{\alpha k} + \sqrt{2}v_{\beta k}}{2v_{dck}} T_h$	$t_0 = T_h - (t_2 + t_3)$
Sector S=3	$t_3 = \dfrac{\sqrt{2}v_{\beta k}}{v_{dck}} T_h$	$t_4 = \dfrac{-\sqrt{6}v_{\alpha k} - \sqrt{2}v_{\beta k}}{2v_{dck}} T_h$	$t_0 = T_h - (t_3 + t_4)$
Sector S=4	$t_4 = \dfrac{-\sqrt{6}v_{\alpha k} + \sqrt{2}v_{\beta k}}{2v_{dck}} T_h$	$t_5 = \dfrac{-\sqrt{2}v_{\beta k}}{v_{dck}} T_h$	$t_0 = T_h - (t_4 + t_5)$
Sector S=5	$t_5 = \dfrac{-\sqrt{6}v_{\alpha k} - \sqrt{2}v_{\beta k}}{2v_{dck}} T_h$	$t_6 = \dfrac{\sqrt{6}v_{\alpha k} - \sqrt{2}v_{\beta k}}{2v_{dck}} T_h$	$t_0 = T_h - (t_5 + t_6)$
Sector S=6	$t_6 = \dfrac{\sqrt{2}v_{\beta k}}{v_{dck}} T_h$	$t_1 = \dfrac{\sqrt{6}v_{\alpha k} + \sqrt{2}v_{\beta k}}{2v_{dck}} T_h$	$t_0 = T_h - (t_6 + t_1)$

Table(II.2): Application times of VSC voltage vectors

Third step: Pulses generation

The vectors to be implemented for different positions of the reference voltage vector are indicated by figure (II.6).



Figure(II.6): Distribution of voltage vectors to be applied for each sector[37].

For sector 1,from Figure (II.6), the ON-time t_{x_on} and OFF-time t_{x_off} of the first switch in each converter leg are expressed as function of time durations by:

$$\begin{cases} t_{a\_on} = \dfrac{t_0}{4} \\ t_{b\_on} = \dfrac{t_0}{4} + \dfrac{t_1}{2} \\ t_{c\_on} = \dfrac{t_0}{4} + \dfrac{t_1}{2} + \dfrac{t_2}{2} \end{cases} \text{and} \begin{cases} t_{a\_off} = \dfrac{3t_0}{4} + t_1 + t_2 \\ t_{b\_off} = \dfrac{3t_0}{4} + \dfrac{t_1}{2} + t_2 \\ t_{c\_off} = \dfrac{3t_0}{4} + \dfrac{t_1}{2} + \dfrac{t_2}{2} \end{cases} \quad \text{(II.41)}$$

In the same manner, the ON and OFF-times of each switch are determined for each sector.

The state of each switching signal is concluded by a simple comparison between time t and the instants t_{x_on}, t_{x_off} according to the following algorithm:

$$\begin{cases} \text{if } t_{a\_on} \le t \le t_{a\_off}, \; S_a = 1; \text{ else, } S_a = 0 \\ \text{if } t_{b\_on} \le t \le t_{b\_off}, \; S_b = 1; \text{ else, } S_b = 0 \\ \text{if } t_{c\_on} \le \text{t} \le t_{c\_off}, \; S_c = 1; \text{ else, } S_c = 0 \end{cases} \quad \text{(II.42)}$$

II.5 Control Methods for VSC-HVDC Systems

II.5.1 General Control Scheme

The aim of the control in all VSC based HVDC systems is the control of transmitted active and reactive powers. Furthermore, the VSC controls are often utilized to provide secondary services, such as improving the dynamics of AC grids. Many control designs are found in the literature for the control of VSC-HVDC. Direct control and vector control schemes, which are based on voltage-controlled VSC and current-controlled VSC designs, respectively are the most broadly adopted techniques[32]-[34]. In voltage-controlled designs, the active and reactive powers are controlled directly by controlling the phase angle and amplitude of the converter output voltage. On the other hand, the current-controlled design uses the converters as a controllable current source, where the injected current vector follows a reference current vector. The current-controlled VSC provides several advantages over the voltage-controlled VSC. The mains advantages signifying[35]: 1) better power quality as the current-controller converter is less influenced by grid harmonics and disturbances, 2) decoupled control of active and reactive powers, 3) inherent protection against over currents, and 4) the control mode can be easily extended to compensate for line harmonics and other power quality issues [40]. The vector control method is broadly adopted in VSC-HVDC and will also be adopted in the following sections.

II.5.2 Vector Oriented Control of VSC-HVDC System

Vector oriented control of VSCs has originally been implemented to variable-speed drives, where the VSC is connected to an AC motor [41],[42]. By using the *dq* decoupling method, the control system is capable to control the torque and flux separately. Once field orientation is achieved the AC motor can be controlled similarly to a separately excited DC motor. Vector current control is commonly regarded as a substantial measure in AC motor control [43].Nevertheless, it is the most adopted control design for VSC based HVDC is vector control. This technique controls the converter voltage to track a current reference injected into the AC network. The vector control design includes the representation of three-phase quantities in the *dq* synchronous reference frame. One of the most beneficial features of vector control is that vectors of AC currents and voltages behave as constant vectors in the steady-state and consequently static errors in the control system can be successfully eliminated by using simple PI controllers.

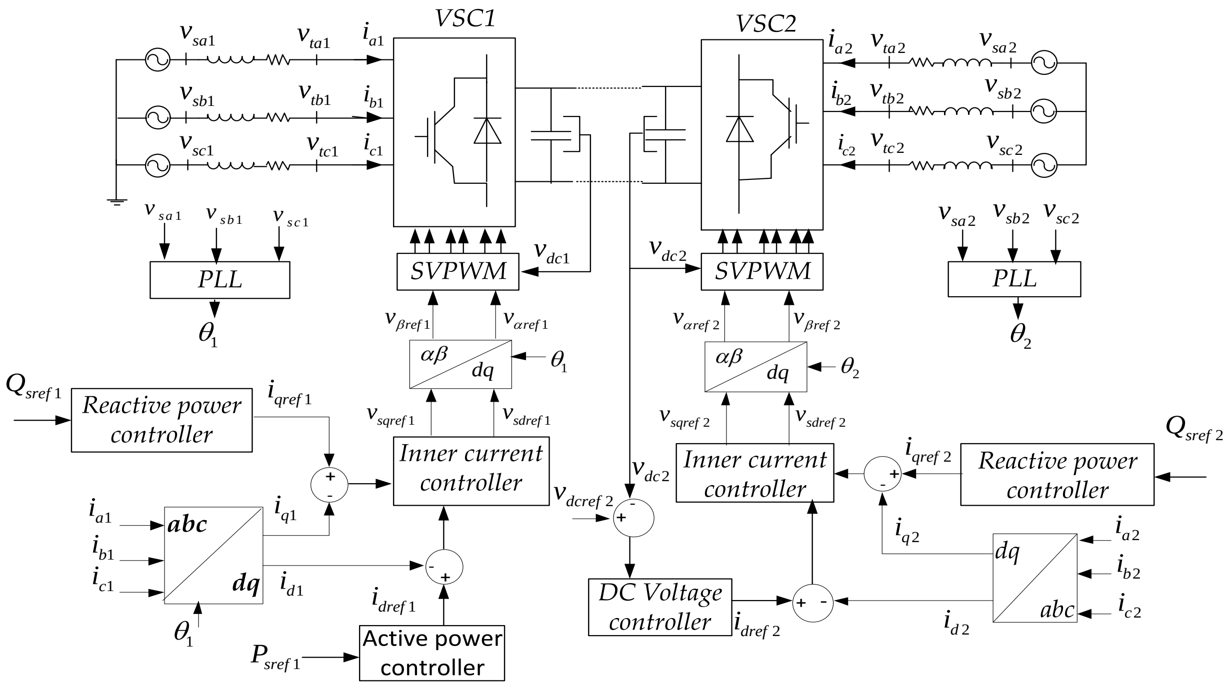


Figure (II.7): Vector oriented control approach of HVDC system.

The primary goal of vector oriented control method is to ensure decoupled control of active and reactive powers. For this, as illustrated in Figure (II.7),the system control is achievable with two control loops in cascade: an outer control loop that provides the current set points and the inner current control loop. The outer controllers cover the direct voltage controller, the active power controller, and the reactive power controller, depending on the application. The reference value for active current can be given by the direct voltage controller or the active power controller, while the reference value for reactive current is produced by the reactive power controller. Under each potential combination of outer controllers, the direct voltage controller is always necessary to ensure an active power balance in the system. Active power taken out of the network must match the active power supplied into the network minus the losses in the DC system, any difference would indicate that the direct voltage in the system will rapidly change to unbearable levels.

Figure (II.7) shows a basic control approach for a VSC-HVDC system where the VSC2 provides the DC side voltage control and power exchange balance among the converter and VSC1 provides active power flow control. The steady-state power flow can be controlled in either direction at VSC1. Consequently, both VSC2 and VSC1 can operate in either rectifier or inverter mode. The general control approach will be made for one VSC and will be used for all the other VSC-HVDC systems during this work. However, several control strategies will be applied depending on the required control of each converter either power flow control or DC voltage control as shown in Figure (II.7).

The dq -reference frame is chosen such that its d-axis is specified to be along with the AC grid voltage. With this alignment; it results:

$$v_{sqk} = 0 \tag{II.43}$$

Using Eq. (II.43), the instantaneous real and reactive powers absorbed from the AC system will be:

$$\begin{aligned} P_{sk} &= v_{dk} i_{dk} \\ Q_{sk} &= -v_{dk} i_{qk} \end{aligned} \tag{II.44}$$

As can be seen, the transformation into rotating dq coordinates system leads to the possibility to control the two current vector components, i_{dk} and i_{qk} independently. Thus, independent control of active and reactive power is possible; see Eq. (II.44), assuming the PLL is performing well.

The inner current controller and the various outer controllers will be explained in detail in the remaining sections of this chapter.

II.5.2.1 Inner Current Controller

The internal current control loop consists of two controllers, for d and q axes currents, respectively and decoupling terms, and feed-forward terms as will be detailed further. And it can be implemented based on the basic relation of the system model like the Figure (II.8) shows.

The system behavior is described by Eq. (II.22), which can be rewritten as:

$$\begin{aligned} v_{sdk} - v_{tdk} &= L_k \frac{di_{dk}}{dt} + R_k i_{dk} - \omega_k L_k i_{qk} \\ v_{sqk} - v_{tqk} &= L_k \frac{di_{qk}}{dt} + R_k i_{qk} + \omega_k L_k i_{dk} \end{aligned} \tag{II.45}$$

Eq. (II.45) designates that the model of the VSC in the synchronous reference frame is a multiple-input multiple-output, strongly coupled nonlinear system. Therefore it will be difficult to realize the exact decoupled control system with general linear control strategies. The transformed voltage equations of each axis have frequency induced term ($\omega_k L i_{dk}$ and $\omega_k L i_{qk}$) that gives a cross-coupling between the two axes. Thus, a close-loop current controller with decoupled current compensation and voltage feed-forward compensation is required to obtain a good control performance [37], as shown in Figure (II.8).

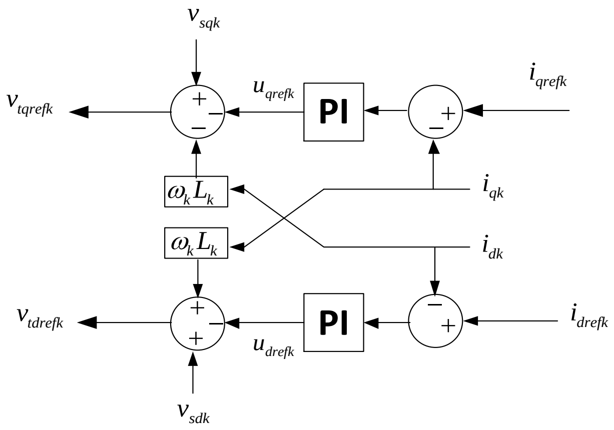


Figure (II.8): Inner Current Controller scheme.

The system inputs should be modified to include components obtained from the converter and feed-forward terms to eliminate the cross-coupling as shown below:

$$\begin{aligned} v_{tdref}(s) &= -u_{drefk}(s) + \omega_k L_k i_{qk} + v_{sdk} \\ v_{tqref}(s) &= -u_{qrefk}(s) - \omega_k L_k i_{dk} + v_{sqk} \end{aligned} \tag{II.46}$$

The PI controller transfer function is given as:

$$R(s) = k_{pi} + \frac{k_{ii}}{s} \tag{II.47}$$

where k_{pi} and k_{ii} are the PI controller gains.

Using Figure (II.8), the PI controller outputs are:

$$u_{dqrefk}(s) = (k_{pi} + \frac{k_{ii}}{s})(i_{dqref}(s) - i_{dqk}(s)) \tag{II.48}$$

By replacing equation (II.48) in equation (II.46) it results:

$$
\begin{aligned}
u_{dkref} &= L_k \frac{di_{dk}}{dt} + R_k i_{dk} \\
u_{qkref} &= L_k \frac{di_{qk}}{dt} + R_k i_{qk}
\end{aligned}
\tag{II.49}
$$

Equation (II.49) shows that the cross coupling terms are cancelled out and independent control in *d* and *q* axes is achieved.

Laplace transforming of Eq. (II.49) is:

$$
u_{dqk}(s) = \frac{1}{L_k s + R_k} i_{dqk}
\tag{II.50}
$$

Figure (II.9) shows the control loop design for each axis after compensating for the cross-coupling terms.

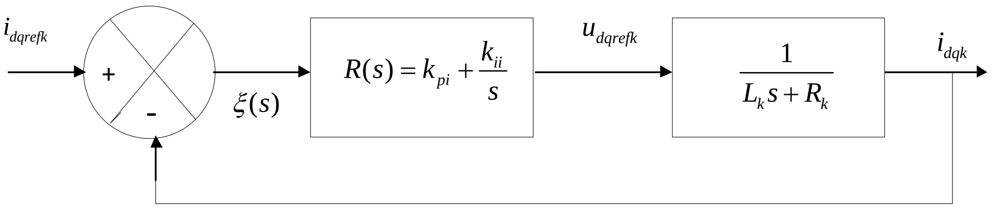


Figure (II.9): Inner current close loop control.

The system closed-loop transfer function as presented in Figure (II.9) is:

$$
H(s) = \frac{\frac{k_{pi}}{L_k} s + \frac{k_{ii}}{L_k}}{s^2 + \frac{(R_k + k_{pi})s + k_i}{L_k}}
\tag{II.51}
$$

By comparing the closed loop transfer function with that of a desired second-order system, it results:

$$
\begin{cases}
k_{pi} = 2\xi_{ik}\omega_{nik}^2 L_k - R_k \\
k_{ii} = L_k \omega_{nik}^2
\end{cases}
\tag{II.52}
$$

where ω_{nik} is the natural frequency, and ξ_{ik} is the damping ratio.

II.5.2.2Outer Controllers

As previously mentioned, the outer controllers consist of DC voltage controller, AC voltage controller, active power controller, and reactive power controller. In the cascaded control system, the outer controllers must be much slower than the inner current controller in order to insure stability [25],[32],[35]. Thus, for the design of the outer controllers, the response of the current control loops may be assumed instantaneous.

II.5.2.2.1Active and Reactive Powers Control

If AC system *d*-axis voltage in Eq. (II.44) is assumed to be constant in steady state, then the active and reactive powers will be proportional to the active and reactive current references, respectively. The simplest approach to control the active and reactive powers consequently will be the open-loop control, as in the following equation:

$$\begin{aligned} i_{drefk} &= \frac{P_{srefk}}{v_{sdk}} \\ i_{qrefk} &= -\frac{Q_{srefk}}{v_{sdk}} \end{aligned} \qquad \text{(II.53)}$$

Further precise control can be accomplished if a feedback-loop is applied, using PI control. In this work, the topology with the open-loop control will be adopted.

II.5.2.2.2DC-Link Voltage Controller

A DC voltage controller is needed for controlling the power exchange between converters employing the averaged model and Eqs. (II.48) and (II.53). The control purpose is to maintain the DC voltage at a given reference value over adjusting the power exchange through i_{dkref} . By controlling the DC voltage, the converter guarantees that the active power available in the DC grid is transferred to the AC grid. So, the converter acts as energy buffer between DC and AC sides, where any unbalance within AC and DC powers leads to a voltage fluctuation across the DC capacitor[44]. Accordingly, the active power reference is calculated through exploring this DC voltage error; thus a general manner to design this control is to operate on the error between the measured DC voltage and its reference via a PI controller. Figure (II.10) describes the control scheme of the DC voltage with a PI controller, in which, the current regulation loop dynamics are neglected. This approximation considerably simplifies the DC-link design procedure without significantly affecting the control accuracy.

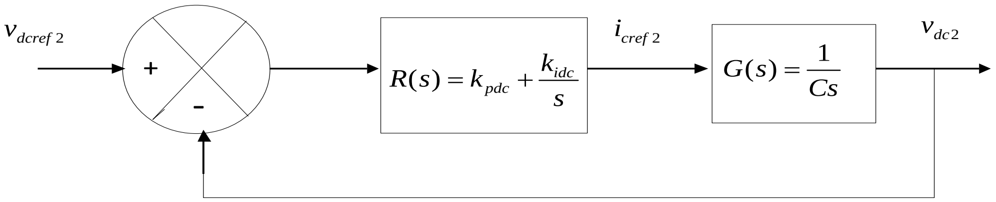


Figure (II.10): DC voltage PI regulation closed-loop

Considering i_{line} as a disturbance signal, the capacitor current i_{c2} can be expressed as:

$$C\frac{dv_{dc2}}{dt} = i_{c2} \tag{II.54}$$

Laplace transform leads to the following transfer function:

$$G(s) = \frac{v_{dc2}}{i_{c2}} = \frac{1}{Cs} \tag{II.55}$$

The PI transfer function is given by:

$$R(s) = k_{pdc} + \frac{k_{idc}}{s} \tag{II.56}$$

where k_{pdc} and k_{idc} denote the PI gains.

The close loop transfer function is:

$$H(s) = \frac{k_{pdc}s + k_{idc}}{Cs^2 + k_{pdc}s + k_{idc}} \tag{II.57}$$

One way to calculate the PI coefficients is to use the pole placement method, in which the closed loop characteristic equation is compared to that of a desired second order system defined by:

$$F(s) = \frac{1}{s^2 + 2\xi_{dc}\omega_{ndc}s + {\omega_{ndc}}^2} \tag{II.58}$$

Through an analogy between the expressions (II.57) and (II.58) we find:

$$\begin{aligned} k_{pdc} &= 2C\xi_{dc}\omega_{ndc} \\ k_{idc} &= C{\omega_{ndc}}^2 \end{aligned} \tag{II.59}$$

The DC side current can be expressed by:

$$i_{dcref\,2} = i_{cref\,2} + i_{line} \tag{II.60}$$

where $i_{cref\,2}$ is the capacitor reference current given by the DC voltage regulator, i_{line} is the measured load current, and $i_{dcref\,2}$ is the direct current reference.

Knowing the DC current reference, the active power reference is calculated as follows (figure (II.11)).

$$P_{dc2ref} = v_{dc2}i_{dcref\,2} \tag{II.61}$$

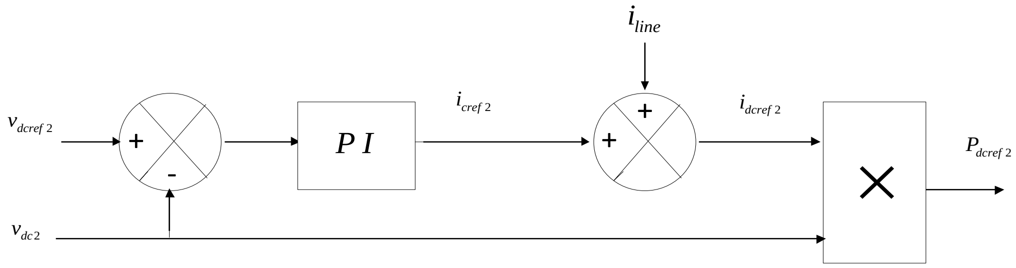


Figure (II.11): Active power reference calculation

Neglecting losses in the converter and phase reactor, and equalizing the power on the AC and DC sides of the converter results in:

$$i_{dref2} = \frac{v_{dc2}}{v_{sd2}} i_{dcref2} \text{ or } i_{dref2} = \frac{P_{dcref2}}{v_{sd2}} \tag{II.62}$$

From equations (II.53), (II.54), (II.60), (II.61) and (II.62), the differential equation for the DC voltage is:

$$C\frac{dv_{dc2}}{dt} = \frac{v_{sd2}}{v_{dc2}} i_{dref2} - i_{line} \tag{II.63}$$

Equation (II.63) indicates that the DC voltage can be controlled by the active current i_{dref2}. Although the i_{line} in equation (II.63) can be represented as a disturbance signal in the DC voltage model, the DC voltage can be controlled without disturbance compensation because the PI controller has the ability to maintain the DC voltage constant without a feed-forward control loop. In this case, the DC voltage controller will be as shown in Figure (II.12).

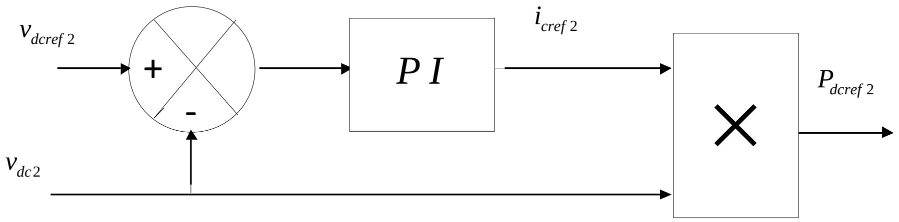


Figure (II.12): Active power reference calculation without compensation.

II.5.2.2.2.1 PI based on Nonlinear Feed-forward Control for DC-Link Voltage Control

Nevertheless, the response of the voltage controller is so slow that the DC output voltage is likely to be exposed to fluctuations. For this raison, line current feed-forward control has been proposed in the literature and proved sufficient for DC line change, but still sensitive to the grid voltage drops[32],[45]. Therefore, in order to improve the DC-link voltage dynamics in the presence of disturbances, a non-linear feed-forward control strategy is proposed based on DC line current and AC input voltage. The active component of reference current consists of two signals, one is the output DC voltage controller, and the other is a nonlinear feed-forward signal calculated from DC line current and AC voltage. The feed-forward signal is made according to the steady-state power balance between the AC and the DC sides.

The converter power balance can be translated in the following equation:

$$P_{s2} = P_{dc2} \tag{II.64}$$

Equation (II.64) can be written as:

$$v_{sd2}i_{d2} + v_{sq2}i_{q2} = v_{dc2}(C\frac{dv_{dc\_2}}{dt} + i_{line}) \tag{II.65}$$

Considering Voltage Oriented Control (VOC), that is $v_{sq2} = 0$, and steady-state operation, equation(II.65) can be simplified as:

$$v_{sd2}i_{d2} = v_{dc2}i_{line} \tag{II.66}$$

Disregarding the dynamic response of currents it becomes:

$$i_{d2} = i_{dref2} \tag{II.67}$$

Presuming $i_{dref2} = K'_f i_{line}$, and using (II.66)[46], it results:

$$v_{sd2}K'_f = v_{dc2} \tag{II.68}$$

Equation(II.68)is a typical line current feed-forward control. It is clear that v_{dc2} is proportional to the grid voltage other than i_{line}. Hence the system has more substantial robustness to change in line but is sensitive to voltage dips. However, considering that

$$i_{dref2} = K''_f \frac{1}{v_{sd}}, \text{ it gives } K''_f = v_{dc2}i_{line} \tag{II.69}$$

Equation (II.69) is the grid voltage feed-forward control where the system has stranger robustness to voltage drops but still sensitive to DC line changes and disturbances.

However, if the two feed-forward terms are nested to combine both voltage and current the i_{dref2} will be:

$$i_{dref2} = K_f \frac{i_{line}}{v_{sd2}} \tag{II.70}$$

Equation (II.70) is employed as a feed-forward signal in this work, which holds information about both, the grid voltage and line, equation (II.66)can be simplified as:

$$K_f = v_{dc} \tag{II.71}$$

Equation (II.70) signifies that the DC output voltage will maintain constant during the grid voltage drops and line fluctuations. Thus the control is simplified to the capacitor where the PI controller is responsible of the charge discharge rate of the DC capacitor, we have:

$$i_{dref2} = K_f \frac{i_{line}}{v_{sd2}} + i_{cref2} \tag{II.72}$$

where i_{cref2} is the output of the PI DC voltage controller.

Using (II.72) as steady state *d*-axis current reference, the block diagram shown in Figure (II.13) illustrates a feed-forward control in the DC voltage controller.

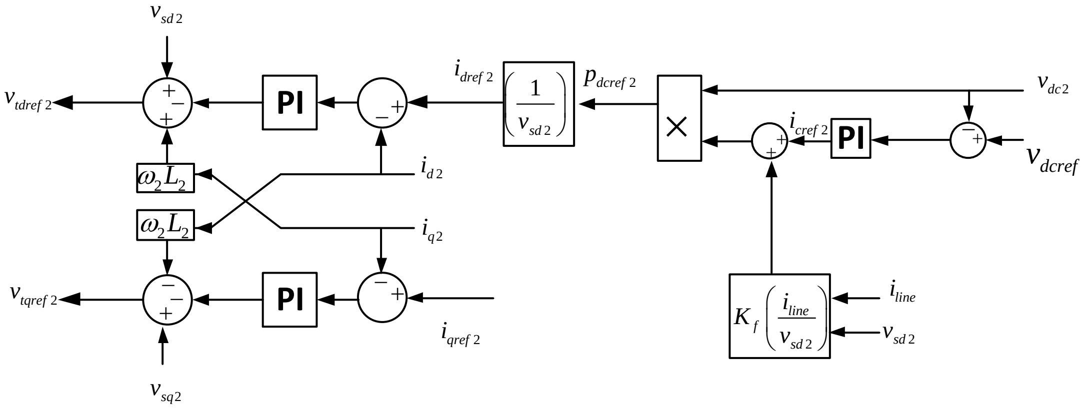


Figure (II.13): Nonlinear feed-forward control scheme

II.5.2.2.2.2PI based on Extended State Observer for DC-Link Voltage Control

To enhance the DC-link voltage dynamics in the presence of disturbances and voltage fluctuations an Extended State Observer (ESO) is employed as a sensor-less based DC-link voltage control strategy. ESO aims to avoid using DC-link voltage sensor unlike the feed-forward method that necessitates extra sensors, which may not be accepted from the reliability and cost points of view. Also, certain variations influence the DC-link voltage controller, and the feed-forward control approach is not able to deal with them efficiently [44].

Extended state observer for the DC-link voltage regulation ensures a zero steady-state tracking error for the DC-link voltage utilizing a simple PI controller also allows fast dynamic response and high robustness upon DC-link voltages variations.

II.5.2.2.2.2.a Extended State Observer Design

The block diagram of the ESO based PI control approach for the three-phase VSC is shown in Figure (II.14). This control arrangement involves a PI voltage loop for controlling the DC-link voltage and an ESO for compensating system disturbances.

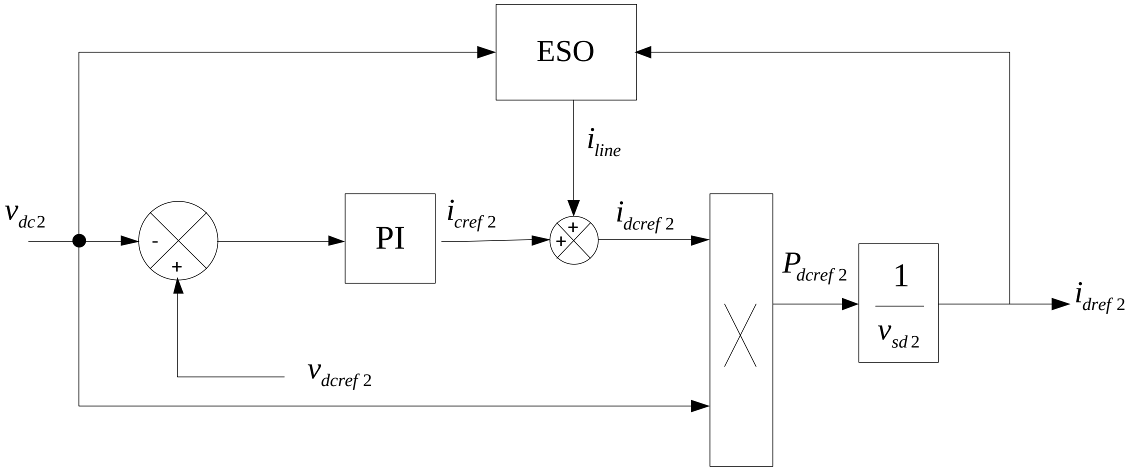


Figure (II.14): Block diagram of ESO based PI control diagram for a three-phase VSC

The power balance across the DC-link is formulated as:

$$\frac{d}{dt}\left(\frac{1}{2}C{v_{dc2}}^2\right)=P_{dc2}-P_{line} \tag{II.73}$$

where $P_{dc2}=v_{dc2}i_{dc2}$ is the power transmitted toward AC-side terminal; if the VSC losses are neglected $P_{dc2}=P_{s2}$ and P_{line} is the power being transmitted to the DC-link. Equation (II.73) can be rewritten as:

$$\frac{d{v_{dc2}}^2}{dt}=\frac{2}{C}(P_{s2}-P_{line}) \tag{II.74}$$

The voltage squared v_{dc2}^2 is regarded as the state variable and denoted as $x_1=v_{dc2}^2$ The term $d(t)=-\frac{2}{C}P_{line}=-\frac{2}{C}v_{dc2}i_{line}$ represents the external disturbance, $d(t)$ is viewed as an extended state variable $x_2=d(t)$. Also considering VOC approach($v_{sq2}=0$) that implies $P_{s2}=v_{sd2}i_{d2}$ where i_{d2} is the system input and is indicated as u. Furthermore, the time derivative of $d(t)$ is indicated as h.

Consequently the system can be written as:

$$\begin{aligned}\dot{x}_1 &= x_2 + bu \\ \dot{x}_2 &= h\end{aligned} \quad \text{where } b=\frac{2}{C}v_{sd2} \tag{II.75}$$

The state-space model is derived as:

$$\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\end{bmatrix}=\begin{bmatrix}0 & 1\\ 0 & 0\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix}+\begin{bmatrix}b\\ 0\end{bmatrix}u+\begin{bmatrix}0\\ 1\end{bmatrix}h \tag{II.76}$$

Based on (II.76), the ESO is constructed as:

$$\begin{bmatrix}\dot{z}_1\\ \dot{z}_2\end{bmatrix}=\begin{bmatrix}0 & 1\\ 0 & 0\end{bmatrix}\begin{bmatrix}z_1\\ z_2\end{bmatrix}+\begin{bmatrix}b\\ 0\end{bmatrix}u+\begin{bmatrix}\beta_1\\ \beta_2\end{bmatrix}\left[x_1-z_1\right] \tag{II.77}$$

where z_1 and z_2 are the estimated value of the x_1 and x_2, $\left[\beta_1 \quad \beta_2\right]^T$ is the gain vector of ESO, which is designed using the pole placement method. The ESO structure is shown in Figure (II.15).

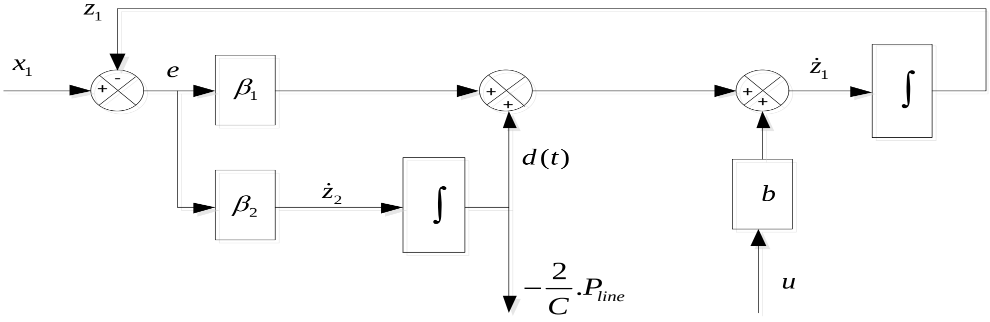


Figure (II.15): Block diagram of the ESO

II.5.2.2.2.2.bParameter Tuning and Stability Analysis

The errors equation can be written as:

$$\begin{aligned}e_1 &= x_1 - z_1 \\ e_2 &= x_2 - z_2\end{aligned} \tag{II.78}$$

By taking the derivative of equation (II.78), it yields:

$$\begin{bmatrix}\dot{e}_1\\ \dot{e}_2\end{bmatrix}=\underbrace{\begin{bmatrix}-\beta_1 & 1\\ -\beta_2 & 0\end{bmatrix}}_{A}\begin{bmatrix}e_1\\ e_2\end{bmatrix}+\begin{bmatrix}0\\ 1\end{bmatrix}h \tag{II.79}$$

The characteristic polynomial of the matrix A is given by:

$$\psi(t) = \lambda^2 + \beta_1\lambda + \beta_2 \tag{II.80}$$

The characteristic polynomial of a desired second order closed loop system is:

$$F(s) = \lambda^2 + 2\xi\omega_n\lambda + \omega_n^{\,2} \tag{II.81}$$

By analogy between (II.80) and (II.81), it results:

$$\begin{aligned} \beta_1 &= 2\,\xi_{eso}\,\omega_{neso} \\ \beta_2 &= \omega_{neso}^{\;\;2} \end{aligned} \tag{II.82}$$

where ξ_{eso} is the desired damping ratio of ESO, and ω_{neso} is the desired bandwidth; the choice of ω_{neso} is an essential factor that influences the system performance. The observer's bandwidth is chosen to be 5-15 times of DC-link voltage controller's bandwidth to ensure that the estimated state dynamics have a fast-tracking performance when the actual state dynamics vary. It is noted that the bandwidth of ESO cannot be selected too large, as a larger bandwidth degrades the system noise immunization. So, selecting the ESO's bandwidth involves a tradeoff between the speed of response and noise protection[44].

II.6 Phase Locked Loop

The grid synchronization is a highly essential and necessary peculiarity of grid side converter control. The synchronization algorithm can detect the phase angle of the grid voltage to synchronize the delivered power. Furthermore, the phase angle plays a significant role in control, being utilized in different transformation modules as Park's transformation. There are several methods capable to detect the phase angle including the zero-crossing detection, the filtering of grid voltages, and the phase-locked-loop (PLL) technique [47]. In this work, the last-named algorithm is adopted to synchronize the delivered power.

The block diagram of the PLL algorithm performed in the synchronous reference frame is presented in Figure (II.16).

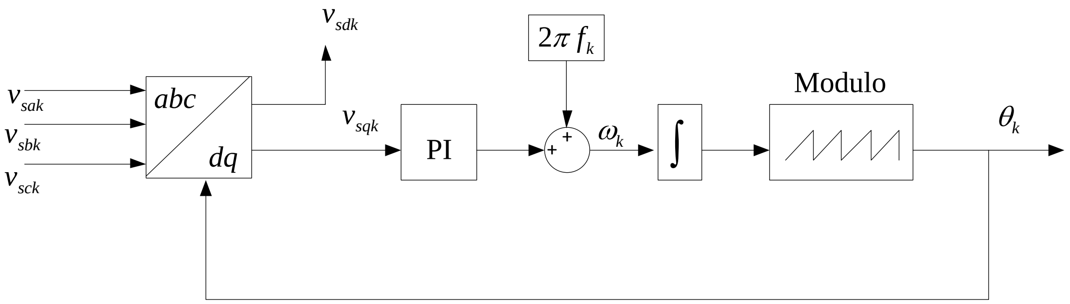


Figure (II.16): Block diagram of PLL

The inputs of the PLL design are the three-phase voltages measured on the grid side and the output is the estimated tracked phase angle. The PLL design is realized in *dq* synchronous reference frame, which signifies that a Park transformation is required. The phase locking of this system is accomplished through controlling the *q*-axis voltage to zero. Commonly, a PI controller is utilized for this objective. By integrating the sum among the PI output and the reference frequency the phase angle is achieved.

The transfer function of the *dq* PLL system is provided by[47]:

$$H_{pll}(s)=\frac{\sqrt{3/2}V_{mk}(k_{ppll}s+k_{ipll})}{s^2+k_{ppll}\sqrt{3/2}V_{mk}s+k_{ipll}\sqrt{3/2}V_{mk}} \tag{II.83}$$

where $\sqrt{3/2}V_{mk}$ is the magnitude of grid voltage and is assumed constant obtained from the Park transformation and the grid frequency $\omega_k = 2\pi f_k$.

Considering that the equation (II.83) is comparable to a second-order transfer function having a zero that is given in the subsequent expression:

$$F(s)=\frac{2\xi_{pll}\omega_{npll}s+\omega_{npll}^2}{s^2+2\xi_{pll}\omega_{npll}s+\omega_{npll}^2} \tag{II.84}$$

By matching (II.84) and (II.83), the controller gains can be obtained. Consequently, the controller parameters a predetermined as function of the damping factor ξ_{pll} and the natural frequency ω_{npll} as follows:

$$k_{ppll}=\frac{2\xi_{pll}\omega_{npll}}{\sqrt{3/2}V_m},\quad k_{ipll}=\frac{\omega_{npll}^2}{\sqrt{3/2}V_m} \tag{II.85}$$

II. 7 Point-to-Point VSC-based HVDC Power Transmission System Simulation

II. 7.1Point-to-Point VSC-based HVDC Structure

The figure (II.17) exhibits a Point-to-Point VSC-HVDC system and its vector oriented control scheme block diagram.

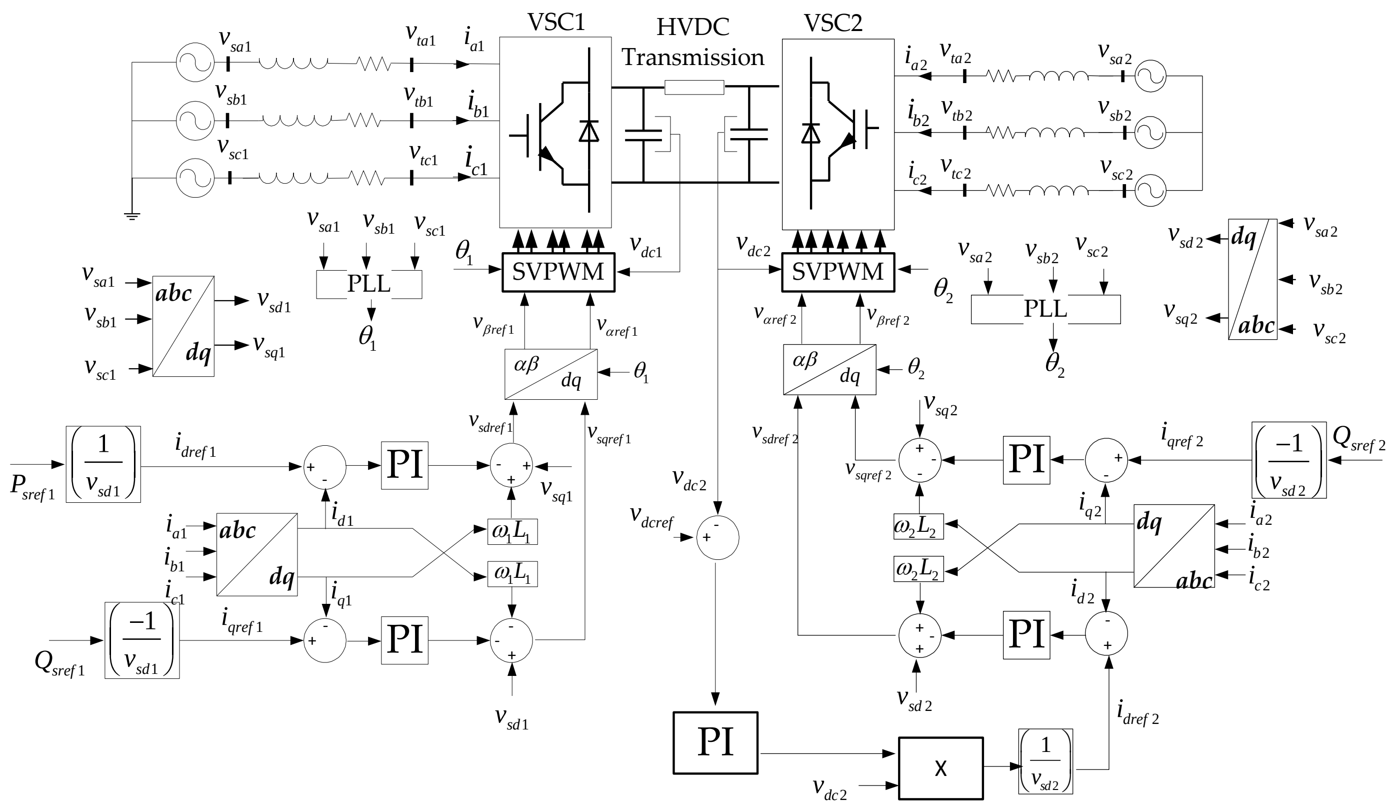


Figure (II.17): Block diagram of the vector oriented control of VSC-based Point-to-Point HVDC system

For the purpose of seeking simplicity the transformer and AC filter in each terminal are not considered and they are replaced by an equivalent sinusoidal three-phase source.

II.7.2 Simulation Results and Discussions

In order to validate the performance of the PI based control of VSC-HVDC transmission system, the system was implemented in Simulink/Matlab environment using the parameters given in Appendix A.

To examine the performance of the designed control system, variations in the active and reactive powers flow are performed at the VSC1 terminal and a shift of the reference value of the DC voltage is also held:

- At t=0.3 s, the controlled output reference signal of the active power is increased from 200 MW to 300 MW.
- At t=0.6 s, the controlled output reference signal of the reactive power for VSC1 is changed from 0 to 50 MVAR.
- At t=0.9 s, the controlled output reference signal of DC-link voltage is increased from 90 kV to 92 kV.
- At t=0.11 s, the controlled output reference signal of the reactive power for VSC2 is changed from 0 MVAR to 50 MVAR.

Figure (II.18) presents the active and reactive powers of both VSC1 and VSC2 AC side terminals as well as their reference values.

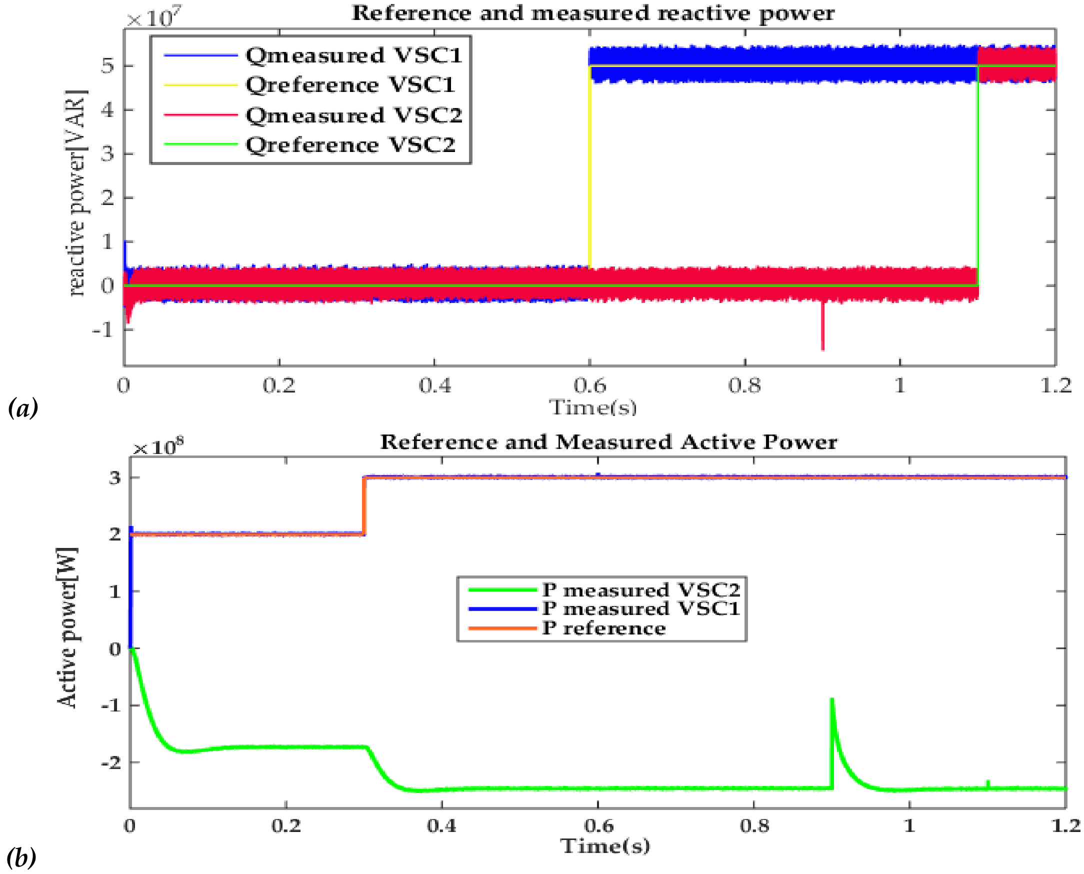


Figure (II.18): Reference and measured powers of VSC1 and VSC2 terminals: (a) reactive powers, (b) active powers

As it can be seen from Figure (II.18), after short transient periods, the measured active and reactive powers follow their references showing fast stabilization without overshoot. At the instant t =0.9s, 110% overshoot in the VSC2 measured active power is noted; this overshoot is due to the change in the DC voltage reference value. Noting that the active and reactive powers are controlled separately and their changes are fully decoupled.

Moreover, the waveforms of the measured active power at each side are nearly equal, as it can be seen in Figure (II.18.b). Indeed, the active power produced by the terminal VSC1 is nearly equivalent in absolute value with that received by terminal VSC2 (AC grid side). However, the contrast of power signs is originating from the fact that one side is regarded as a transmitting terminal and the other one is regarded as a receiving terminal. The small deference between transmitted and received powers values is due to the transmission losses in to the line either on the DC side or the AC sides.

As illustrated in Figure (II.18.a), the measured reactive powers in both terminals follow with precision their references; the stabilization is almost immediate with no transient and overshoots. It is worth noticing that the reactive power reference changes in one terminal do not affect the other terminal. From these results, it can be concluded that the VSC1 and VSC2 control their reactive powers separately.

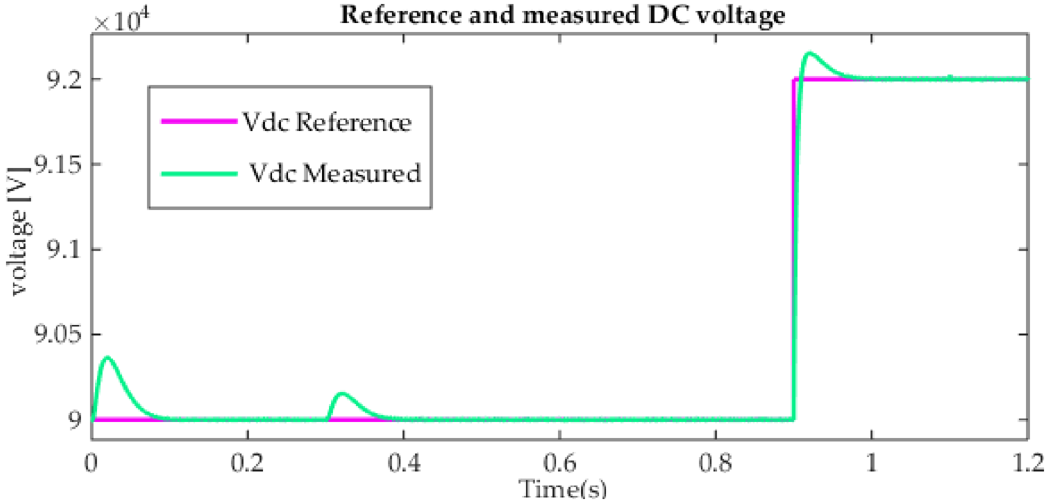
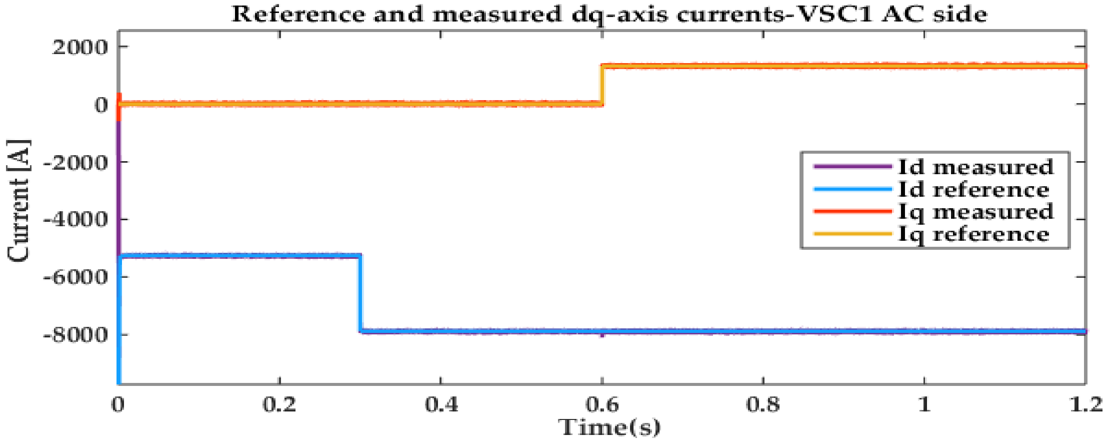
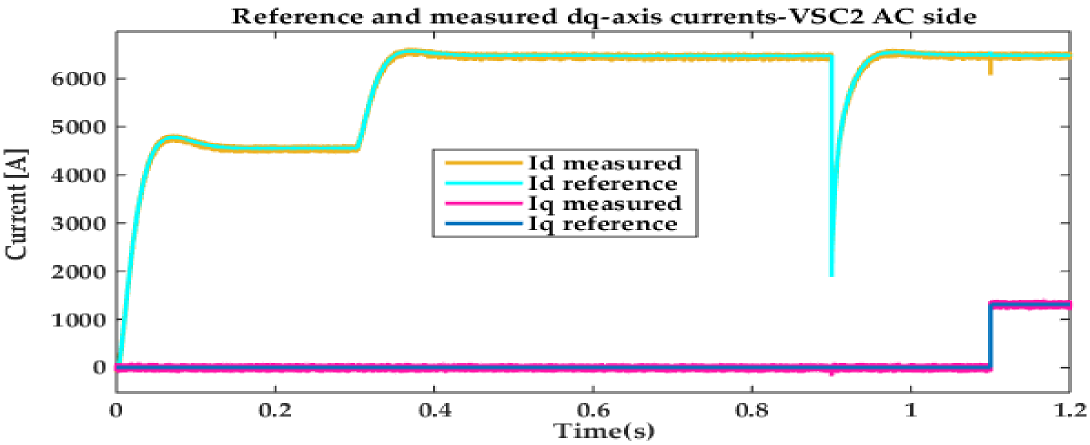


Figure (II.19): Reference and measured DC voltage

From Figure (II.19), it can be noted that the measured DC voltage matches with its reference with an overshoot less than 1% during transients. At the instant t=0.3 s, a transient occurs on the DC voltage due to the increase in active power yet the DC voltage restores its reference value thanks to the PI controller.



(a)



(b)

Figure (II.20): Reference and measured dq-axes currents: (a)VSC1 AC side currents, (b) VSC2 AC side currents.

Due to the fact that the active power is determined by d-axis current, it can be viewed that it is varying proportionally with the active power (see Figure (II.20)). Additionally, since the q-axis current is directly associated with the reactive power; its variations are similar to those in the reactive power flow as illustrated in Figure (II.20). Also, it can be observed from Figure (II.20), the two dq-axes components of both AC sides currents follow quite well their reference signals. However, the DC voltage variation has a negative impact on d-axis current of the terminal VSC1 resulting in an excessive value. Fortunately, the transient ends fast and the signal quickly settles.

The three-phase currents measured at the output of each VSC are given in Figures (II.21)and(II.22).

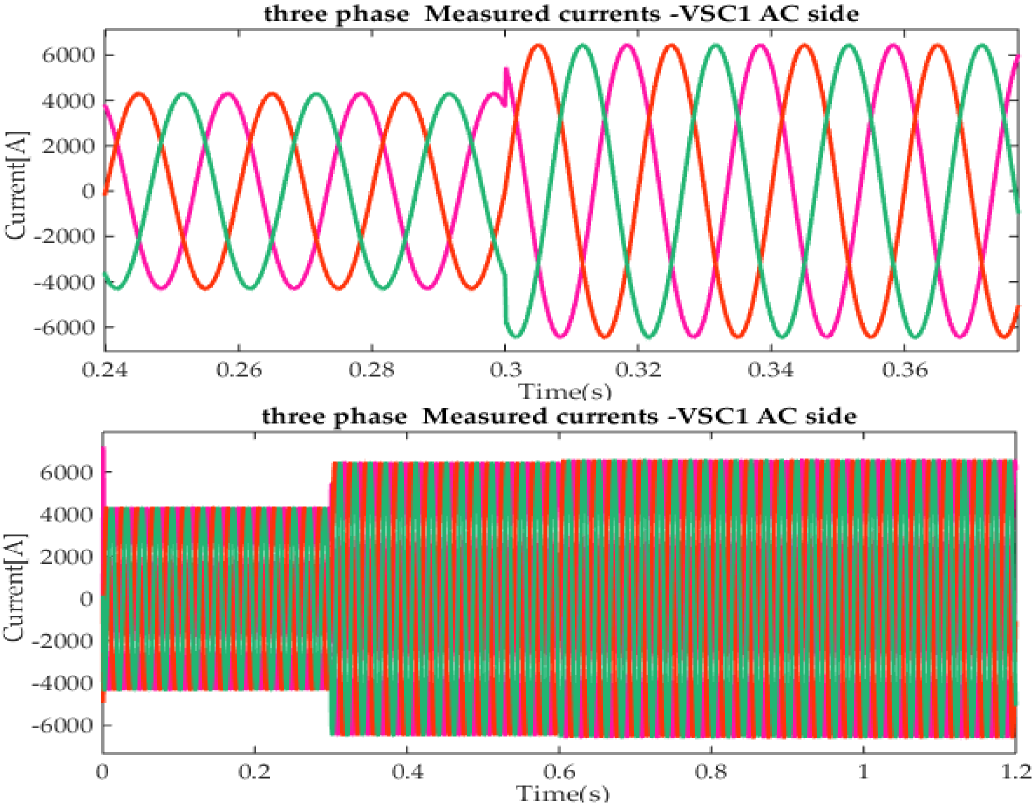


Figure (II.21): VSC1 AC side three phase currents

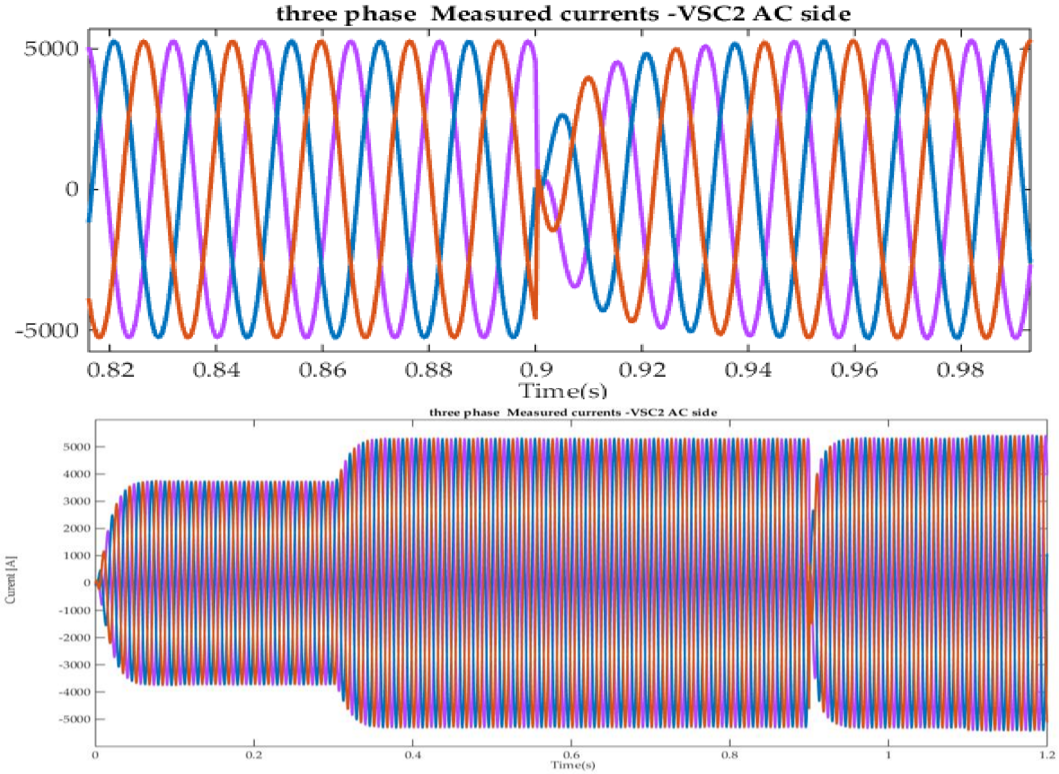


Figure (II.22): VSC2 AC side three phase currents

As it can be observed from Figures (II.21) and (II.22) the waveform of the output current at each AC side of both converters are sinusoidal with different frequencies. Also, it can be noted that the waveforms of the currents at the VSC2 side are disturbed at t=0.9s; the same instant at which the reference DC voltage changed causing the measured value to change thus effecting the injected active power in the VSC AC side currents.

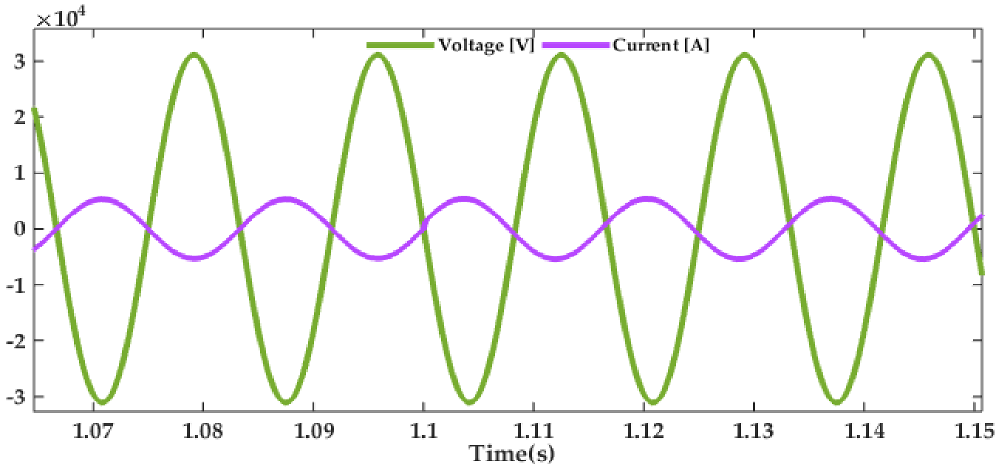
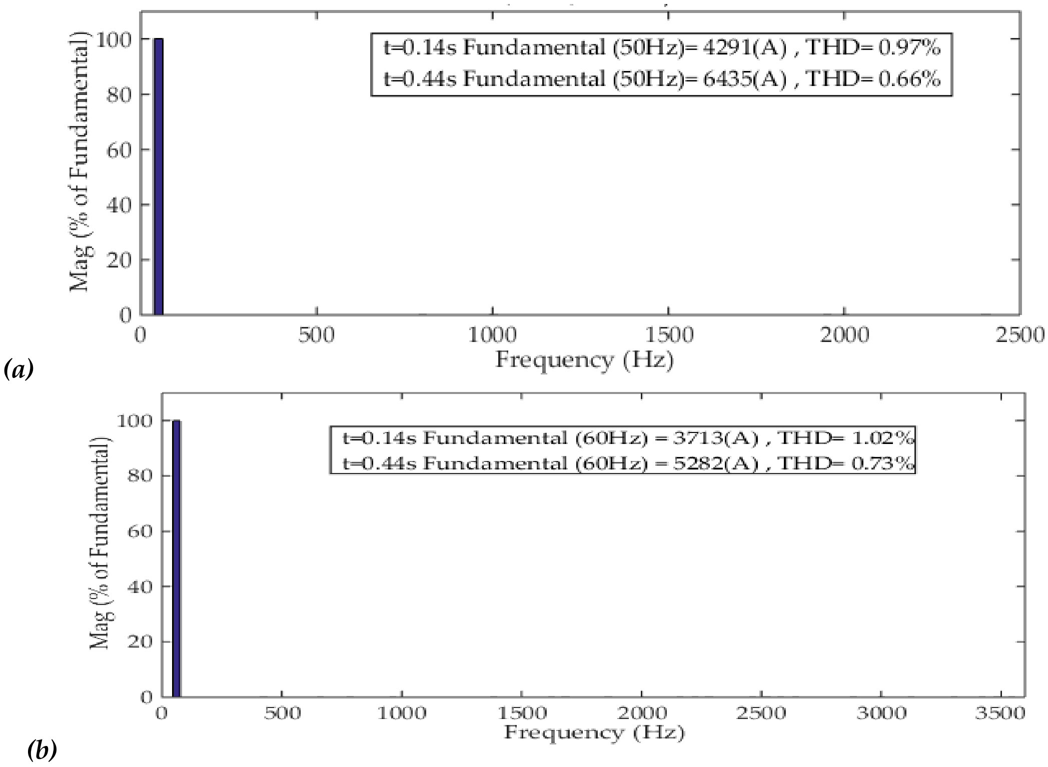


Figure (II.23): VSC2 AC side measured phase voltage and current

As can be seen from Figure (II.23), the waveform of the output phase current and voltage at the VSC2 AC side are in phase hence signifying a unity power factor. until, t=1.1s it can be noted that the waveform of the current is leading compared to the measured voltage, the same instant at which the reactive power injected change reference from 0VAR to 50MVAR.



Figure(II.24):Line current harmonic spectra: (a) VCS1 AC side currents, (b) VCS2 AC side currents

Figure (II.24) shows the line currents harmonic spectra. It is noted that the total harmonic distortion (THD) varies between 1.02% and 0.97% before the variation of the active power reference and 0.73% and 0.66% after its variation for VSC2 and VSC1, respectively. The obtained THD values are less than the 5%,which is in agreement with IEEE 519 standard.

In the followings, the PI based DC voltage control scheme is enhanced by adding: 1) a nonlinear feed-forward or 2) an ESO.

Figure (II.25)shows the response of the VSC2 DC voltage using PI controller with nonlinear feed-forward. As it appears in the plot the control scheme enhanced the performance of the controller against the disturbances. Indeed, at t=0.3s the transient caused by the active power change is reduce to less than 0.1%, due to the feed-forward action that compensated for the error rapidly and effectively mitigating the disturbances. On the other hand, the overshoot generated at t=0.9s by the DC voltage reference change is less than 1%. Not only that, the response is much faster compared to that obtained by traditional PI controller.

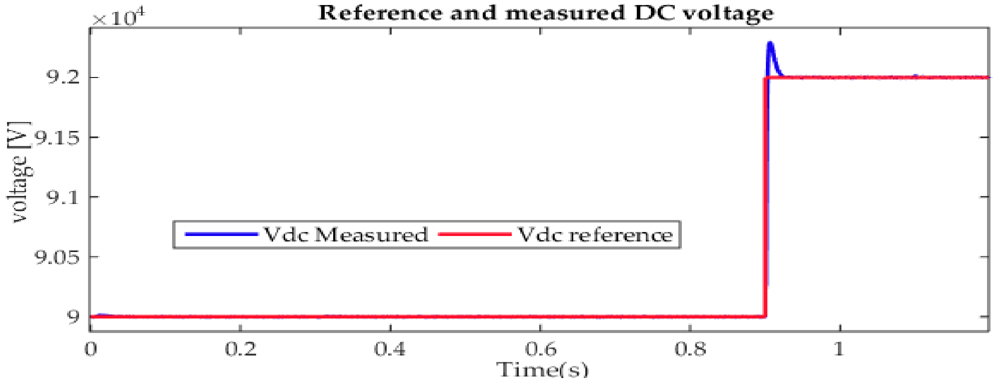


Figure (II.25): Reference and measured DC voltage using feed-forward PI

Moreover, a comparison between Figures (II.24) and (II.19) shows that the disturbances in the measured DC voltage are considerably less during the application of feed-forward compensation. The reason behind that is that any change in P_{dc} is rapidly communicated to P_{sref} and the balance of power is quickly regained.

Figure (II.26) shows that the DC voltage follows its reference value (90 kV) after a very small transient regime. As it can be noted from this plot, the ESO based PI has the ability to reject disturbances as it enhanced the performance of the PI controller at the starting transient. Estimating the total disturbances with quick dynamic response has a positive impact on reducing the transient like that provoked by disturbances happened at t=0.3. Also, the plot shows the dynamic response of the controller during reference value variation at t=0.9s, with an overshoot less than 1% and a very fast settling.

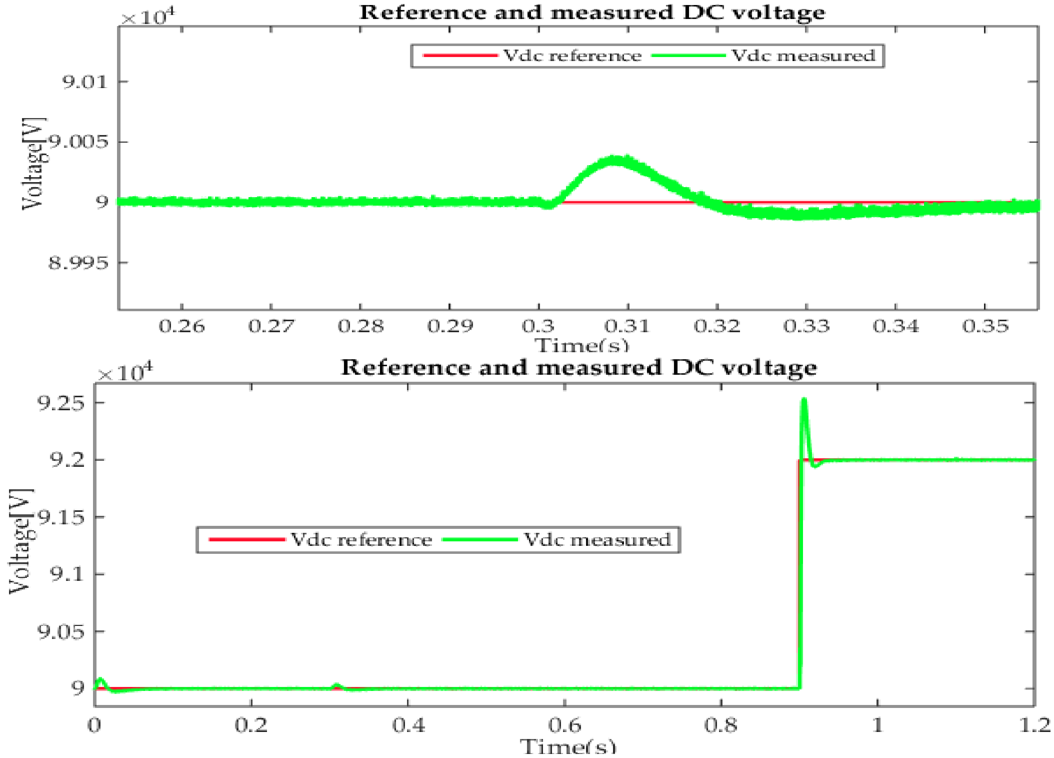


Figure (II.26): Reference and measured DC voltage using ESO based PI

II.8 Back-to-Back VSC-Based HVDC System Simulation

II.8.1Back-to-Back VSC-Based HVDC Structure

Figure (II.27) exhibits a VSC-HVDC system of the back-to-back configuration and its control scheme block diagram. The simulated system is nearly identical to the one utilized in the previously section except the transmission line is not included resulting in two converters connected back to back through a capacitor.

The objective of this section is to analyze the performance of the VSC-based back-to-back HVDC system control when transmitting power between two asynchronous networks, in which the first terminal is operating at 50z and the second one at 60 Hz.

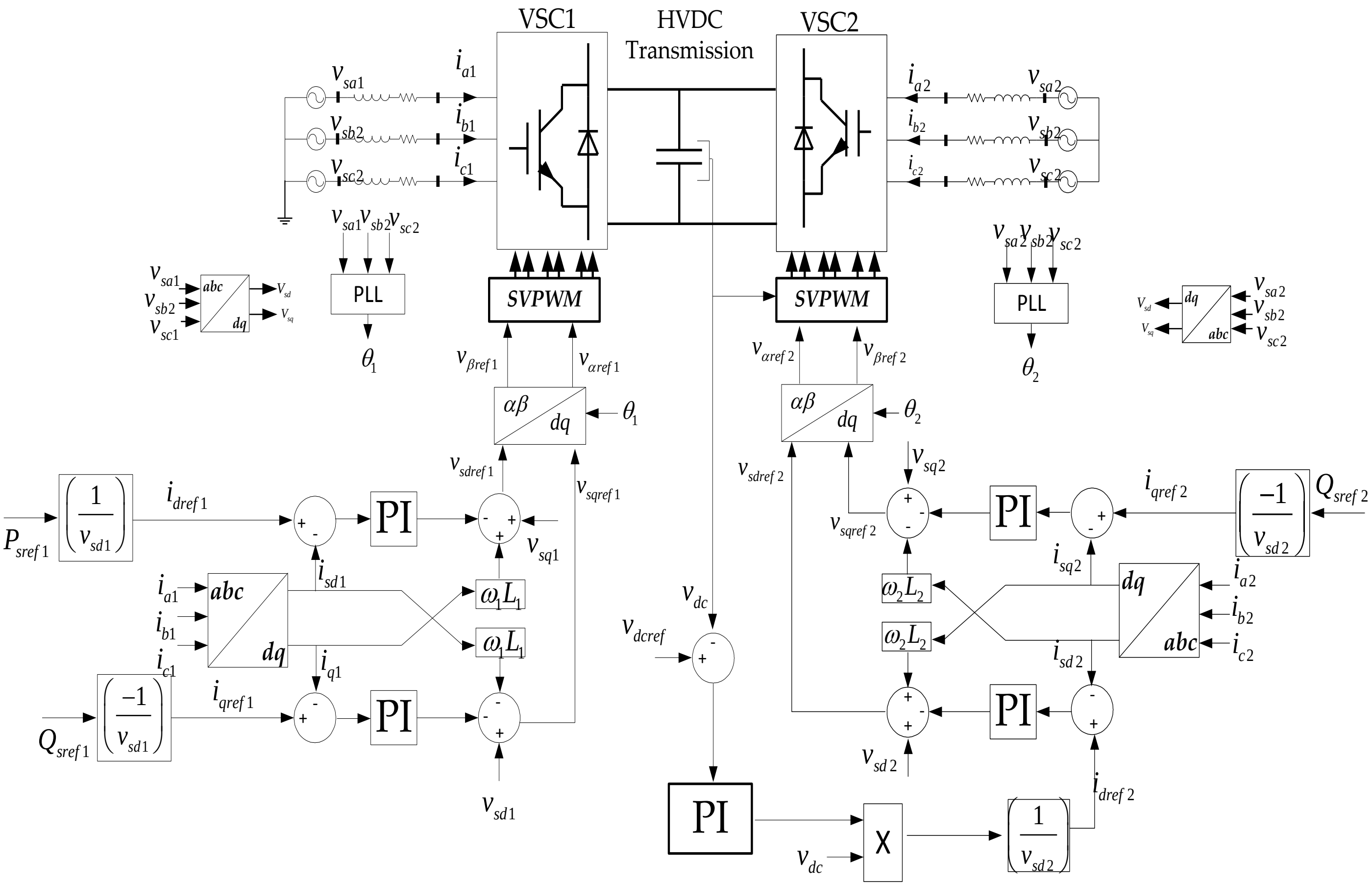
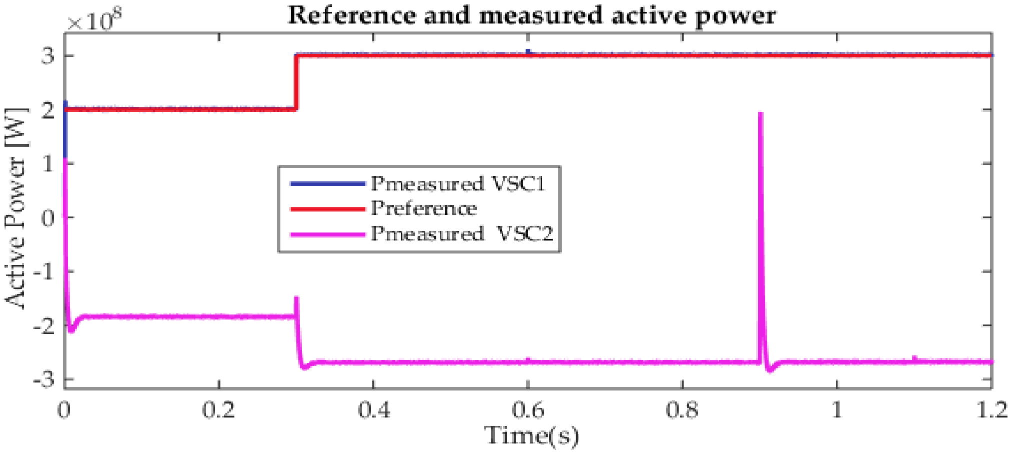


Figure (II.27): Block diagram of the vector oriented control of VSC-based Back-to-Back HVDC system

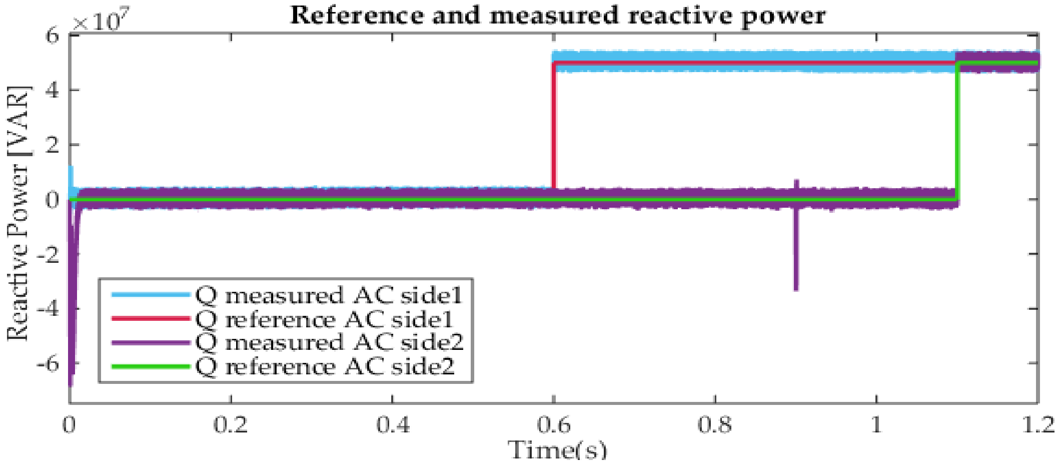
II.8.2 Simulation Results

In order to examine the performance of the designed control system the same tests that adopted in previous section will be also held in the back-to-back configuration.

Figures (II.28.a) and (II.28.b) present the reference and measured active and reactive powers at each AC side of both terminals.



(a)



(b)

Figure (II.28): Reference and measured powers: (a) active powers, (b) reactive powers

According to Figure (II.28),after a relatively slow transient regime on the VSC2 side, the active and reactive powers stabilize at their predetermined reference values. Furthermore, it can be seen that the active and reactive powers spike at t=0.9s for a brief instant of time due to the change in the DC voltage unlike the active and reactive powers of the VSC1 AC side, where they are clean from any transient or overshoot.

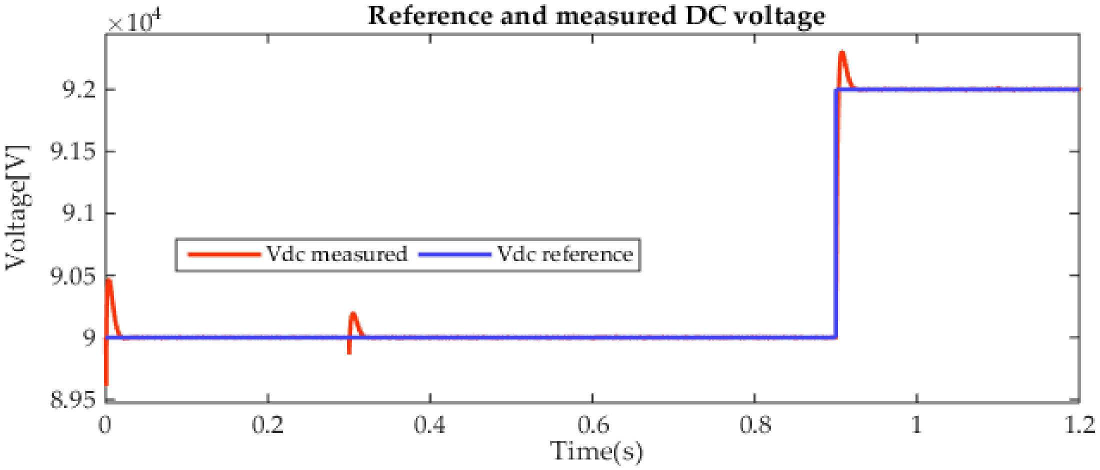
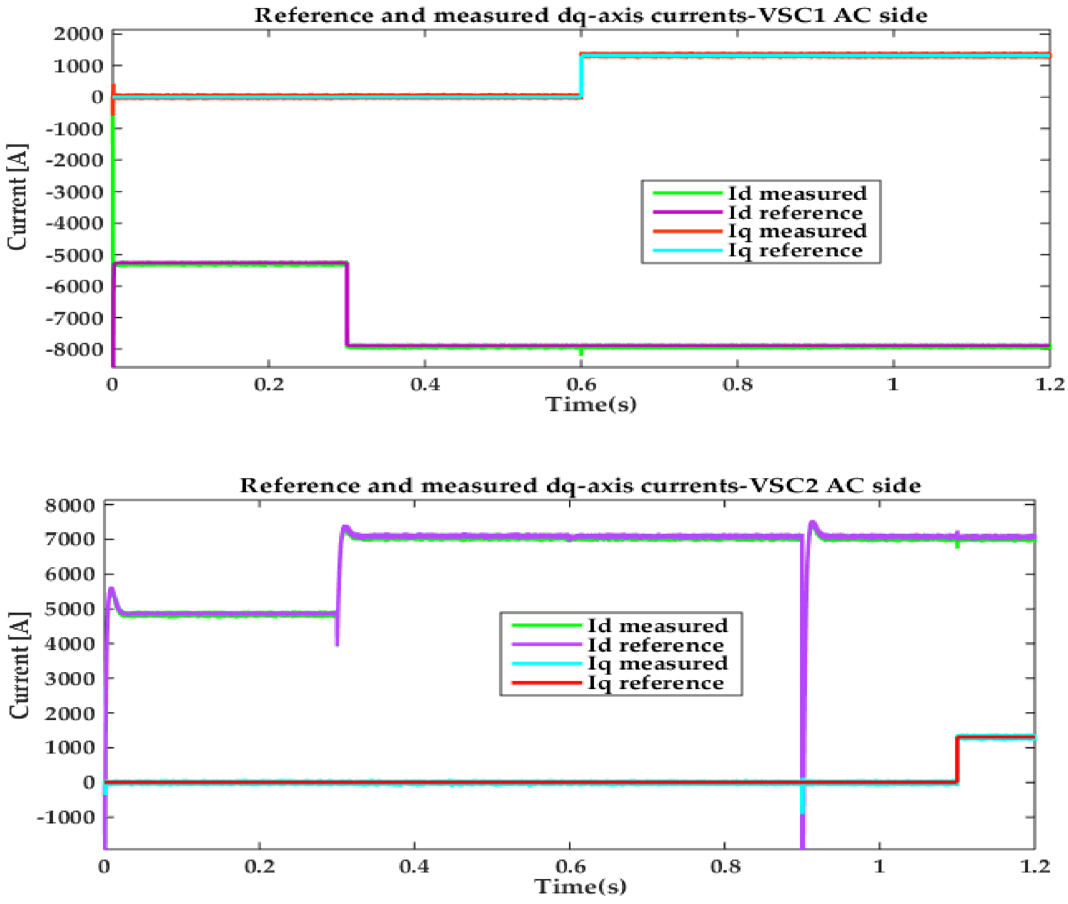


Figure (II.29): DC-bus voltage and its reference

In Figure (II.29), the DC-bus voltage goes through a very short transient regime at the start then it converges again to its set point. The same behavior is observed at t=0.9s when the DC voltage reference changes, the DC voltage tracks it with less than 1% overshoot. At t=0.3s, after an active power change, a quick rise in the DC voltage response can be observe. After this short transient, the voltage curve stabilizes at its set point once more.



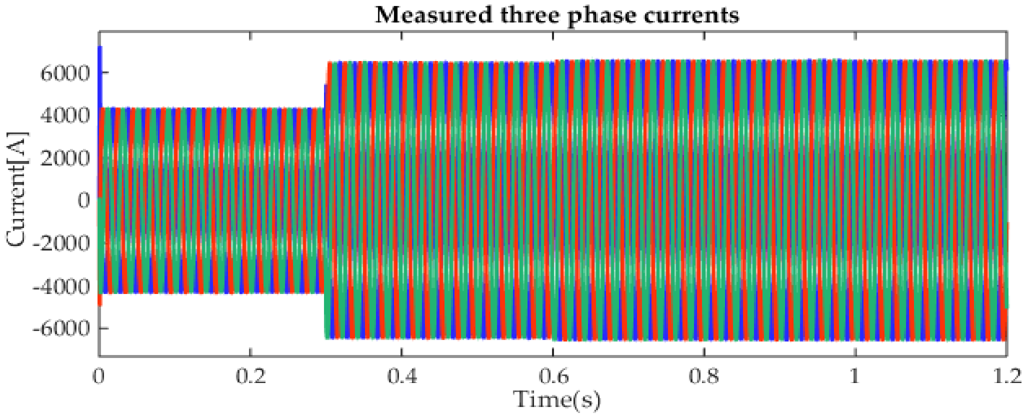
(a)

(b)

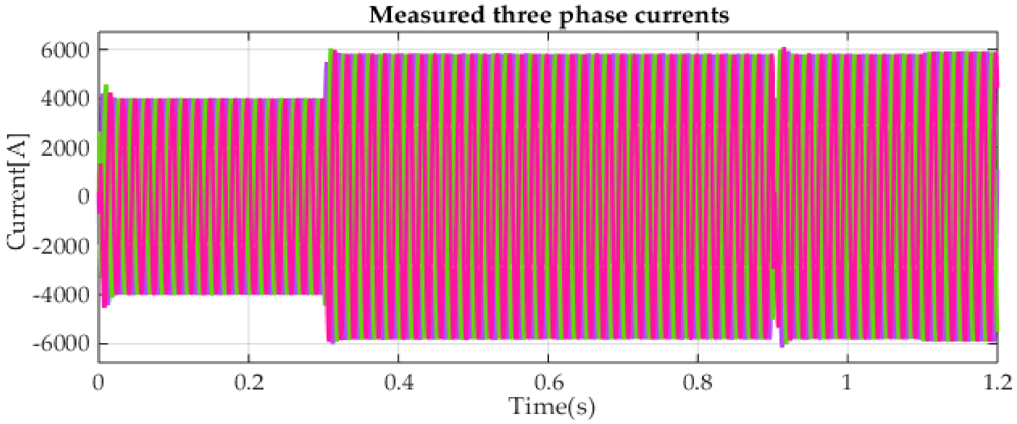
Figure (II.30): Reference and measured dq-axes currents: (a)VSC1 AC side currents, (b)VSC2 AC side currents

Figure (II.30) illustrates the variations of the dq-axes currents as they follow their references values in the steady-state after a relatively quick start transient. It can be noted also at t=0.9s an overshot appears in d-axis current that due to the variation of the DC-bus voltage. Unlike the dq-axes currents in the VSC2 AC side, their counterparts in the VSC1 AC side matched their references almost perfectly with no transients and overshoots.

In Figures (II.31.a) and (II.31.b), the phase currents at the two ends of HVDC system are shown.



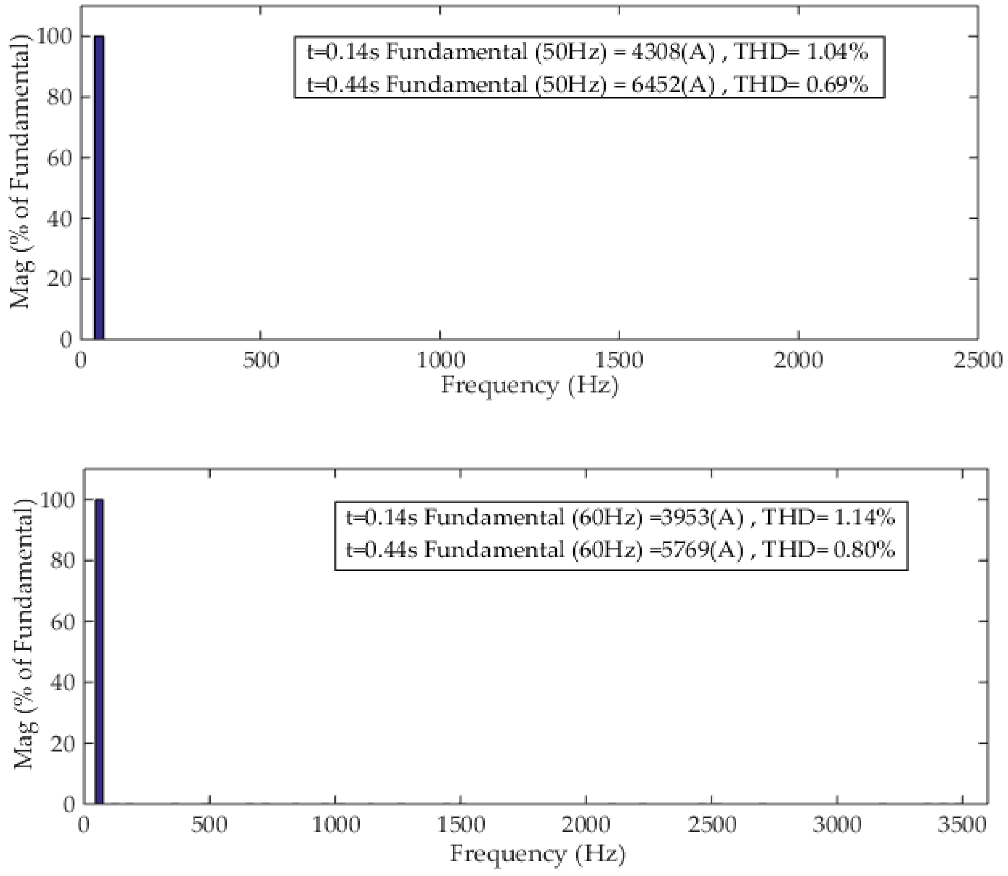
(a)



(b)

Figure (II.31): Three-phase line currents: a)VSC1 AC side, b)VSC2 AC side

Both figures exhibited above show the waveforms of measured currents, at start-up and during the power reference changing, are governed with brief transient regimes. When the steady-state is reached all waves stabilize at their nominal values. By comparing these plots no differences in the currents dynamics can be seen. Accordingly, it can be observed that the synchronization with the grid is well achieved and no irregularities in transferring power between areas working at distinctive frequencies.



(a)

(b)

Figure (II.32):Line currents harmonic spectra: (a)VCS1 side current, (b)VCS2 side current

The currents harmonic spectra given by the figures (II.32) show that the SVM scheme is able of providing sinusoidal current waveforms with low values of total harmonic distortion decreasing from 1.14% and 1.04% to 0.80% and 0.69% for VSC2 and VSC1 line currents, respectively.

Aiming to enhance the performance and robustness of DC-link voltage controller against disturbances, this controller is reinforced by a feed-forward compensator or by an ESO.

Figure (II.33) shows that the performance of the VSC2 DC voltage controlled by PI with nonlinear feed-forward. According to this figure, the ripple of measured DC voltage is high due to direct influence of the chopped i_{line} current. Moreover, the overshoot in start is increased considerably compared to the former control.

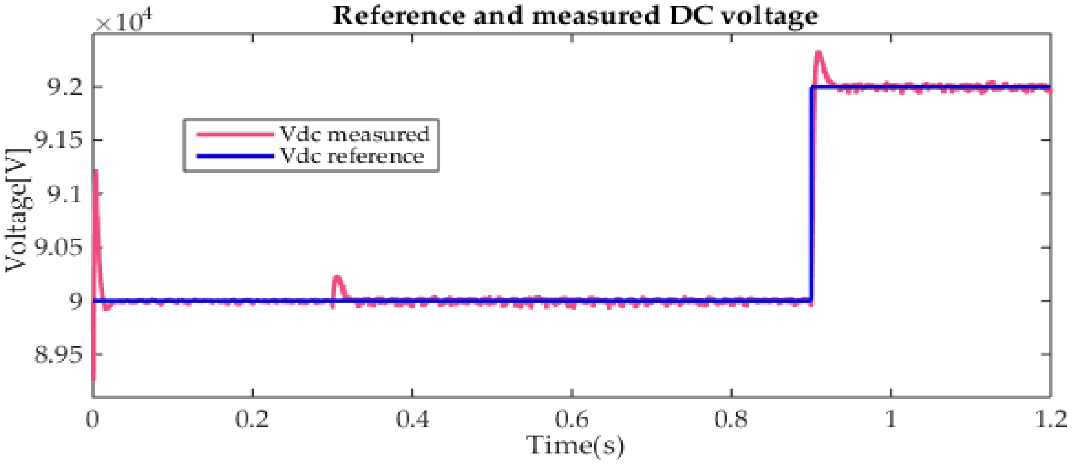
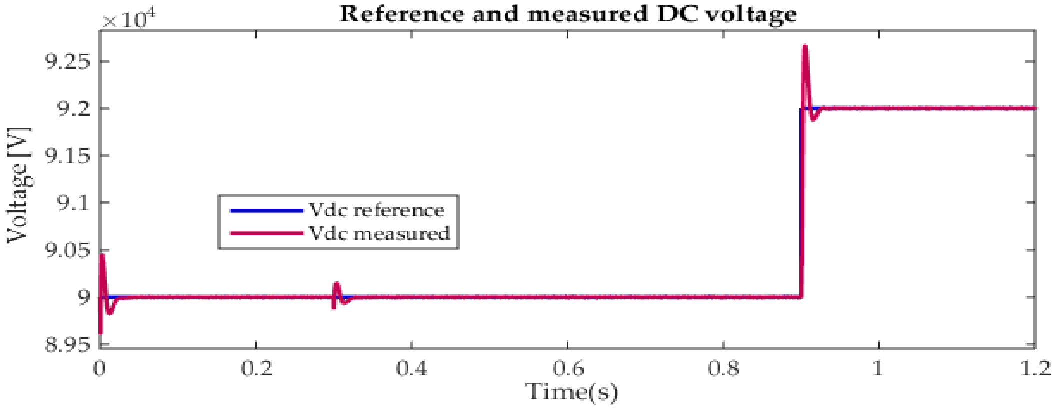


Figure (II.33): DC-link voltage and its reference controlled by nonlinear feed-forward based PI

As it can be observed from Figure (II.34), the DC voltage follows its reference in steady state operation. However, at t=0.3 s, a transient occurs on the DC voltage caused by the increased active power. Thanks to the DC-link controller, the DC voltage stabilizes fast at its set-point as the ESO based PI controller compensates for the error rapidly and effectively estimates the disturbances. At t =0.9s, another transient takes place due to the DC voltage increase resulting in1% overshoot, but the controller intervenes quickly and stabilizes again the DC voltage at its desired reference.



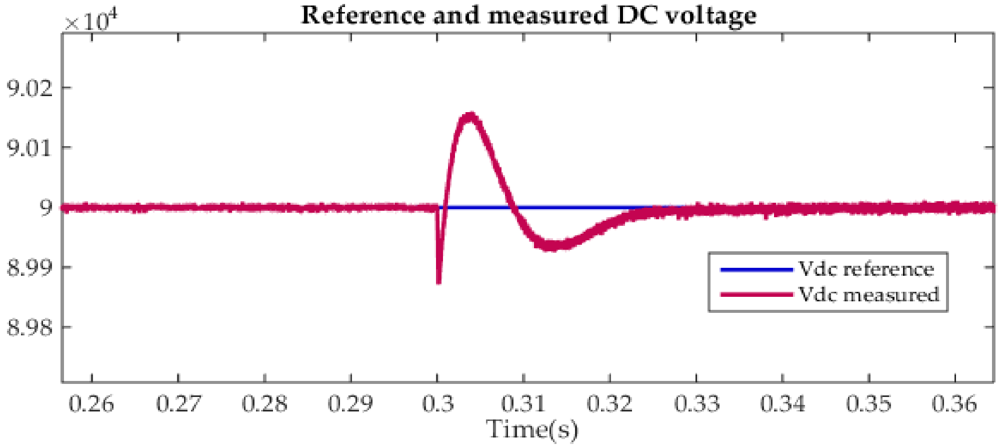


Figure (II.34): DC-link voltage and its reference controlled by ESO-based PI

II.9 Conclusion

In this chapter, a PI based control structure of a VSC-based HVDC system is studied. In its first part, a mathematical model of a VSC based HVDC system is presented. The obtained model is used to develop control strategies suitable for such a system to control the flow of power and regulate the DC-bus voltage. For both the inner current control loop and the outer DC control loops, PI regulators are used. In order to enhance the performance of the DC-link voltage two compensating strategies namely nonlinear feed-forward and extended state observer are adopted. In the second part of this chapter, the behavior of the back-to-back and point-to-point configurations of VSC-based HVDC system are tested and analyzed using the controllers that are designed before. The obtained simulation results show good performances despite some disturbances that the linear controller (PI) cannot face. For this reason, in the next chapter, a nonlinear control will be implemented in order to improve the overall system dynamics even in the presence of disturbances.

Chapter III

Sliding Mode Control of HVDC Systems

III.1 Introduction

Usually, nonlinear control techniques are applied in order to resolve some of conventional control problems such as parametric variations, and ensuring zero static error also guarantying a rapid response, therefore have a stable and robust control system. Among these nonlinear control techniques, sliding mode control (SMC) is known by its simplicity and robustness.

SMC, developed in the early 1950s by *V. Utkin*, has been recognized as an efficient tool for robust controllers design in complex high-order nonlinear dynamic plants operating under various uncertain conditions. SMC, based on the variable structure system control theory, provides means to overcome poor performance or instability problems and to guarantee robustness under parameter uncertainties resulted when PID controllers are used [48, 50]. SMC's major advantage is its low sensitivity to parameter variations and disturbances, which relaxes the necessity of the system's exact modeling [50][14].

In the first part of this chapter, the objective will not to deal in depth with sliding mode control technique, but rather to present a brief reminder on it then to apply it in the control of the VSC based HVDC system with both back-to-back and point-to-point structures. The point is to enhance the control of active and reactive powers as well as the DC voltage by using the merits of first order SMC approach. In the second part of this chapter, a special attention will be given to the control by super twisting algorithm. For this, a theoretical brief on the super twisting algorithm will be given, and eventually; this control will be applied to the aforementioned VSC-HVDC systems by replacing the classic SMC controllers by super twisting algorithm controllers.

III.2 First Order Sliding Mode Control

The sliding mode control technique is a particular mode of operation with variable structure systems. A system with a variable structure is a system that can change its structure by switching its control between two states, according to a switching logic well specified as illustrated in the figure (III.1).

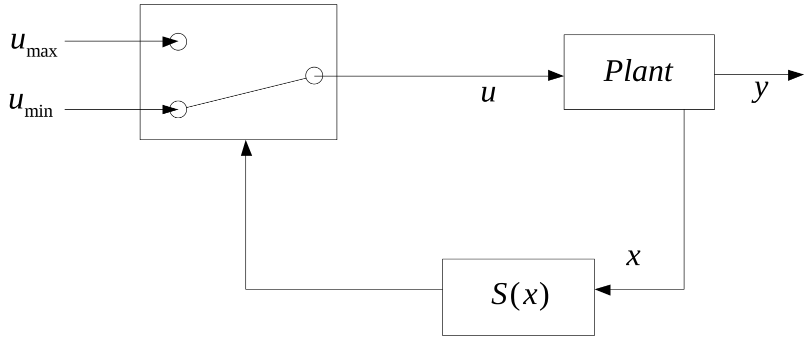


Figure (III.1): Variable structure regulation system with a change of structure by switching

The switching between two values is defined by the following law:

$$u = \begin{cases} u_{min} & \text{for } S(x) > 0 \\ u_{max} & \text{for } S(x) < 0 \end{cases} \tag{III.1}$$

For systems with variable structure, the satisfactory choice of the parameters of each structure, and a good definition of the switching logic is necessary. Under certain conditions, switching can be done at a very high frequency, the system is then in sliding mode. The dynamic behavior of the system is defined by $S(x)=0$, $S(x)$ being the sliding surface, the objective is to bring the state trajectory of the system towards this surface and to maintain the sliding regime until the point of equilibrium [48-50] [16].The significant advantage of the variable-structure control in sliding mode is the robustness against changes in parameters or disturbances [16]. The ease of implementation and simplicity are other advantages of sliding mode control. These advantages make the application of this control very interesting and perfectly suitable for the grid connected Voltage Source Converter. However, the oscillation phenomenon called "chattering" associated with sliding mode control has a major drawback because it can excite the dynamics of high-frequency switching which makes it undesirable because it often causes control inaccuracy and high heat loss in electric circuitry[49][14].

The designing of the control law in sliding mode consists, first of all, is the choice the manifold in the state space which allows the convergence of the trajectory of the state variables of the system towards the desired point of equilibrium, then to establish the condition of existence of sliding mode which is linked to the convergence of the state trajectory, and to determine the control laws, which has the role of maintaining the sliding conditions (attractiveness), in other words, the conception of the law of control by sliding mode is carried out in three steps[16][14]:

Step 1: Choice of sliding surface.
Step 2: Development of the convergence condition.
Step 3: Determination of the control law.

III.2.1 Choice of Sliding Surface

For a system defined by equation (III.2), the vector of the surface $S(x)$ has the same dimension as the command vector u.

$$\frac{dx}{dt} = f(x) + B(x)u \tag{III.2}$$

The sliding surface is a scalar function such that the variable to be adjusted slides on this surface and tends towards the origin of the phase plane [48, 53][[16]. A general form proposed by *J.J. Slotine* that ensure the convergence of the variable to settle towards its reference is given by [51]:

$$S(x) = \left(\frac{d}{dt} + \lambda\right)^{r-1} e(x) \tag{III.3}$$

$e(x)$:Represents the difference between the variable to be regulated and its reference.
λ : is a positive constant.
r : is the relative degree of variable; it represents the number of times one takes to differentiate the output to bring up the control.
The objective of the control is to keep the surface at zero. The sliding surface can be viewed as a linear differential equation, of which the only solution is $e(x) = 0$. For a suitable choice of the controller gains, this returns to a problem of tracking the trajectory, which is equivalent to an exact linearization of the difference while respecting the condition of convergence [51-53].

III.2.2 Conditions of Existence and Convergence

The condition of convergence or attractiveness allows the dynamics of the system to converge towards the sliding surface; it is a question of formulating a scalar function of *Lyapunov* $V(x) > 0$ for the state variables of the system. The control law must decrease this function. The solution is to choose a scalar function $S(x)$ to guarantee the attraction of the variable to be controlled towards its reference value and to design a command such that the square of the sliding surface corresponds to a *Lyapunov* function.
Lyapunov's function is defined as follows:

$$V(x) = \frac{1}{2} S^2(x) \tag{III.4}$$

The derivative of this function is:

$$\dot{V}(x) = S(x)\dot{S}(x) \tag{III.5}$$

In order to force the function $V(x)$ to decrease, it is sufficient to ensure that its derivative is negative. Equation (II.4) explains that the square of the distance between a given point of the phase plane and the sliding surface expressed by $S^2(x)$ decreases all the time provided that the derivative of the *Lyapunov* function always remains negative, forcing the path of the system to move towards the surface from its both sides. This condition assumes an ideal sliding regime where the switching frequency is infinite[52].

III.2.3 Determination of the Sliding Mode Control Law

Obtaining a sliding regime requires a discontinuous control. If this discontinuous control is essential, it does not prevent a continuous part from being added to it [16]. In the presence of a disturbance, the purpose of the discontinuous control is to verify the attractiveness conditions. The controller structure by sliding mode consists of two parts, one concerning the exact linearization (u_{eq}), and the other stabilizing (u_{sw}), it is given by:

$$u = u_{eq} + u_{sw} \tag{III.6}$$

The equivalent command proposed by *Filipov* and *Utkin* [16], is used to maintain the variable to be controlled on the sliding surface $S(x)=0$. The discontinuous control is used to drive this variable towards its reference if it is not on the sliding surface [53][12]. It is then determined to verify the convergence condition.

III.2.3.1 Equivalent Control

Consider the previous system (II.2), an equivalent control vector can be developed by setting the derivative as a function of time of the switching function equal to zero:

$$\dot{S}(x,t) = \left(\frac{\partial S}{\partial x}\right)(f(x,t) + B(x,t)u) + \frac{\partial S}{\partial t} = 0 \tag{III.7}$$

Hence, we can find the equivalent command defined by:

$$u_{eq} = -\left[\left(\frac{\partial S}{\partial x}\right)^t B(x,t)\right]^{-1} \left\{\left(\frac{\partial S}{\partial x}\right)^t f(x,t) + \frac{\partial S}{\partial t}\right\} \tag{III.8}$$

With the condition of existence:

$$\left(\frac{\partial S}{\partial x}\right)^t B(x,t) \neq 0 \tag{III.9}$$

III.2.3.1 Discontinuous Control

In the case where the state trajectories are not on the sliding surface $S(x)=0$, due to disturbances or changes in system parameters, a control capable of bringing these trajectories towards its references is necessary. A discontinuous function (two-level switch) can be used to fulfill this requirement, this control is defined by:

$$u_{sw} = -k\,\mathrm{sgn}(\mathrm{S}(x)) \qquad \text{with } k > 0 \tag{III.10}$$

with:

$$\operatorname{sgn}(S(x)) = \begin{cases} 1 & S(x) > 0 \\ -1 & S(x) < 0 \\ 0 & S(x) = 0 \end{cases} \tag{III.11}$$

III.2.4 Integral Slide Mode Control

In this approach, the sliding surface can be improved by inserting an integral action in its expression, this surface is then defined by [16]:

$$S(t) = \left(\lambda + \frac{d}{dt}\right)^{r-1} e(x) + k_i \int e(t)dt \tag{III.11}$$

where k_i is a positive integral gain.

The advantage of this approach is that the sliding surface in this case is a plane passing through the origin. In the case where the system is second order, $r = 2$, the solution is obtained in a plane, while the solution is obtained on a line in the classic sliding mode[16][12][54].

III.3 Sliding Mode Control of a VSC Based HVDC Systems

After having presented a brief introduction to the sliding mode control, in the following sections, we will apply this technique to control the VSC based HVDC systems. Both configurations namely back-to-back and point-to-point are considered. The control of the before mentioned system must allow DC-bus voltage as well as active and reactive powers regulation.

III.3.1 Controllers Design

The overall model of the VSC-HVDC system in the synchronous reference frame (*dq*) is given by:

$$\begin{cases} \dfrac{di_{dk}}{dt} = \dfrac{-R_k}{L_k} i_{dk} + \omega_k i_{qk} - \dfrac{v_{tdk}}{L_k} + \dfrac{v_{sdk}}{L_k} \\ \dfrac{di_{qk}}{dt} = \dfrac{-R_k}{L_k} i_{qk} - \omega_k i_{dk} - \dfrac{v_{tqk}}{L_k} + \dfrac{v_{sqk}}{L_k} \\ \dfrac{dv_{dck}}{dt} = \dfrac{v_{sdk} i_{d2}}{C v_{dck}} - \dfrac{i_{line}}{C} \end{cases} \tag{III.12}$$

To apply the sliding mode control on the VSC-HDVC system, the system (III.12) should be subdivided into two subsystems as follows:

Subsystem 1

The first subsystem is characterized by the state vector $x = \begin{bmatrix} i_{dk} & i_{qk} \end{bmatrix}^T$, and the control vector $u = \begin{bmatrix} v_{tdrefk} & v_{tqrefk} \end{bmatrix}^T$, and it is defined by:

$$\begin{cases} \dfrac{di_{dk}}{dt} = \dfrac{-R_k}{L_k} i_{dk} + \omega_k i_{qk} - \dfrac{v_{tdk}}{L_k} + \dfrac{v_{sdk}}{L_k} \\ \dfrac{di_{qk}}{dt} = \dfrac{-R_k}{L_k} i_{qk} - \omega_k i_{dk} - \dfrac{v_{tqk}}{L_k} + \dfrac{v_{sqk}}{L_k} \end{cases} \tag{III.13}$$

Subsystem **2**

The second subsystem is a first order, and it is characterized by the state vector $x = v_{dc}$,and the control vector $u = i_{drefk}$ .It is governed by:

$$\frac{dv_{dck}}{dt} = \frac{v_{sdk} i_{d2}}{C v_{dck}} - \frac{i_{line}}{C} \tag{III.14}$$

After dividing overall system in two subsystems, the design of powers and DC-bus voltage controllers requires to apply to each of these sub-models the sliding mode control.

III.3.1.1 Current Controller Design

From the model of the first subsystem, we define the following two surfaces:

The first surface is that of the active component of the line current i_{idk} defined by:

$$S_{1k} = i_{idk} - i_{idrefk} + k_{ik} \int \left(i_{idk} - i_{idrefk} \right) dt \tag{III.15}$$

The second surface is that of the reactive component of the alternating current i_{qk} defined by:

$$S_{2k} = i_{qk} - i_{qrefk} + k_{ik} \int \left(i_{iqk} - i_{iqrefk} \right) dt \tag{III.16}$$

Equivalent Control Design:

During the sliding mode, we have:

$$\begin{aligned} S_{1k} &= \dot{S}_{1k} = 0 \\ S_{2k} &= \dot{S}_{2k} = 0 \end{aligned} \tag{III.17}$$

Using the two equations of the first subsystem, the two sliding surfaces derivatives take the following form:

$$\begin{aligned} \dot{S}_{1k} &= f_{1k}(x) + g_{1k} u_{eqdk} - i_{drefk} + k_{ik} \left(i_{idk} - i_{idrefk} \right) = 0 \\ \dot{S}_{2k} &= f_{2k}(x) + g_{2k} u_{edqk} - i_{qrefk} + k_{ik} \left(i_{iqk} - i_{iqrefk} \right) = 0 \end{aligned} \tag{III.18}$$

with:

$$f_k(x) = \begin{bmatrix} f_{1k} \\ f_{2k} \end{bmatrix} = \begin{bmatrix} -\dfrac{R_k}{L_k} i_{dk} + \omega_k i_{qk} - \dfrac{v_{sdk}}{L_k} \\ -\dfrac{R_k}{L_k} i_{qk} - \omega_k i_{dk} - \dfrac{v_{sqk}}{L_k} \end{bmatrix} ; g_k(x) = \begin{bmatrix} g_{1k} \\ g_{2k} \end{bmatrix} = \begin{bmatrix} -\dfrac{1}{L_k} & 0 \\ 0 & -\dfrac{1}{L_k} \end{bmatrix}$$

From equation (III.18), the equivalent control law can be defined by:

$$\begin{aligned} u_{eqdk} &= \frac{\dot{i}_{drefk} - f_{1k}(x) - k_{ik}\left(i_{idk} - i_{idrefk}\right)}{g_{1k}} \\ u_{eqdk} &= \frac{\dot{i}_{qrefk} - f_{2k}(x) - k_{ik}\left(i_{iqk} - i_{iqrefk}\right)}{g_{2k}} \end{aligned} \tag{III.19}$$

Discontinuous Control Design:

In the case where the state trajectory is different from the sliding surface, the discontinuous control ensures the reduction of the distance between the state trajectory and its sliding surface. The discontinuous control law is defined as:

$$\begin{aligned} \dot{S}_{1k} &= -k_{i1k}sign(S_{1k}) \\ \dot{S}_{2k} &= -k_{i2k}sign(S_{2k}) \end{aligned} \tag{III.12}$$

k_{dc} *and* k_{ijk} are positive constants.

The sliding mode control law is then given by:

$$\begin{aligned} v_{tdrefk} &= -k_{i1k}sign(S_{1k}) + \frac{\dot{i}_{drefk} - f_{1k}(x) - k_{ik}\left(i_{idk} - i_{idrefk}\right)}{g_{1k}} \\ v_{tqrefk} &= -k_{i2k}sign(S_{2k}) + \frac{\dot{i}_{qrefk} - f_{2k}(x) - k_{ik}\left(i_{iqk} - i_{iqrefk}\right)}{g_{2k}} \end{aligned} \tag{III.13}$$

III.3.1.2 DC Voltage Controller Design

The third surface is that of DC voltage, the sliding surface is defined by:

$$S_{dc} = v_{dc2} - v_{dcref\,2} + k_{idc}\int\left(v_{dc2} - v_{dcref\,2}\right)dt \tag{III.14}$$

During the sliding mode, we have:

$$\dot{S}_{dc} = f_{dc}(x) + g_{dc}(x)u - \dot{v}_{dcref\,2} + k_{dc}\left(v_{dc2} - v_{dcref\,2}\right) = 0 \tag{III.15}$$

Where:

$$f_{dc}(x) = -\frac{i_{line}}{C}\,;\, g(x) = \frac{v_{sdk}}{Cv_{dck}}$$

From equation (III.15), the equivalent control law can be defined by:

$$u_{eqdc} = \frac{\dot{v}_{dcref\,2} - f_{dc}(x) - k_{dc}\left(v_{dc2} - v_{dcref\,2}\right)}{g_{dc}(x)} \tag{III.16}$$

The discontinuous control law is chosen as:

$$\dot{S}_{dc} = -k_{dc}sign(S_{dc}) \tag{III.17}$$

where k_{dc} is a positive constant.

The sliding mode control law is then given by:

$$i_{dref\,2} = -k_{dc}\,sign(S_{dc}) + \frac{\dot{v}_{dcref\,2} - f_{dc}(x) - k_{dc}\left(v_{dc2} - v_{dcref\,2}\right)}{g_{dc}(x)} \tag{III.18}$$

III.4 SMC of Point-to-Point VSC-based HVDC System

III.4.1 Point-to-Point VSC-based HVDC SMC Scheme

Figure (III.2) presents a Point-to-Point VSC-HVDC system and its SMC control scheme block diagram.

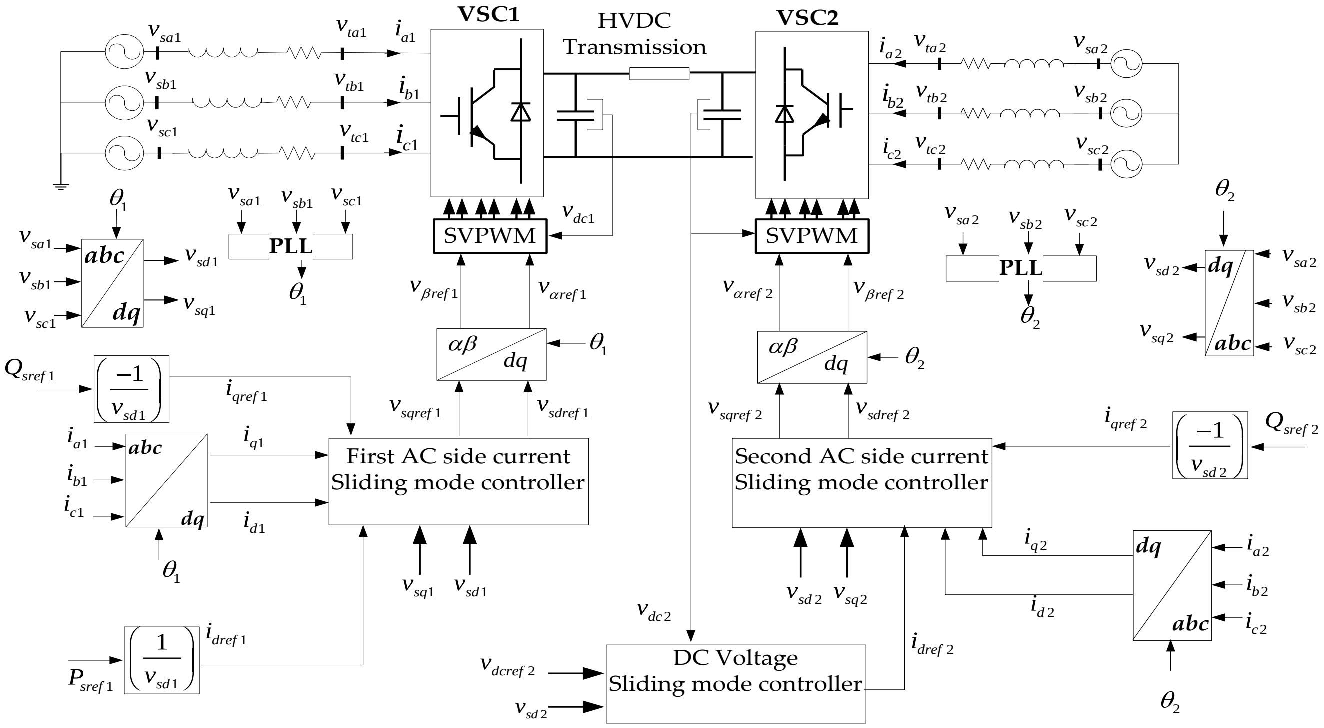


Figure (III.2): Block diagram of the SMC control of VSC-based Point-to-Point HVDC system.

III.4.2 SMC based Point-to-Point VSC-based HVDC Simulation

In order to test the behavior of the VSC based HVDC transmission system controlled by SMC, the system was implemented in the same conditions to those of the previous chapter.

To analyze the performance of the designed control system, the following same scenarios are adopted.

- At t=0.3 s, the controlled output reference signal of the active power is increased from 200 MW to 300 MW.
- At t=0.6 s, the controlled output reference signal of the reactive power for VSC1 is changed from 0 to 50 MVAR.
- At t=0.9 s, the controlled output reference signal of DC voltage is increased from 90 kV to 92 kV.

- At t=0.11 s, the controlled output reference signal of the reactive power for VSC2 is changed from 0 MVAR to 50 MVAR.

Figure (III.3) illustrates the active and reactive powers of both VSC1 and VSC2 AC side terminals as well as their reference values. The figure shows that the measured powers follow their references after a short startup transient periods showing quick stabilization without overshoot on both AC sides. At t=0.3s,the active power reference changes and the VSC1 AC side follows it with almost no transient, but the active power on the VSC2 side has a brief transient. At t =0.9s, an overshoot in the VSC2 active power is noted; this overshoot is due to the change in the DC voltage. Noting that the active and reactive powers are controlled separately and their variations are completely decoupled. Further, the waveforms of the active power at each side are approximately equal, as can be seen in Figure (III.3). Certainly, the active power generated by the terminal VSC1 is nearly equivalent in absolute value with that received by the terminal VSC2. However, the small deference of power on the absolute value is due to the transmission loss in the DC line.

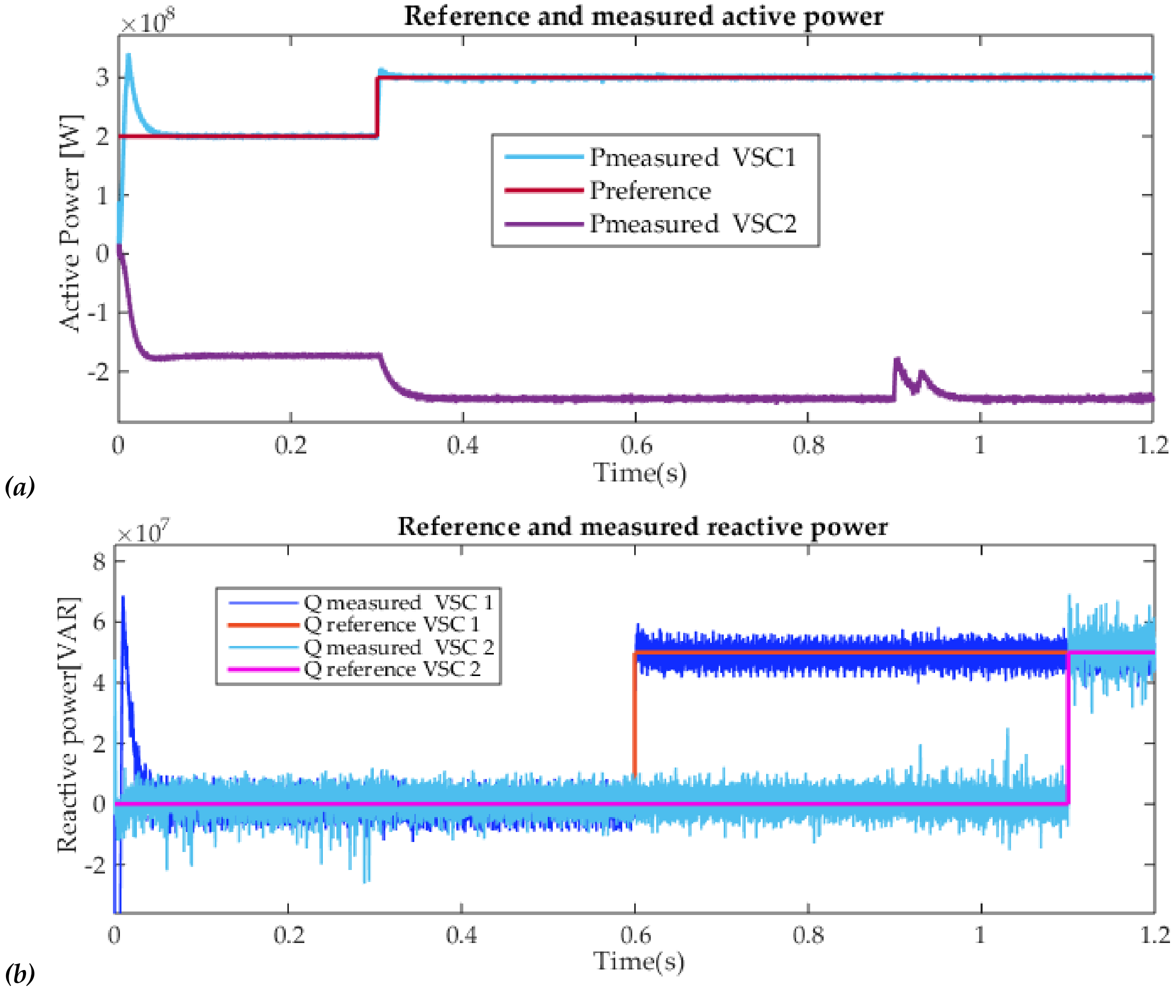


Figure (III.3): Reference and measured powers of VSC1 and VSC2 terminals: (a) active powers, (b) reactive powers

Regarding the reactive powers in both terminals as illustrated in Figure (II.3), they follow with precision their references; the stabilization is almost without delay with any transients and overshoots. It should be pointed out that the reactive power reference changes in one terminal do not influence the other terminal. From this, it can be concluded that the VSC1 and VSC2 control the reactive power disjointedly.

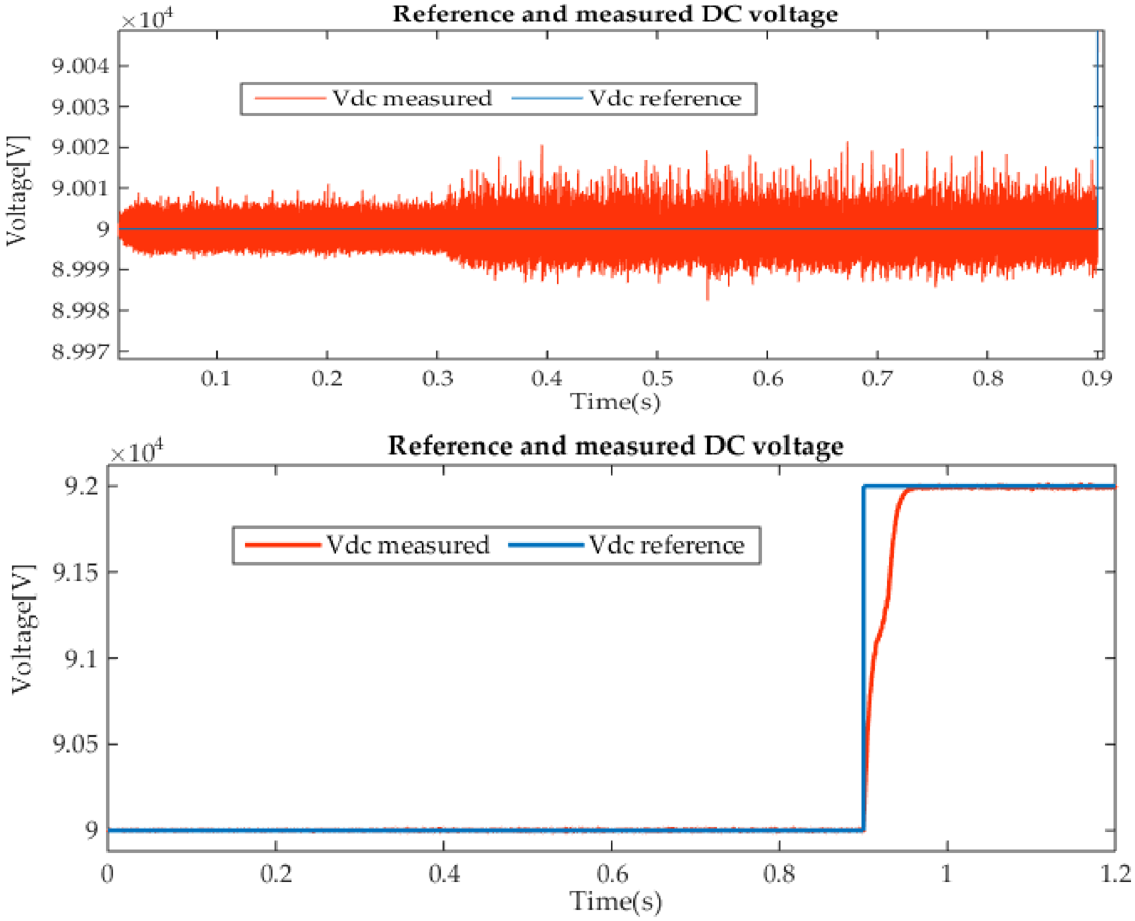


Figure (III.4): Reference and measured DC voltage

It is possible to observe from the result of Figure(III.4) that the measured DC voltage follows its reference maintaining almost constant and stable with no transient and overshot. However, the change in its reference at t=0.9s induces a transient in DC voltage response that is quickly stabilized.

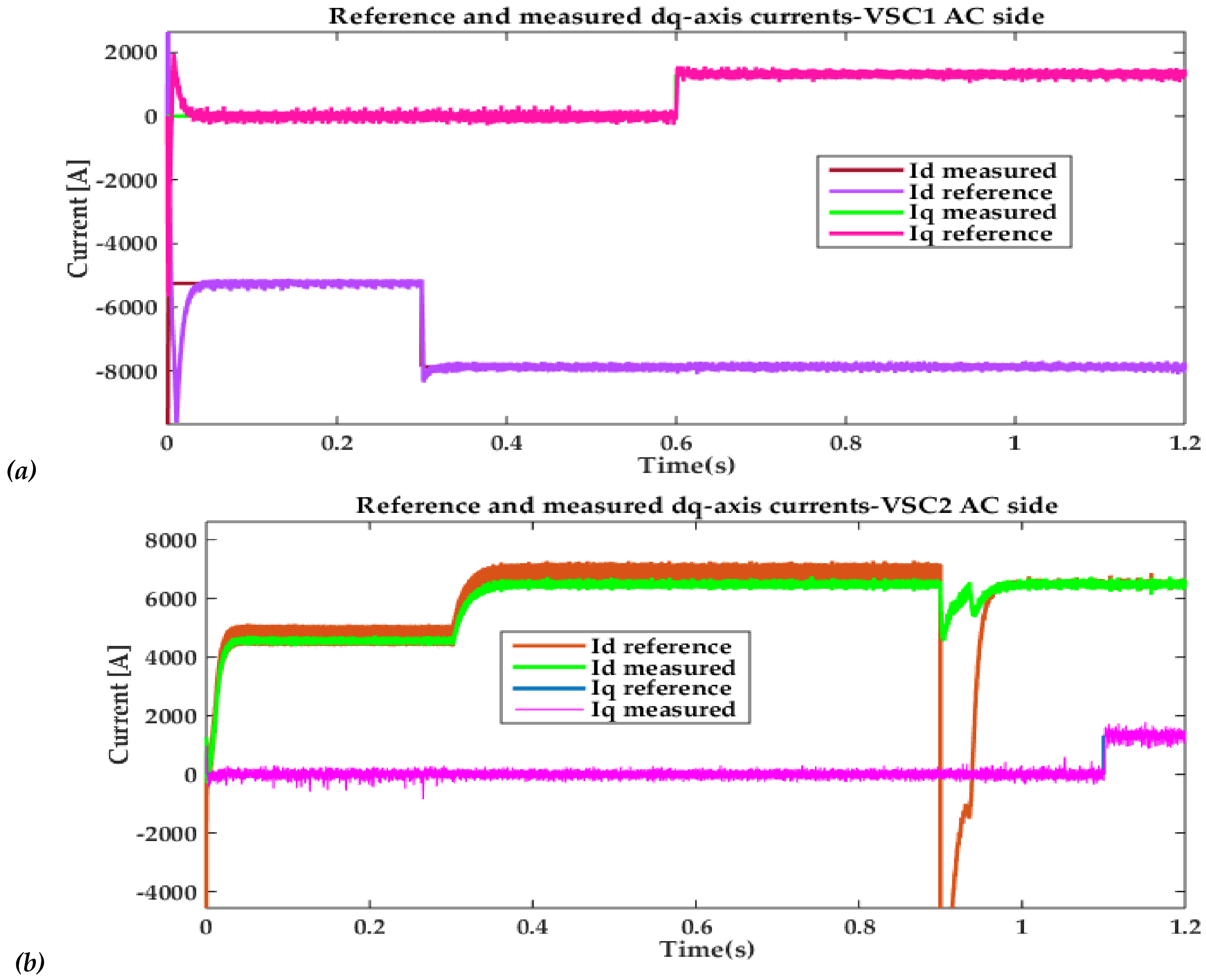


Figure (III.5): Reference and measured *dq*-axes currents: a)VSC1 AC side currents, b) VSC1 AC side currents.

It can be seen from Figure (III.5) that the *dq*-axis currents variations are similar to those in the powers flow due to the fact that the powers are determined by *dq*-axes currents components. Moreover, it can be seen from Figure (III.6), the two *dq*-axes components of both AC sides currents follow quite well their reference signals. However, the reference DC voltage change occurred at t=0.9s has a negative impact on *d*-axis current of the terminal VSC2 causing an excessive undershoot.

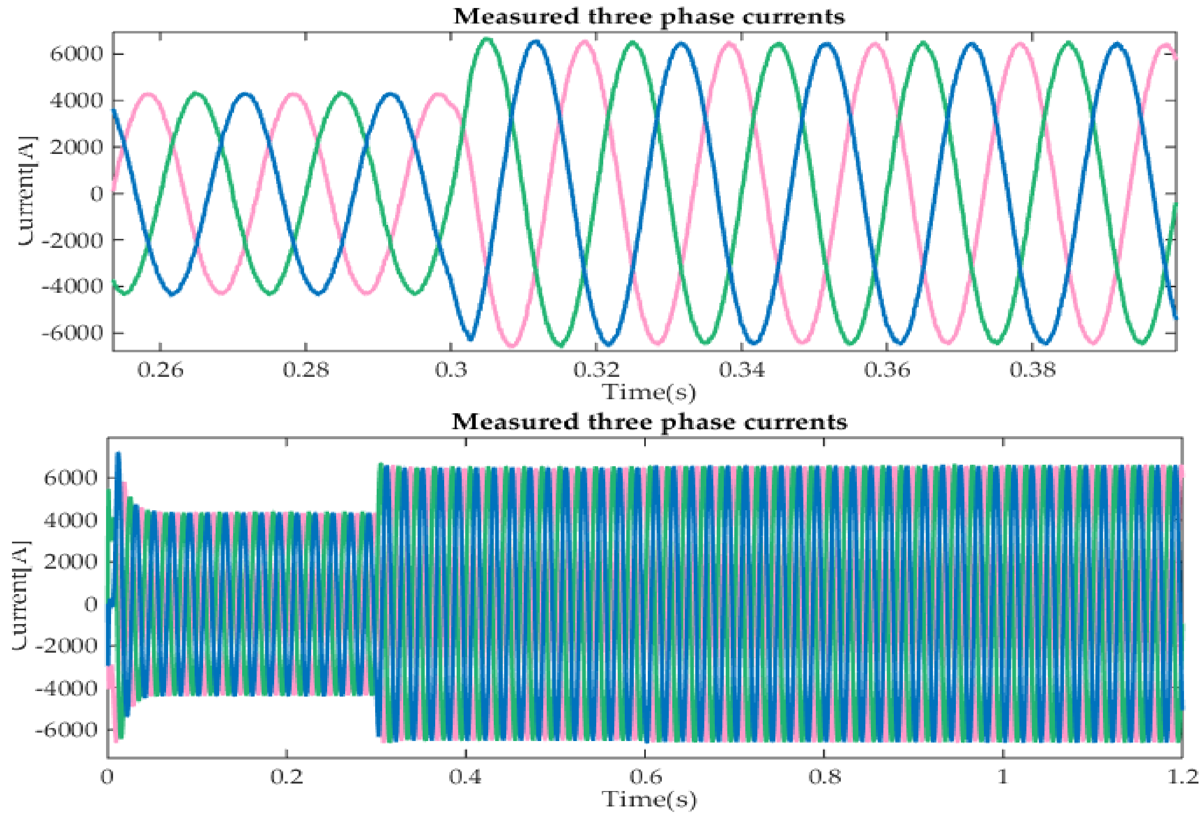


Figure (III.6): VSC1 AC side three phase currents

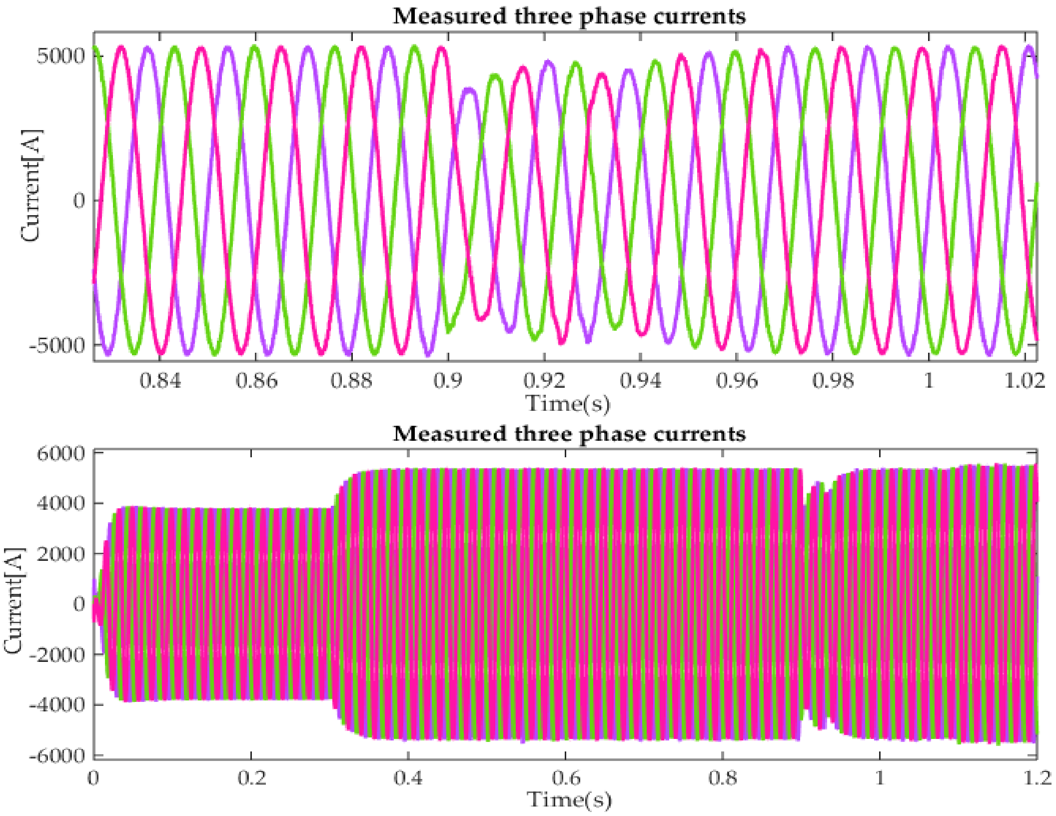


Figure (III.7): VSC2 AC side three phase currents

The three-phase line currents of each VSC are given in Figures (III.6)and (III.7). As can be noted from these results, the curves of line currents on both terminals are sinusoidal with different frequencies. By comparing the line currents measured at VSC1, when working at 50 Hz, with those measured at VSC2, when working at 60 Hz, no noticeable difference in the dynamics can be observed. Consequently, if the synchronization with the grid is well obtained no differences in sending power between areas working at different frequencies shall occur. Also, it can be remarked that the curves of the currents at VSC2 side are disturbed at t=0.9s; the same instant at which the DC voltage changes affecting thus the active power injected in the VSC2 AC side.

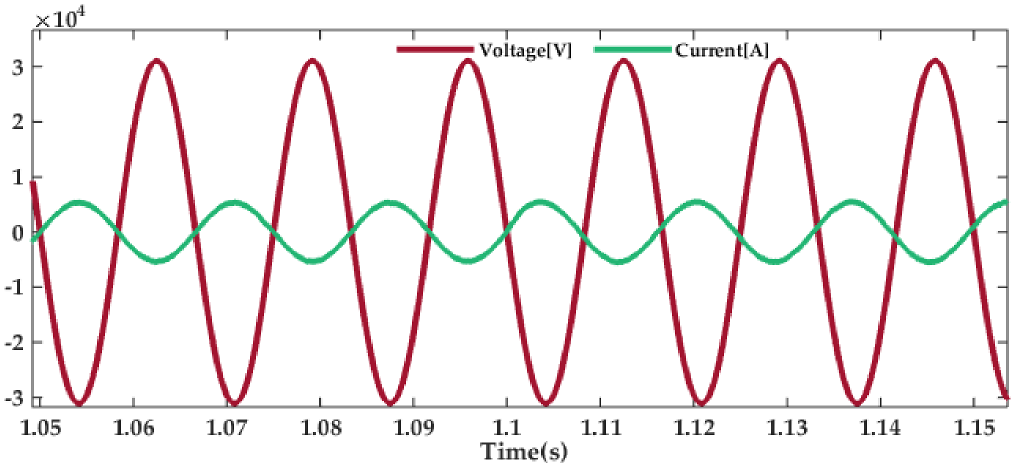
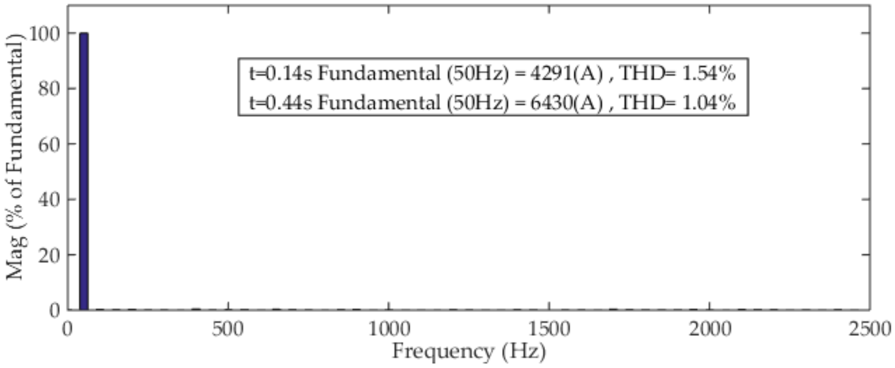
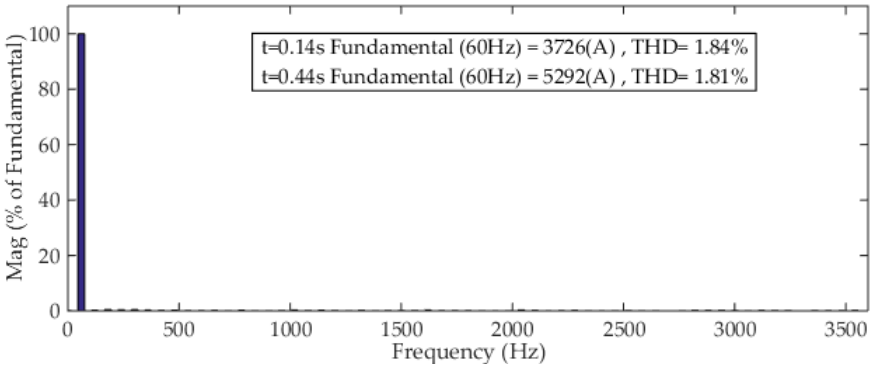


Figure (III.8): VSC2 AC side measured phase current and voltage

As can be detected from Figure (III.28), the waveform of the output phase voltage and current at the VSC2 AC side are in phase hence signifying a unity power factor. until the moment t=1.1s at which the injected reactive power change reference from 0VAR to 50MVAR. it can be noted that the waveform of the current is leading compared to the measured voltage.



(a)



(b)

Figure(III.9):Line currents harmonic spectra: (a) VCS1 AC side currents, (b) VCS2 AC side currents

Figure (III.9) shows the line currents harmonic spectra. It is can be seen that the total harmonic distortion (THD) varies between 1.54% and 1.84% before the variation of the active power and 1.04% and 1.81% after its variation for VSC1 and VSC2, respectively. So, the THD values are in conformity with IEEE 519 standard since their values do not exceed 5% as recommended.

III.5 SMC of Back-to-Back VSC-based HVDC System

III.5.1 Back-to-Back VSC-based HVDC SMC Scheme

The SMC scheme of Back-to-Back VSC-based HVDC system is presented in Figure (III.10).

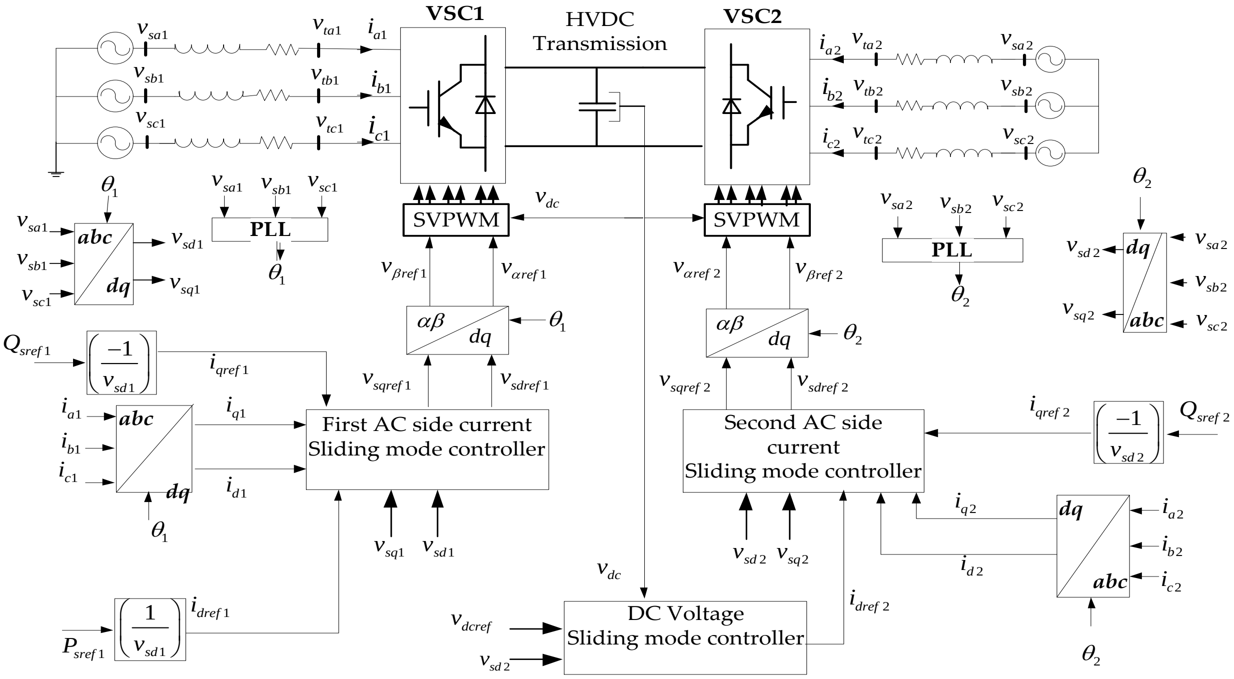


Figure (III.10): Block diagram of the SMC control of VSC-based Back-to-Back HVDC system.

III.5.2 SMC based Back-to-Back VSC-based HVDC Simulation

In order to analyze the response of the designed sliding mode controller applied on the Back-to-Back VSC-based HVDC system, the same tests adopted in the previous section will be also adopted herein.

Figures (III.11) presents the reference and measured active and reactive powers at the each AC side of both terminals.

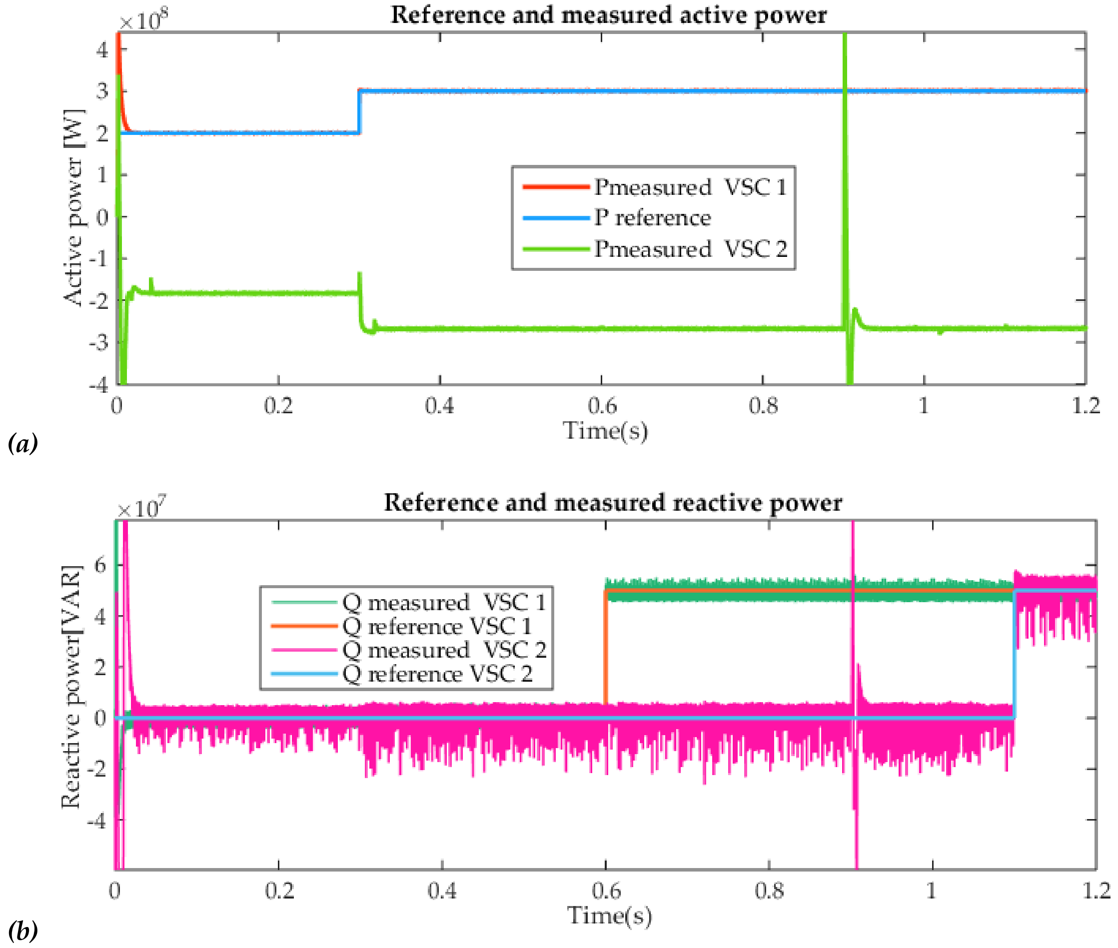


Figure (III.11): Reference and measured powers of VSC1 and VSC2 terminals: (a) active powers, (b) reactive powers

From Figure (III.11), it can be observed that after an approximately small startup transient the active and reactive powers stabilize at their desired reference values. However, due to the shift in the DC voltage references at t=0.9s the active and reactive powers spikes a short moment of time, after that they regain their references.

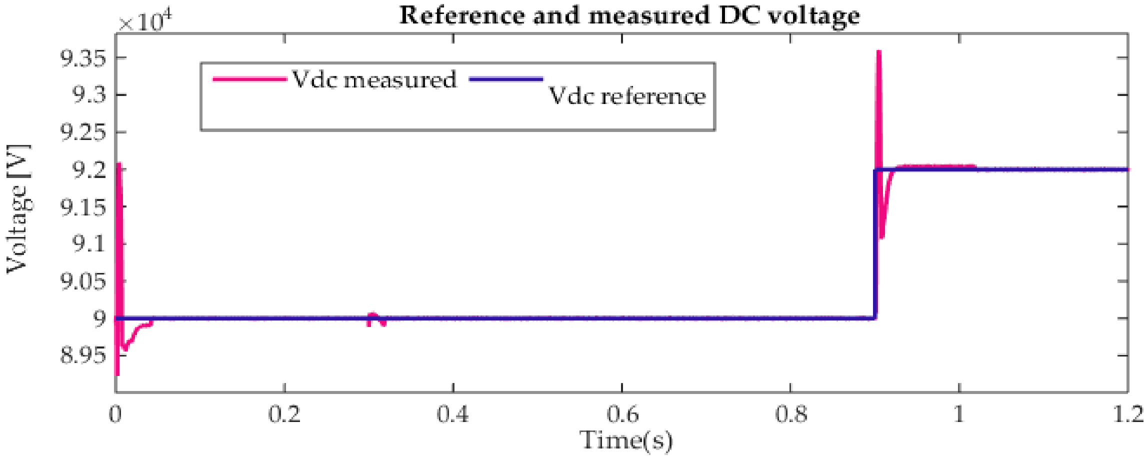


Figure (III.12): Reference and measured DC voltage

According to Figure (III.12), the DC-link voltage mirrors its reference value after a pretty short transient regime with an overshoot less than 2.5%. At t=0.3 due to the rise in active power a small transient occurs yet it is quickly restored. At t=0.9, it is observed that the reference value is correctly followed by the measured DC voltage after a relatively large overshoot.

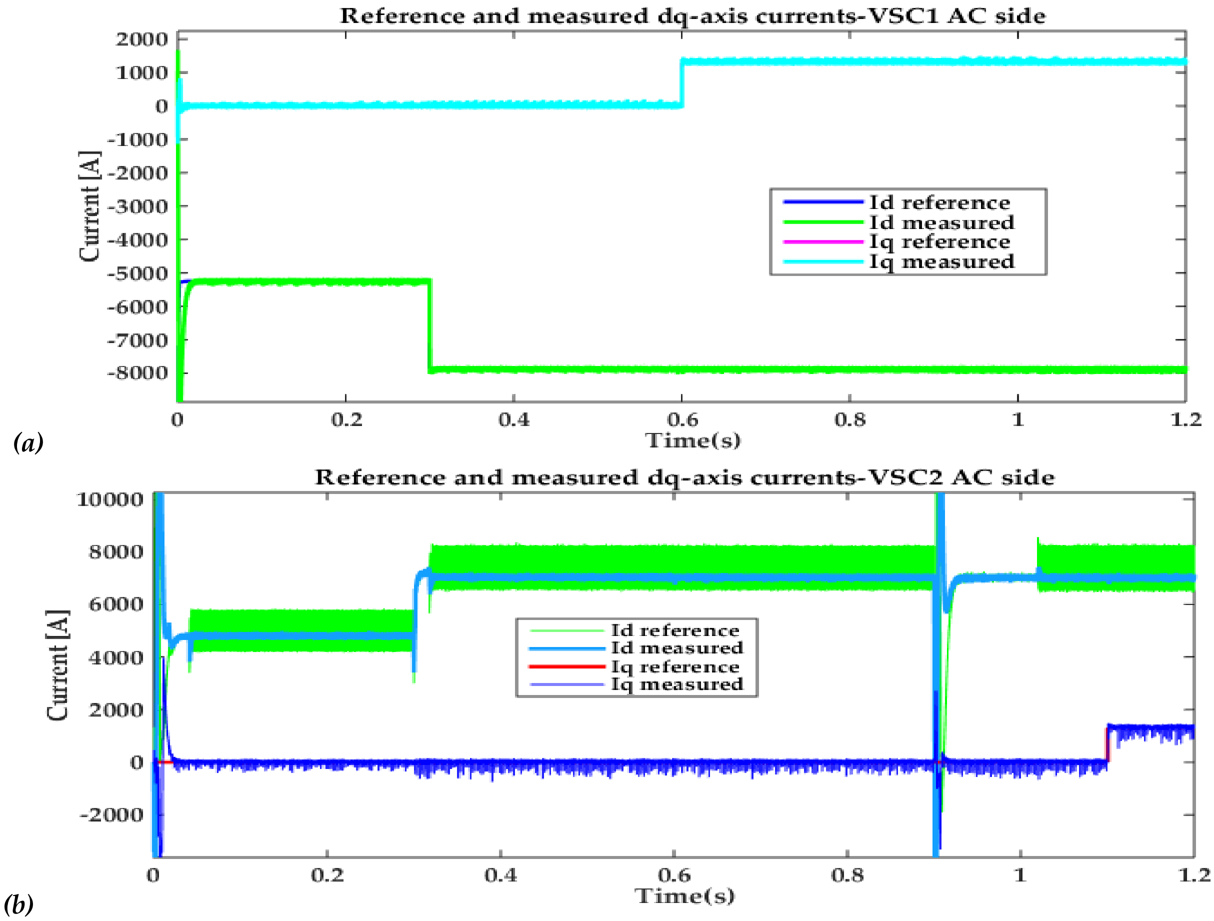


Figure (III.13): Reference and measured *dq*-axes currents: a)VSC1 AC side currents, b) VSC1 AC side currents.

Figure (III.13) demonstrates the performance of the *dq*-axes currents as they follow their references. However, the change in references DC voltage at t=0.9s provokes transient in the active power, which is in turn reflected in the current d-axis component. It can be seen that, this transient affects also the reactive power or current q-axis component of the VSC2 AC side only unlike the VSC1 AC side where no transient and overshoot are noted.

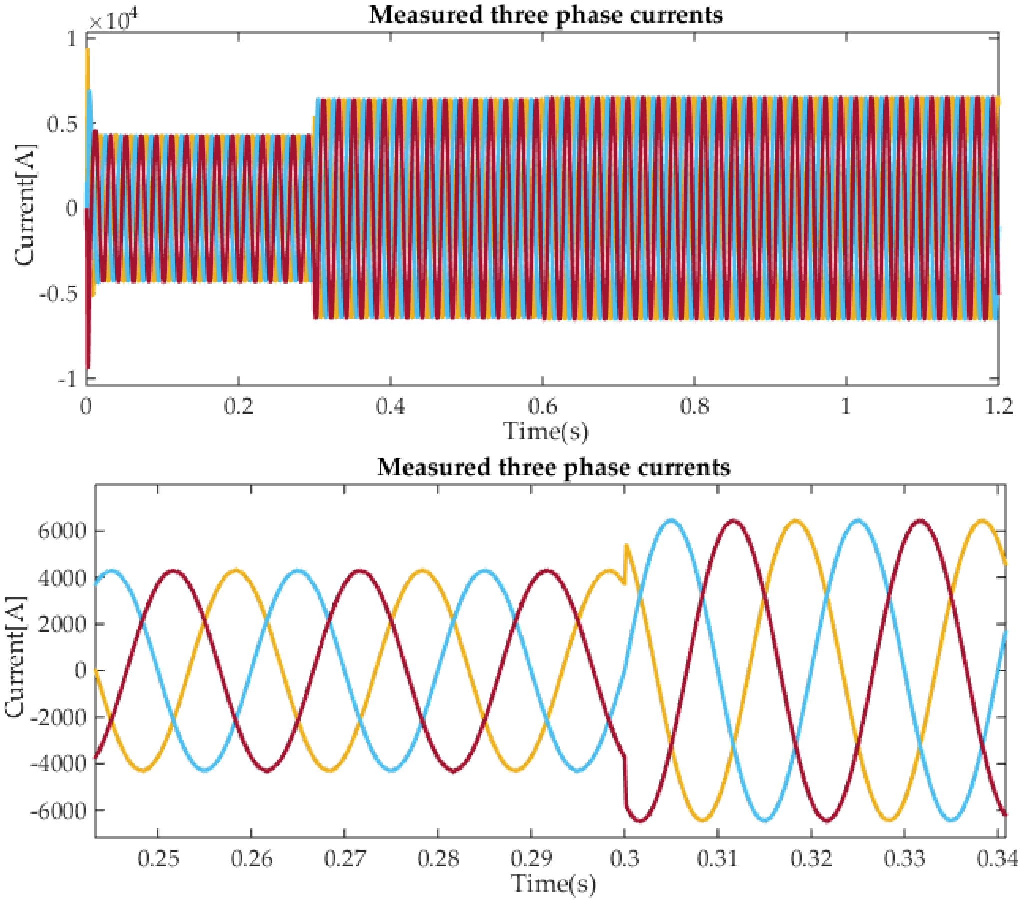


Figure (III.14): VSC1 AC side three phase currents

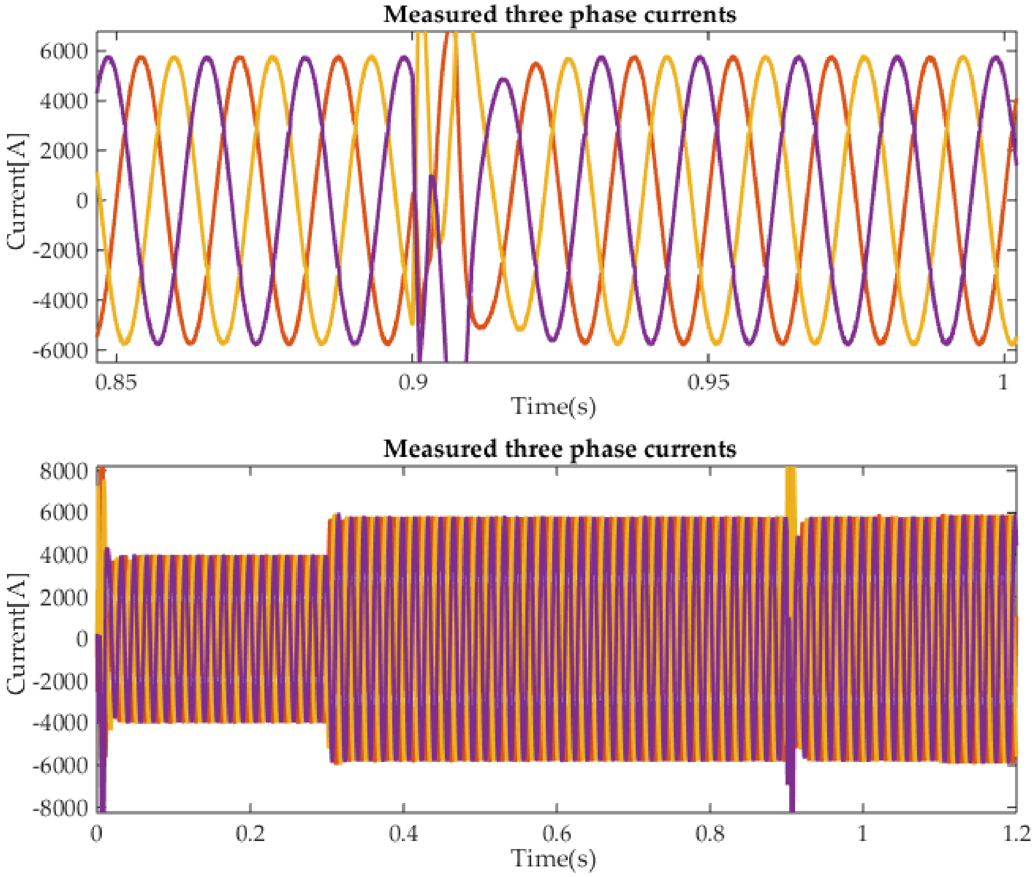
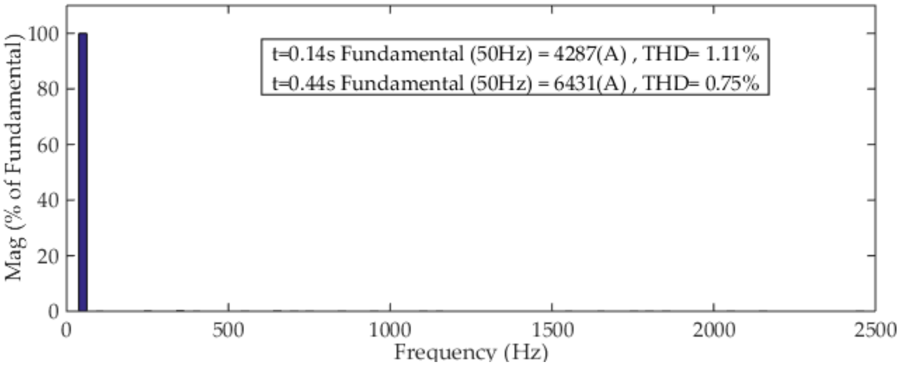
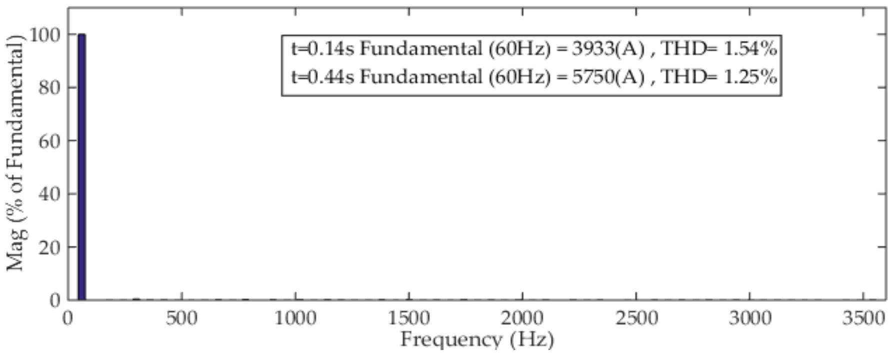


Figure (III.15): VSC2 AC side three phase currents

Figures (III.14)and (III.15) present the three-phase line currents of each VSC showing that the line currents, at start-up and during the power reference changing, are affected with short transient regimes. All waves stabilize at their nominal values when the steady-state is reached. By comparing these plots no differences in the dynamics of the currents can be seen regardless of the difference in frequencies. Accordingly, it can be observed that the synchronization with the grid is well achieved and no abnormalities in transferring power between areas operating at deferent frequencies are observed.



(a)



(b)

Figure(III.16):Line currents harmonic spectra: (a) VCS1 AC side currents, (b) VCS2 AC side currents

The line currents harmonic spectra plotted in figure (III.16) shows that the total harmonic distortion (THD) varies between 1.11% and 1.54% before the variation of the active power and 0.75% and 1.25% after its variation for VSC1 and VSC2, respectively. The THD values are smaller than 5%, which is in concordance with IEEE 519 standard.

III.6 Comparative Study between the SMC and PI Controllers

III.6.1 Point-to-Point VSC-based HVDC Configuration

This test is done to show the robustness of the control against sudden variations in DC voltage and in the active and reactive powers.

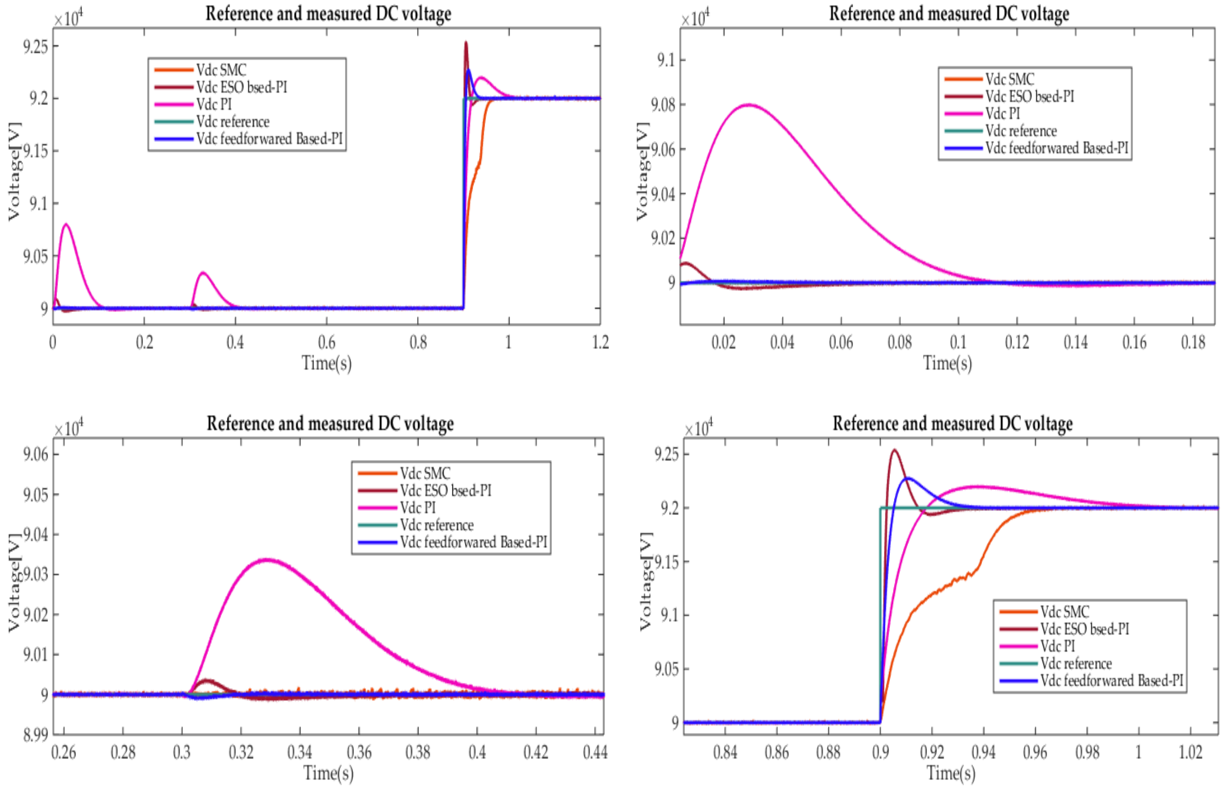
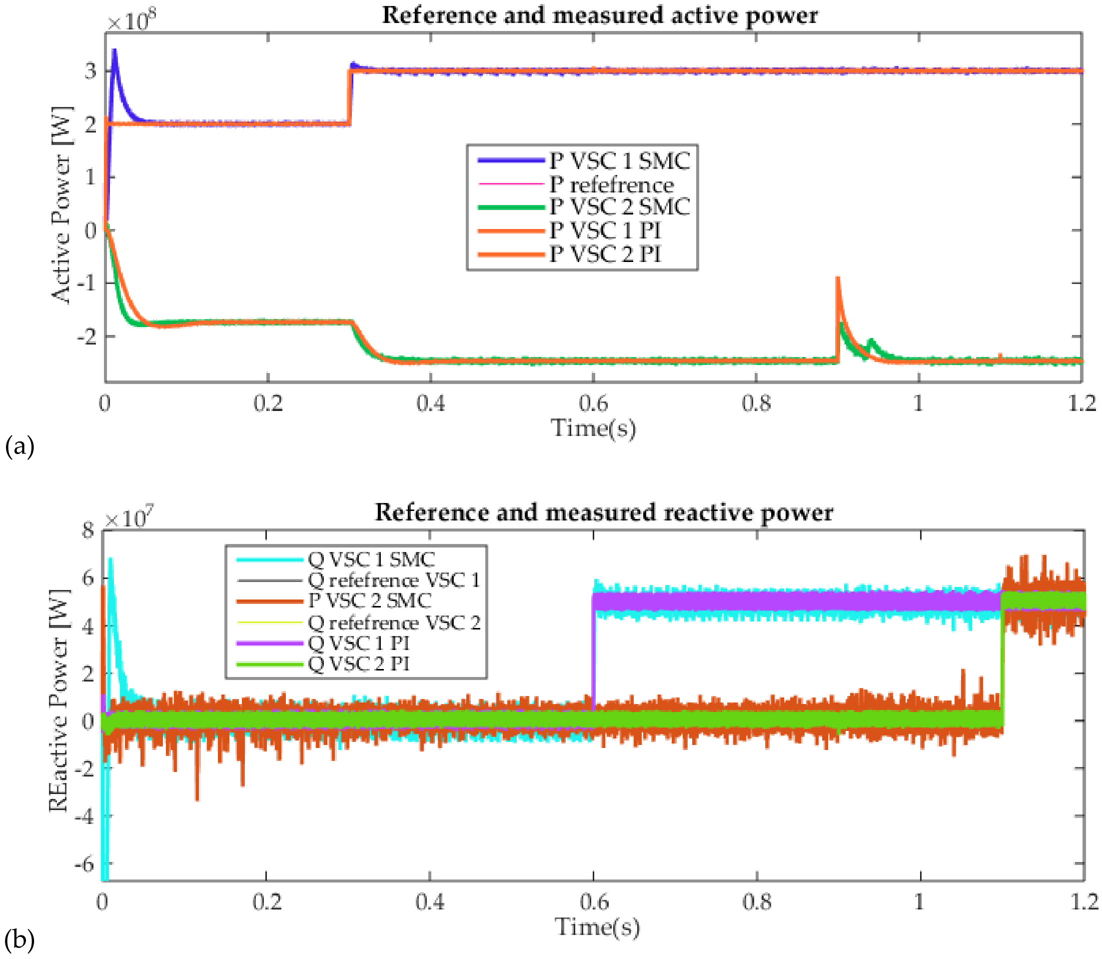


Figure (III.17): Reference and measured DC voltage

Figure (III.17) shows the DC voltage responses using the sliding mode controller as well as three different PI-based controllers. As can be seen, all controllers have almost the same performance in steady state in terms of tracking a predetermined reference. At t=0.3s, where the injected active power raises, the SMC controller compensated for well the transient with no overshoot compared to PI-based controller. At t=0.9s,using SMC, the DC voltage flows its reference change without overshoot compared with the others PI variants. In this, the traditional PI control technique has the worst performance in term of convergence time.



(a)

(b)

Figure (III.18): Reference and measured powers of VSC1 and VSC2 terminals: (a) active powers, (b) reactive powers

Figure (III.18) presents the active and reactive powers at each end of HVDC system when it is controlled by PI and SMC controllers. It can be observed that at the start transient the SMC controller has an overshoot in both active and reactive powers of the first terminal compared to the PI-based control. However, the second terminal powers have a better performance in term of convergence time, where, at the start, the active power of the SMC controller converges faster than that of PI based control. Also, at t=0.9s, the power overshoot caused by the change in DC voltage is much smaller in case of SMC than that in case of PI. Nevertheless, the main downfall of the SMC controller is its chattering effect, which is clear in also in Figure (III.19).

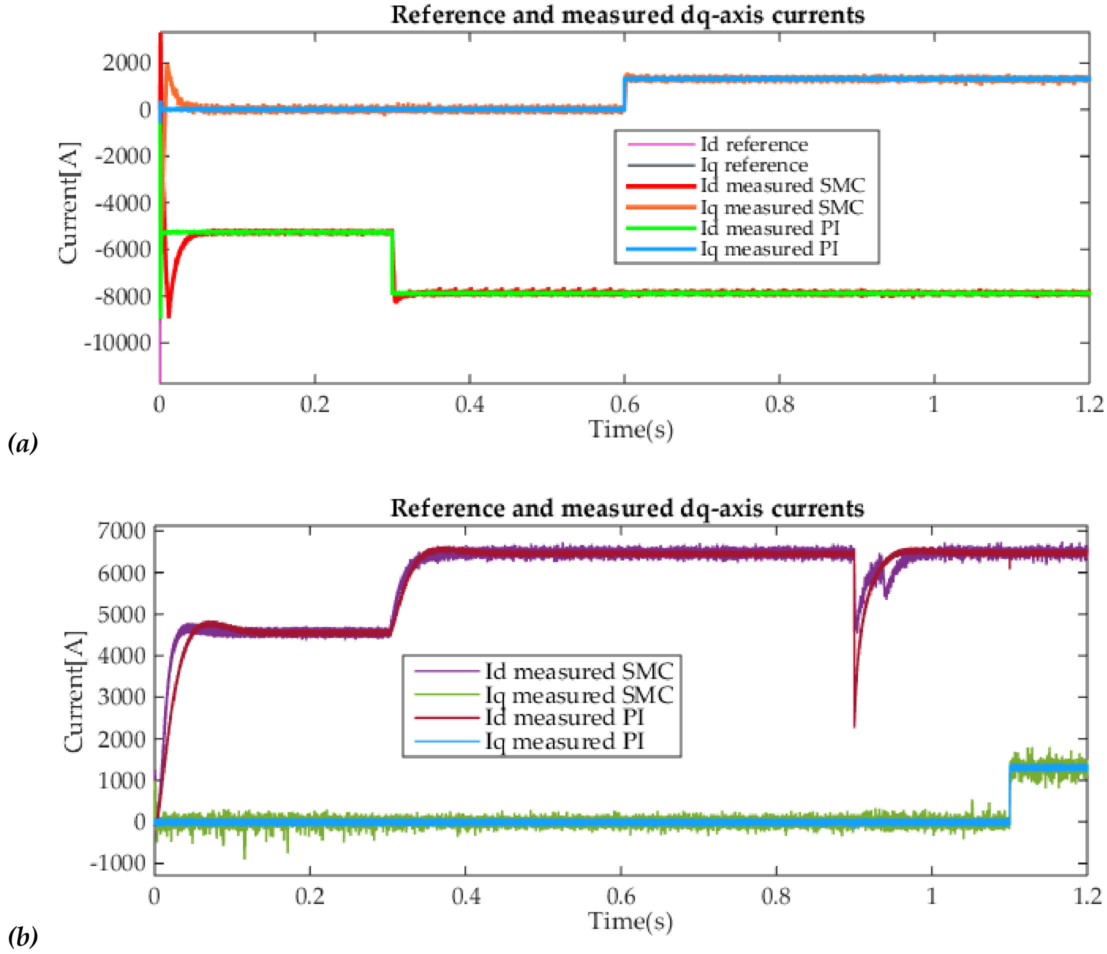


Figure (III.19): Reference and measured *dq*-axes currents: (a)VSC1 AC side currents, (b) VSC2 AC side currents

III.6.2Back-to-Back VSC-based HVDC Configuration

Figure (III.20) shows the DC voltage responses controlled by using both SMC and PI controllers, where the traditional PI has the worst performance. At t=0.3s, a transient occurs on the DC voltage, which is caused by the increased active power. Between all controllers, the SMC has the least overshoot and stabilizes fast the DC voltage at its set-point. However, at the start and at t=0.9s, the DC voltage controlled by SMC has a relatively large overshoot compared to the others PI controllers.

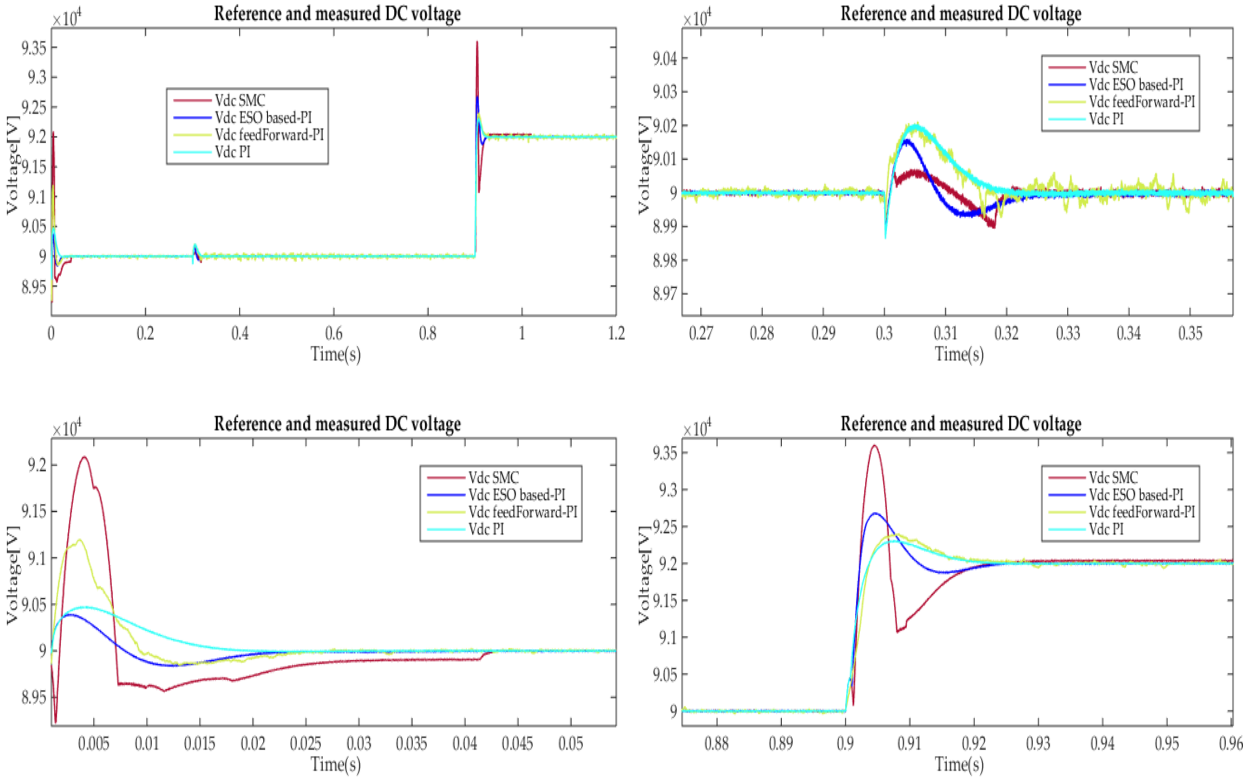
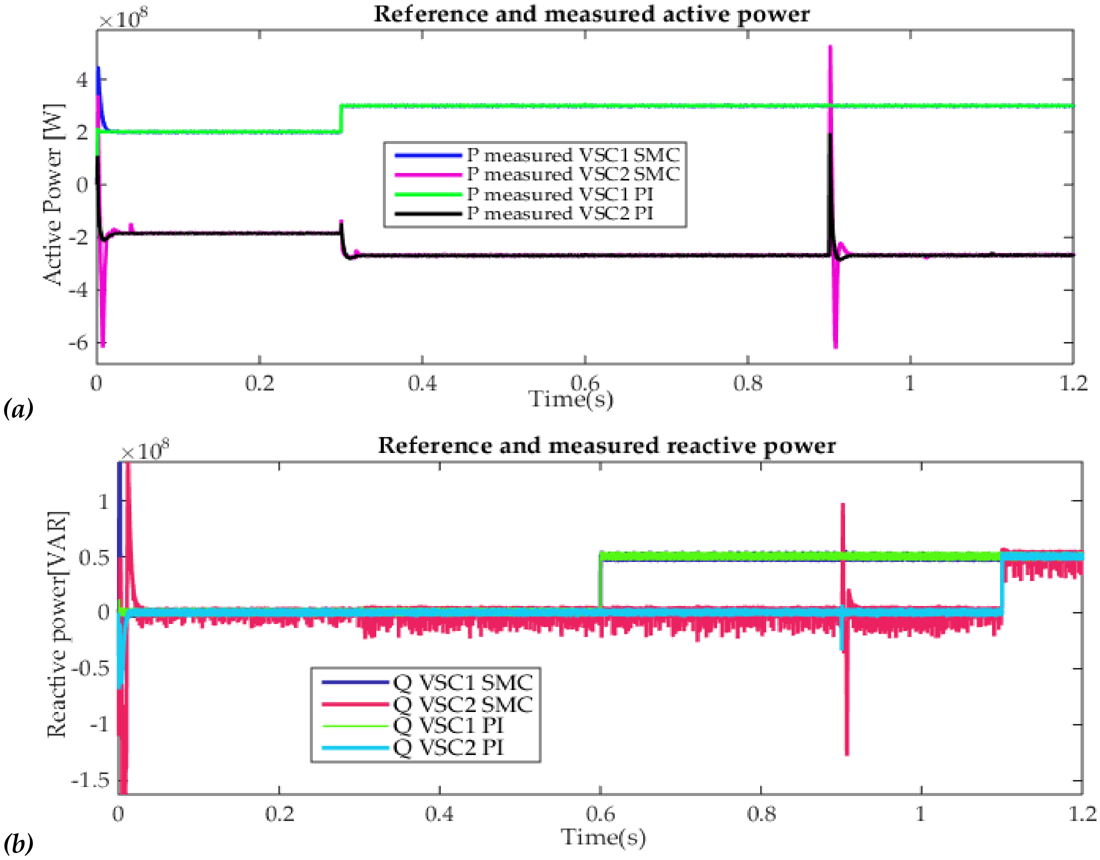


Figure (III.20): Reference and measured DC voltage



(a)

(b)

Figure (III.21): Reference and measured powers of VSC1 and VSC2 terminals: (a) active powers, (b) reactive powers

Figure (III.21) exhibits the active and reactive powers at each end of the HVDC system controlled by PI and SMC controllers. It can be observed that the powers curves are much chattered when using SMC compared to the PI controller case. At t=0.9s, the powers overshoots using SMC controller are comparatively larger than that using PI controller but with lesser response time.

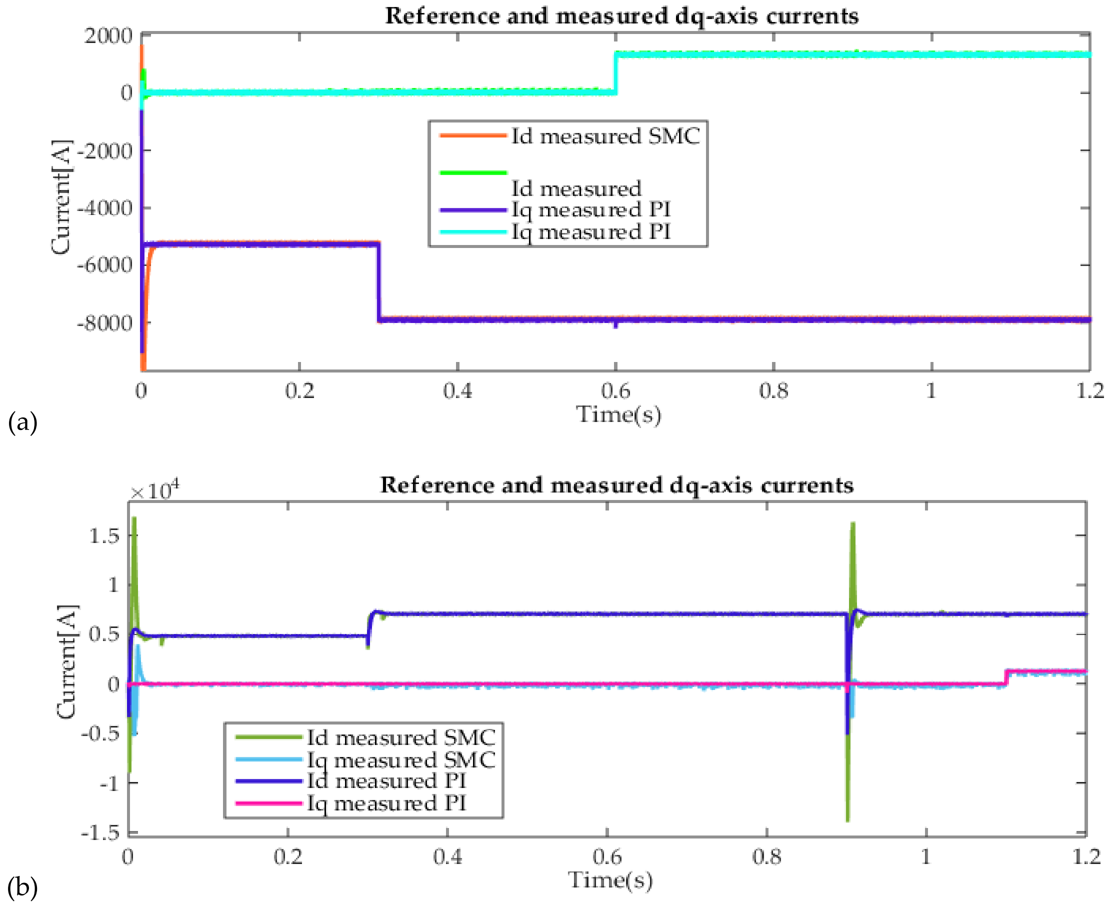


Figure (III.22): Reference and measured *dq*-axes currents: (a)VSC1 AC side currents, (b) VSC2 AC side currents.

Figure (III.22) shows the performance of the *dq*-axes currents in both HVDC terminals with SMC and PI controllers. Again, the chattering effect is visible on these current curves when the sliding mode control is applied.

III.7 Second-Order Sliding Mode Control

Higher-order sliding modes (HOSM) have arisen as a hopeful strategy for managing the chattering problem while keeping the main advantages of the classical SMC concerning robustness, order reduction, simplicity, and facility of implementation [55]–[57].

Moreover, it is alleged that the practical implementation of HOSM results in a higher accuracy contrasted to the classical SMC in the presence of switching delays and measurement noise [58]. HOSM is regarded as an extension of the classical sliding mode theory. In this context, classical

SMC previously presented is usually referred to as first-order sliding mode control (1-SMC). Another reason for developing this method is that the 1-SMC is limited to applications where the relative degree within the system and the sliding variable has to be one, which can limit the choice of the sliding variable [59]. The main idea is to increase the order of the controlled system by adding integrators to the input channel before the application of the actual control signal. Consequently, the discontinuous control component acts on the higher-order time derivative of the sliding variable rather than its first-time derivative like in 1-SMC. In other words, this new strategy can significantly reduce the chattering effect considering the actual discontinuous control action is "embedded" in the higher derivative of the sliding variable [59], [53], [60].

There are several algorithms to accomplish HOSM. In particular, the second order sliding mode controllers (2-SMC) are applied to zero the outputs with relative degree two or to avoid chattering while zeroing outputs with relative degree one. Among second order algorithms, one can find the sub-optimal controller, the terminal sliding mode controllers, the twisting controller, and the super-twisting controller. In particular, the twisting algorithm forces the sliding variable of relative degree two into the 2-sliding set, requiring knowledge of *S(x).* The super-twisting algorithm does not require that, but the sliding variable has relative degree one. Therefore, the super-twisting algorithm is nowadays favored over the classical siding mode, since it eliminates the chattering phenomenon.

This section presents a brief review on the super-twisting algorithm, which has been successfully implemented to solve the chattering problems.

III.7.1 Basic Concepts Second-Order Sliding Mode Control: Super Twisting Algorithm

Considering an uncertain nonlinear system whose dynamics is described by:

$$\begin{cases} x^n = f(x) + g(x)u \\ S = S(x) \end{cases} \tag{III.19}$$

where $x \in R^n$ is the state vector; t is the time; $u \in R$ is the control input; $f(x)$ and $g(x)$ are some smooth and uncertain vector functions; *S* is the sliding variable. The sliding surface is defined to fulfill the required control specifications, and is designed such that it has a relative degree *r* with respect to the control variable *u* to ensure convergence in infinite time.

The control objective in 1-SMC is to drive the designed sliding variable *S* to zero in finite time. While for 2-SMC, it is required to drive both the sliding variable *S* and it derivative $\dot{S}$ to zero in finite time. This is done by means of a discontinuous control action that acts on the second derivative of the sliding variable $\ddot{S}$ [53].

Although it is a 2-SMC, this algorithm was originally developed for systems with relative degree one for the purpose of avoiding the chattering problem connected with the application of 1-SMC [55]. In other words, this algorithm can drive both the sliding variable and its derivative to zero in finite time only when the relative degree of the system is one.

The control signal of the sliding mode control usually can be broken into two parts, one concerning the equivalent control, which deals with the dynamics of the system and the sliding surface, and another concerning the switching control, which is accountable for maintaining the dynamics of the system onto the sliding surface.

Defining the sliding surface as:

$$S(x) = e \tag{III.20}$$

where e is the tracking error defined as follows:

$$e = x - x_{ref} \tag{III.21}$$

where x_{ref} is the desired trajectory, and x is the actual trajectory.

The sliding mode control is given:

$$u = u_{eq} + u_{sw} \tag{III.22}$$

where u_{eq} is the equivalent control proposed by *Filipov* without regarding the system uncertainty and external disturbance. It serves to keep the variable to control on the sliding surfaces. The equivalent control is derived by considering that the derivative of the surface is null $S(x) = 0$. u_{sw} is the discrete control, which ensures convergence such that $\dot{S}S < 0$.

In Super-Twisting sliding mode control, switching control is usually adopted as:

$$\begin{aligned} u_{sw} &= -\lambda |S|^{\frac{1}{2}} sign(S) + u_1 \\ \dot{u}_1 &= -\alpha sign(S) \end{aligned} \tag{III.23}$$

Therefore, the time derivative of the sliding surface *S(x)* is:

$$\dot{S}(x) = \dot{e} = \dot{x} - \dot{x}_{ref} \tag{III.24}$$

Equation (III.19) can be rewritten:

$$\dot{S} = f(x) + g(x)u - \dot{x}_{ref} \tag{III.25}$$

Setting $\dot{S}(x) = 0$, then the equivalent control law can be obtained:

$$u_{eq} = \frac{-f(x) + \dot{x}_{ref}}{g(x)} \tag{III.26}$$

The switching control law is designed based on the Super-Twisting algorithm, the algorithm is as follow:

$$u_{sw} = -\lambda |S|^{\frac{1}{2}} sign(S) - \int \alpha sign(S) dt \tag{III.27}$$

where α and λ are positive constants.

The final control law can be obtained as follows:

$$u = \frac{-f(x) + \dot{x}_{ref}}{g(x)} - \lambda |S|^{\frac{1}{2}} sign(S) - \int \alpha sign(S) dt \tag{III.28}$$

III.7.2Stability Analysis

The work presented in[61]-[62] suggests quadratic like *Lyapunov* functions for the super-twisting controller, making it possible to obtain an explicit relation for the controller design parameters. In the following lines, this analysis will be revisited.

Considering the following SISO nonlinear scalar system:

$$\dot{S} = \psi(S) + u \tag{III.29}$$

Where $\psi(S)$ is an unknown bounded perturbation term and globally bounded by $|\psi(S)| \le \delta |S|^{\frac{1}{2}}$ for some constant $\delta > 0$. The super-twisting sliding mode controller for perturbation and chattering elimination is given by:

$$\begin{aligned} u_{sw} &= -\lambda |S|^{\frac{1}{2}} sign(S) + u_1 \\ \dot{u}_1 &= -\alpha sign(S) \end{aligned} \tag{III.30}$$

System (III.29)closed by control (III.30)results in:

$$\begin{aligned} \dot{S} &= -\lambda |S|^{\frac{1}{2}} sign(S) + u_1 + \psi(S) \\ \dot{u}_1 &= -\alpha sign(S) \end{aligned} \tag{III.31}$$

Proposing the following candidate *Lyapunov* function:

$$V = 2\alpha |S| + \frac{1}{2} u_1{}^2 + \frac{1}{2}\left(\lambda |S|^{\frac{1}{2}} sign(S) - u_1 \right) = \xi^T P \xi \tag{III.32}$$

where

$$\xi^T = \left(|S|^{\frac{1}{2}} sign(S), u_1 \right)$$

$$P = \frac{1}{2} \begin{pmatrix} 4\alpha + \lambda^2 & -\lambda \\ -\lambda & 2 \end{pmatrix}$$

The time derivative of (III.32)is:

$$\frac{dV}{dt} = \frac{d}{dt}\left(\xi^T P \xi \right) = \dot{\xi}^T P \xi + \xi^T P \dot{\xi} \tag{III.33}$$

Equation (III.33) can be rewritten in the following form:

$$\dot{V} = -\frac{1}{\left|S^{1/2}\right|}\xi^T Q\xi + \frac{\psi(S)}{\left|S^{1/2}\right|}q^T\xi \tag{III.34}$$

where

$$Q = \frac{\lambda}{2}\begin{pmatrix} 2\alpha+\lambda^2 & -\lambda \\ -\lambda & 1 \end{pmatrix}$$

$$q^T = \begin{pmatrix} 2\alpha+\frac{1}{2}\lambda^2 & -\frac{1}{2}\lambda \end{pmatrix}$$

Applying the bounds for the perturbations as given in [61][62], the expression for the derivative of the *Lyapunov* function is reduced to

$$\dot{V} = -\frac{\lambda}{2\left|S^{1/2}\right|}\xi^T\widehat{Q}\xi \tag{III.35}$$

where

$$\widehat{Q} = \begin{pmatrix} 2\alpha+\lambda^2-(\frac{4\alpha}{\lambda}+\lambda)\delta & -\lambda+2\delta \\ -\lambda+2\delta & 1 \end{pmatrix} \tag{III.36}$$

$\dot{V}$ is negative if $\widehat{Q} \geq 0$, which is valid if the controller gains α and λ satisfy the following conditions:

$$\lambda > 2\delta, \quad \text{and} \quad \alpha > \lambda\frac{5\lambda\delta+4\delta^2}{2(\lambda-2\delta)} \tag{III.37}$$

III.8 Second Order Sliding Mode Control of a VSC Based HVDC Systems

After discussing the theoretical basis of second order sliding mode control, the control law will be driven for the VSC-HVDC system.

The control of this system must enable DC-bus voltage regulation as well as AC currents control for each substation and consequently the regulation of the active reactive powers flow.

III.8.1 Current Controller Design

For the purpose of line currents controller design, the following two surfaces need to be defined. The first surface is defined as function of the *d*-axis tracking error by:

$$S_{1k} = i_{idk} - i_{idrefk} \tag{III.38}$$

The second surface is defined as function of the *q*-axis tracking error by:

$$S_{2k} = i_{qk} - i_{qrefk} \tag{III.39}$$

The equivalent control design starts first by defining the sliding surfaces derivatives as follows:

$$\begin{aligned} S_{1k} &= \dot{S}_{1k} = 0 \\ S_{2k} &= \dot{S}_{2k} = 0 \end{aligned} \tag{III.40}$$

Using the first subsystem model equations, the derivatives of the two sliding surfaces can be written in the following form:

$$\begin{aligned} \dot{S}_{1k} &= f_{1k}(x) + g_{1k} u_{eqdk} - \dot{i}_{drefk} = 0 \\ \dot{S}_{2k} &= f_{2k}(x) + g_{2k} u_{edqk} - \dot{i}_{qrefk} = 0 \end{aligned} \tag{III.41}$$

with:

$$f_k(x) = \begin{bmatrix} f_{1k} \\ f_{2k} \end{bmatrix} = \begin{bmatrix} -\dfrac{R_k}{L_k} i_{dk} + \omega_k i_{qk} - \dfrac{v_{sdk}}{L_k} \\ -\dfrac{R_k}{L_k} i_{qk} - \omega_k i_{dk} - \dfrac{v_{sqk}}{L_k} \end{bmatrix}; g_k(x) = \begin{bmatrix} g_{1k} \\ g_{2k} \end{bmatrix} = \begin{bmatrix} -\dfrac{1}{L_k} & 0 \\ 0 & -\dfrac{1}{L_k} \end{bmatrix}$$

Setting $\dot{S}_{ik} = 0$, then the equivalent control law can be obtained as:

$$\begin{aligned} u_{eq1k} &= \frac{-f_{2k}(x) + \dot{i}_{qrefk}}{g_{1k}} \\ u_{eq2k} &= \frac{-f_{2k}(x) + \dot{i}_{qrefk}}{g_{2k}} \end{aligned} \tag{III.42}$$

The switching control law is designed based on the Super-Twisting algorithmas as follows:

$$\begin{aligned} u_{sw1k} &= -\lambda_{ik} \left|S_{1k}\right|^{\frac{1}{2}} sign(S_{1k}) - \int \alpha_{ik} sign(S_{1k}) dt \\ u_{sw2k} &= -\lambda_{ik} \left|S_{2k}\right|^{\frac{1}{2}} sign(S_{2k}) - \int \alpha_{ik} sign(S_{2k}) dt \end{aligned} \tag{III.43}$$

Where α_k and λ_k are positive constants

The final second order sliding mode control is then given by:

$$\begin{aligned} v_{drefk} &= \frac{-f_{1k}(x,t) + \dot{i}_{drefk}}{g_{1k}} - \lambda_{ik} \left|S_{1k}\right|^{\frac{1}{2}} sign(S_{1k}) - \int \alpha_{ik} sign(S_{1k}) dt \\ v_{qrefk} &= \frac{-f_{2k}(x) + \dot{i}_{qrefk}}{g_{2k}} - \lambda_{ik} \left|S_{2k}\right|^{\frac{1}{2}} sign(S_{2k}) - \int \alpha_{ik} sign(S_{2k}) dt \end{aligned} \tag{III.44}$$

III.8.2 DC-link Voltage Controller Design

The third surface is that of DC-link voltage; the sliding surface is defined as:

$$S_{dc} = v_{dc2} - v_{dcref\,2} \tag{III.45}$$

Therefore, the time derivative of the sliding surface S_{dc} is:

$$\dot{S}_{dc} = v_{dc2} - \dot{v}_{dcref\,2} \tag{III.46}$$

Setting $\dot{S}_{dc}=0$, then the equivalent control law can be obtained as:

$$u_{eqdc}=\frac{-f_{dc}(x)+\dot{v}_{dcref\,2}}{g_{dc}(x)} \tag{III.47}$$

where:

$$f_{dc}(x)=-\frac{i_{line}}{C}\ ;\ g_{dc}(x)=\frac{v_{sdk}}{Cv_{dck}}$$

The switching control law is designed based on the Super-Twisting algorithm as follows:

$$u_{swdc}=-\lambda_{dc}\left|S_{dc}\right|^{\frac{1}{2}}sign(S_{dc})-\int\alpha_{dc}sign(S_{dc})dt \tag{III.48}$$

where α_{dc} and λ_{dc} are positive constants.

The final control law can be obtained as follows:

$$i_{dref\,2}=\frac{-f_{dc}(x)+\dot{v}_{dcref\,2}}{g_{dc}(x)}-\lambda_{dc}\left|S_{dc}\right|^{\frac{1}{2}}sign(S_{dc})-\int\alpha_{dc}sign(S_{dc})dt \tag{III.49}$$

III.9 Second Order SMC of Point-to-Point VSC-based HVDC System

III.9.1 Point-to-Point VSC-based HVDC Second Order SMC Scheme

The figure (III.23) presents a Point-to-Point VSC-HVDC system and its second order sliding mode control scheme block diagram.

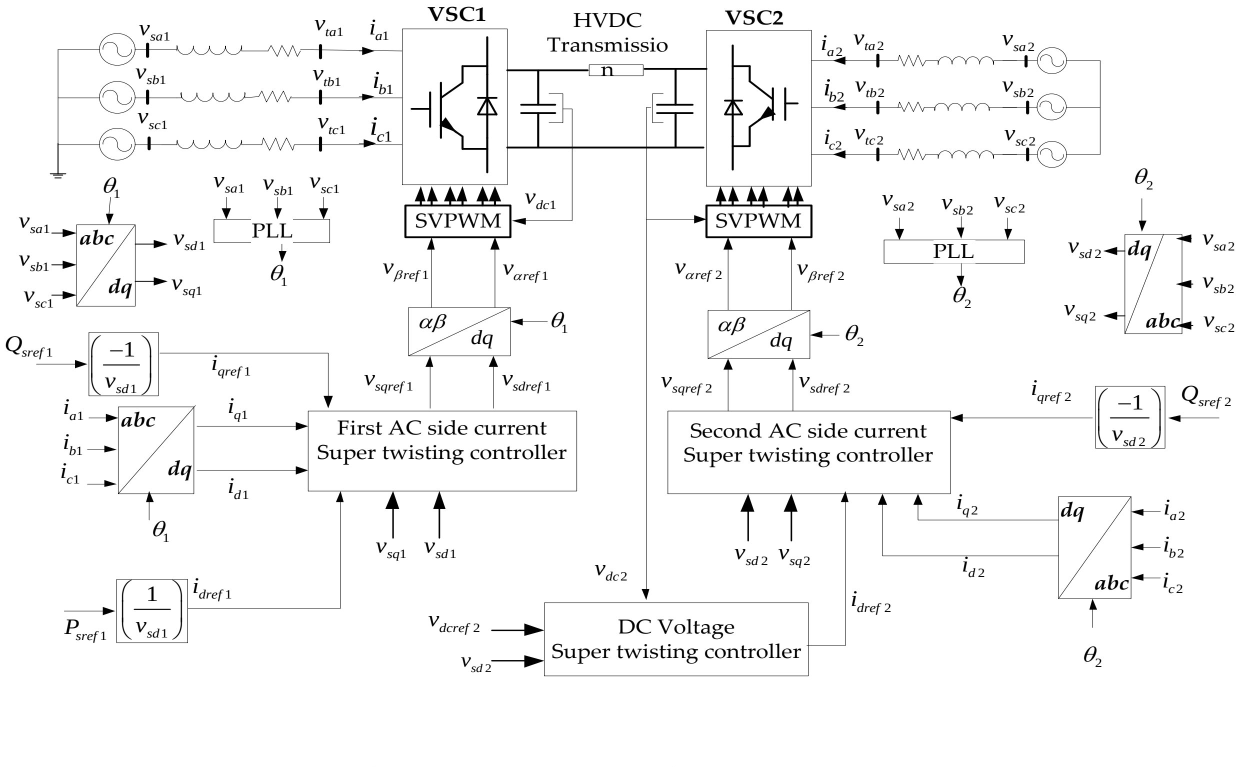


Figure (III.23): Block diagram of the second order SMC of VSC-based Point-to-Point HVDC system.

III.9.2 Second Order SMC Based Point-to-Point VSC-based HVDC Simulation

To validate and analyze the performance of the super twisting algorithm controller on the VSC based HVDC transmission system, the system was implemented in Simulink/Matlab environment using the same parameters given in Appendix A.

To analyze the performance of the designed control system, the same tests adopted in the previous sections of this chapter will be performed

Figure (III.24) presents the active and reactive powers at each AC side of both terminals.

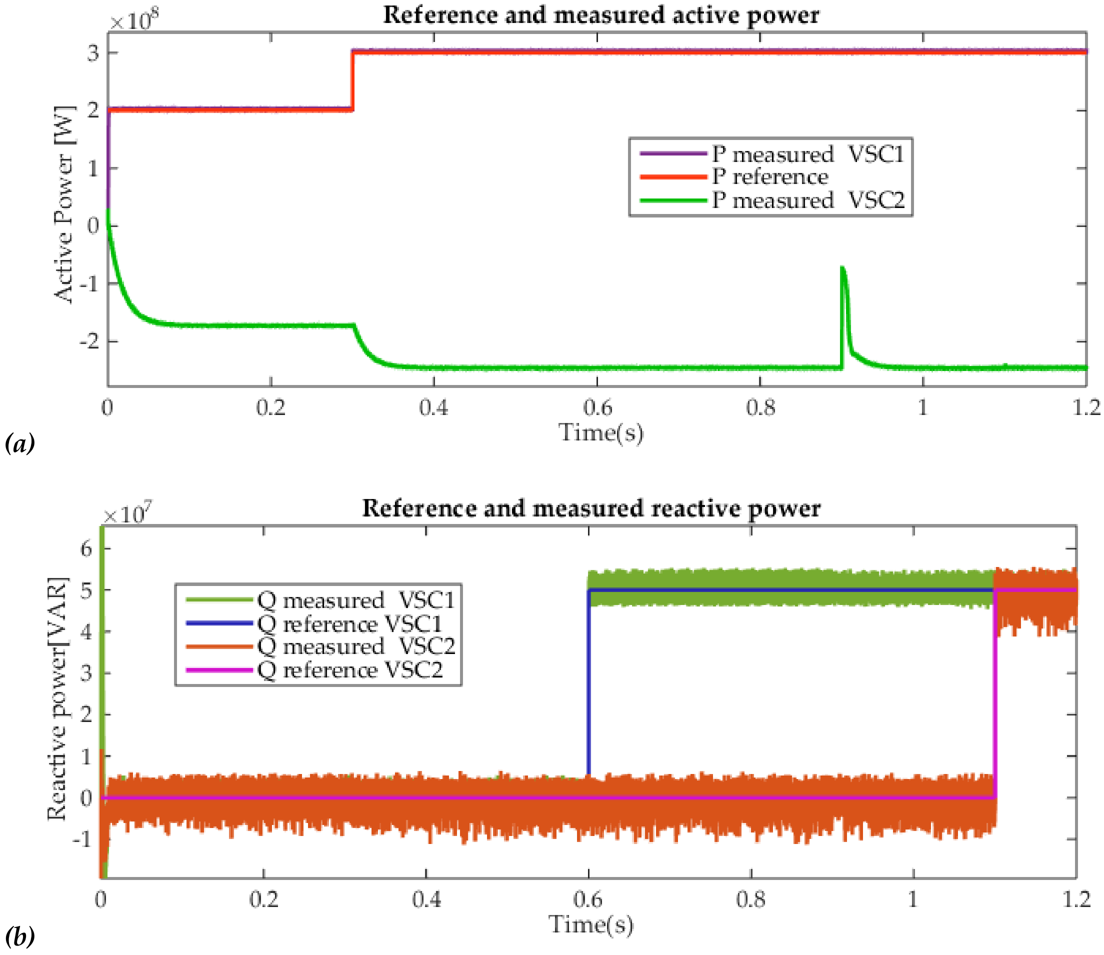


Figure (III.24): Reference and measured powers of VSC1 and VSC2 terminals: (a) active powers, (b) reactive powers

Figures (III.24) presents the reference and measured active and reactive powers at each AC side of both terminals. The active and reactive powers stabilize at their reference values after a short transient. Moreover, it can be observed that only the active power of the VSC2 AC side spikes at t=0.9s for a short instant of time due to the change in the DC voltage where the other measured powers are clean from any transients or overshoots.

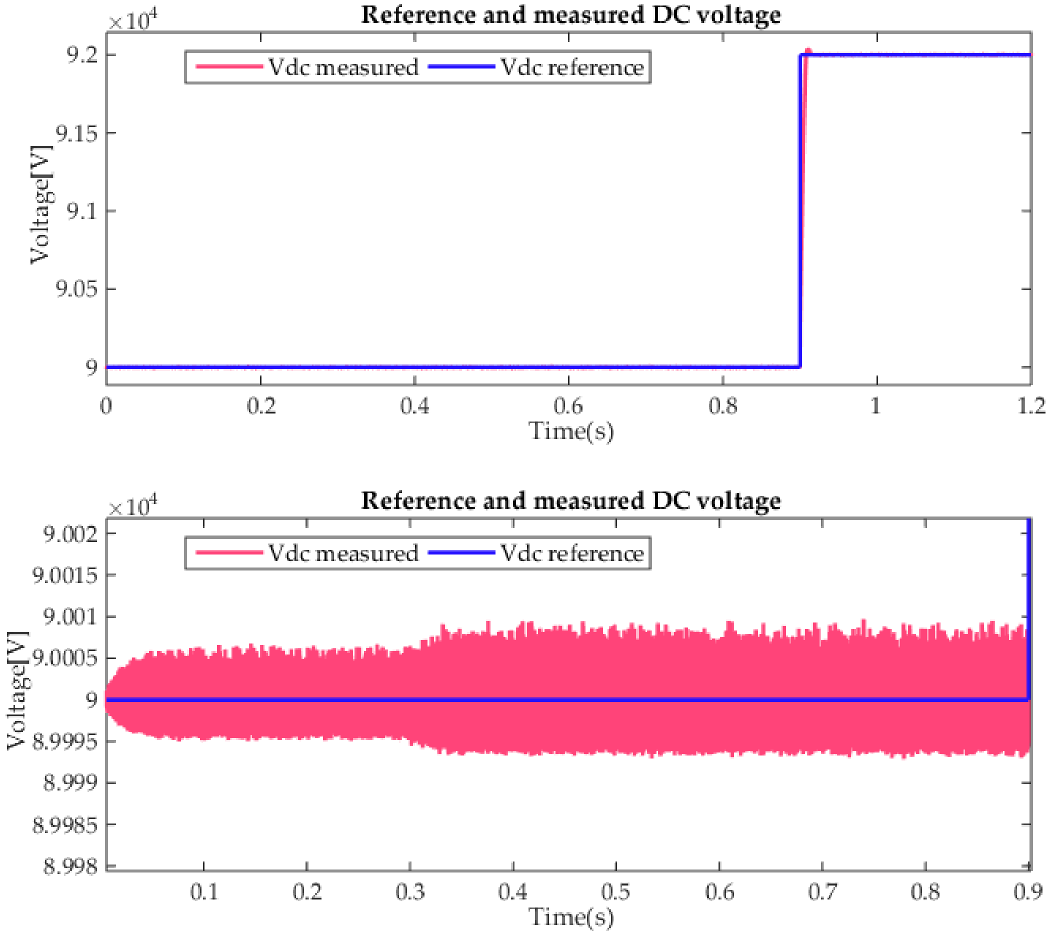
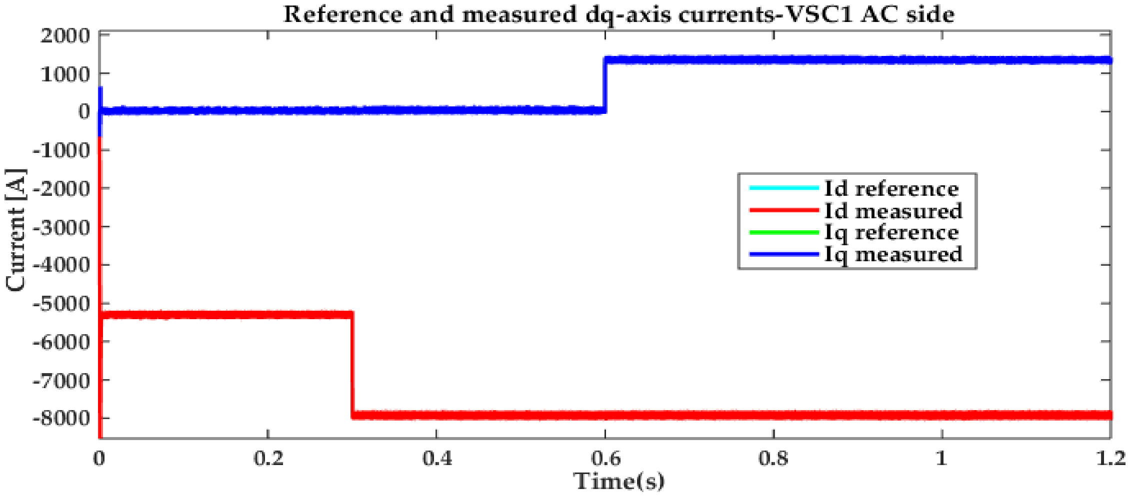
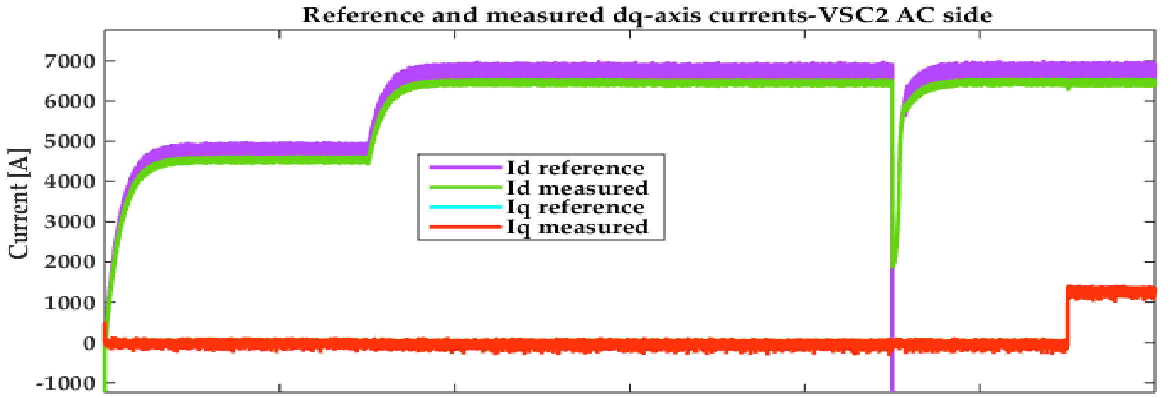


Figure (III.25): Reference and measured DC voltage

Figure (III.25)shows the response of the VSC2 DC voltage. As it can be observed from this plot, the DC voltage tracks accurately and almost perfectly its reference with no transient and overshoot.



(a)



(b)

Figure (III.26): Reference and measured *dq*-axes currents: (a)VSC1 AC side currents, (b) VSC2 AC side currents.

Figure (III.26) represents the changes of the *dq*-axes currents while following their predetermined reference values during the start transient as well as in the steady-state. At the moment of DC voltage change a spike appears in the current active component.

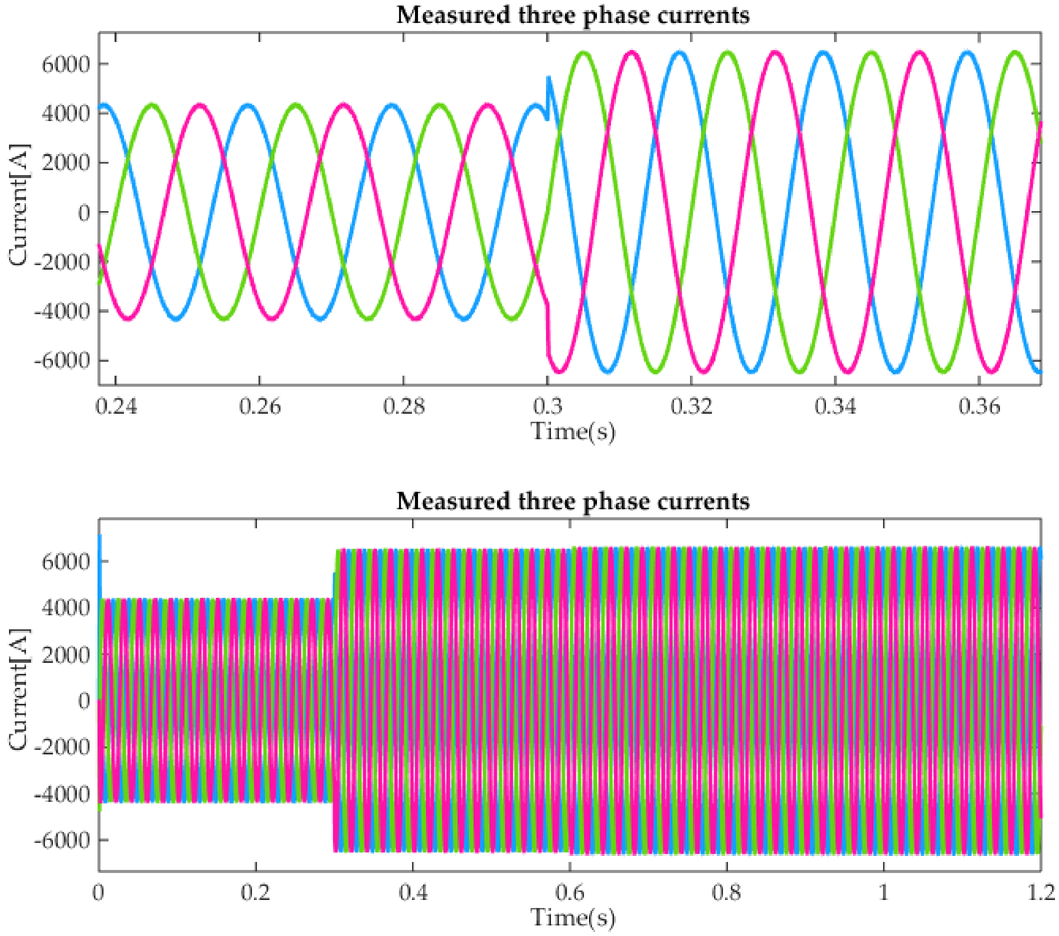


Figure (III.27): VSC1 AC side three phase currents

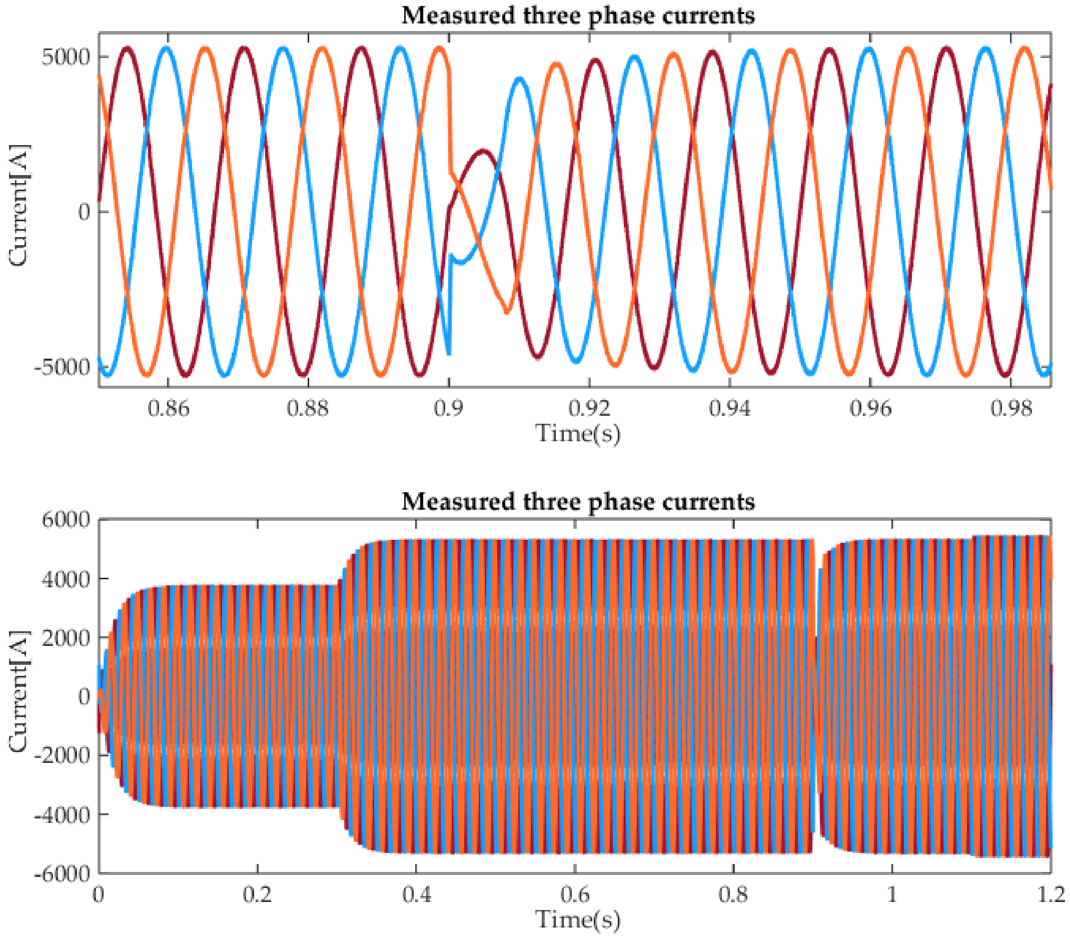


Figure (III.28): VSC2 AC side three phase currents

In Figures (II.27) and (II.28), the phase currents at the two ends of both converter AC sides are shown. As it can be observed both currents has almost clean sinusoidal waveforms but with two different frequencies.

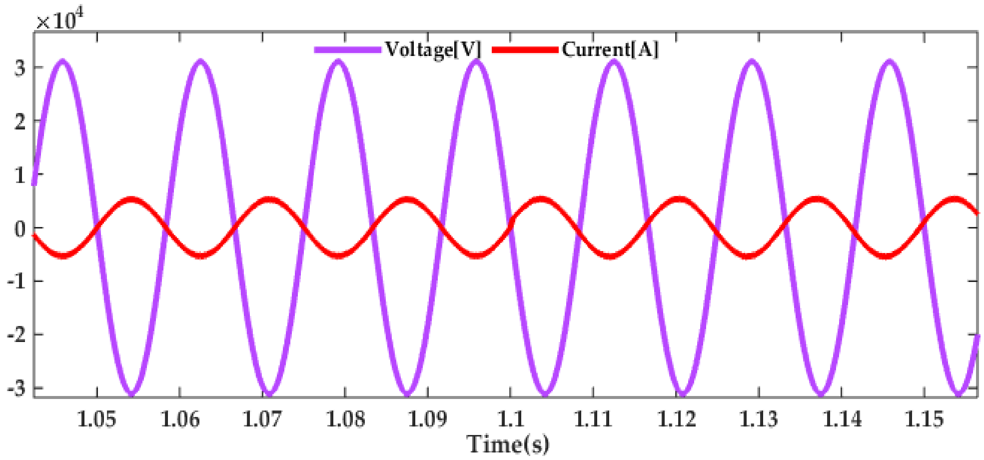
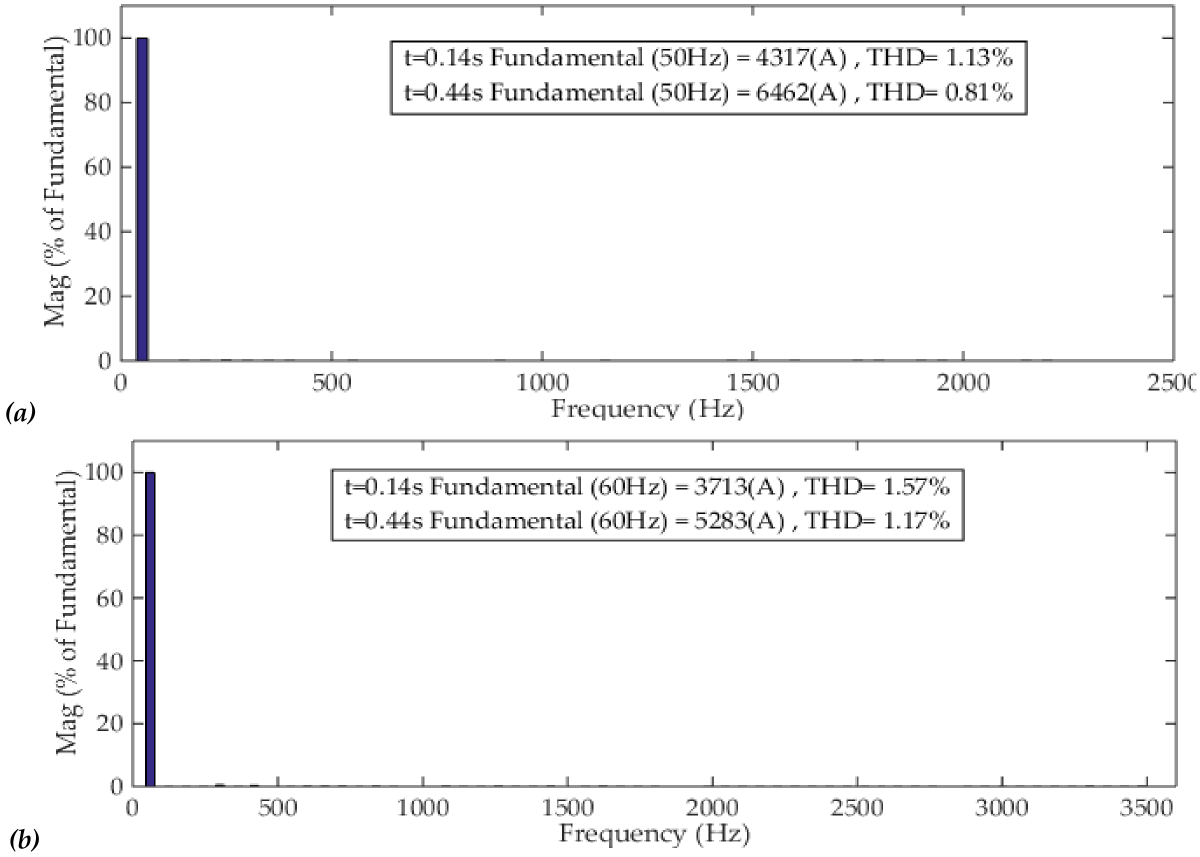


Figure (II.29): VSC2 AC side measured phase voltage and current

As can be observed from Figure (III.29), the waveform of the output phase voltage and current at the VSC2 AC side are in phase thus signifying a unity power factor. until the instant t=1.1s at which the injected reactive power change reference from 0VAR to 50MVAR. it can be noted that the waveform of the current is leading compared to the measured voltage.



Figure(III.30):Line currents harmonic spectra: (a) VCS1 AC side currents, (b) VCS2 AC side currents

The currents harmonic spectra given through the figure (III.30) show that the sinusoidal current waveforms have low values of total harmonic distortion ranging from 1.57% and 1.13% to 1.17% and 0.81% for VSC2 and VSC1 line currents, respectively.

III.10 Second Order SMC of Back-to-Back VSC-based HVDC System

III.10.1 Back-to-Back VSC-based HVDC Second Order SMC Scheme

Figure (III.31) shows a VSC-HVDC system with back-to-back configuration and its second order sliding mode control design block diagram. This system is nearly identical to the one employed in the previous section apart from that the transmission line is not included.

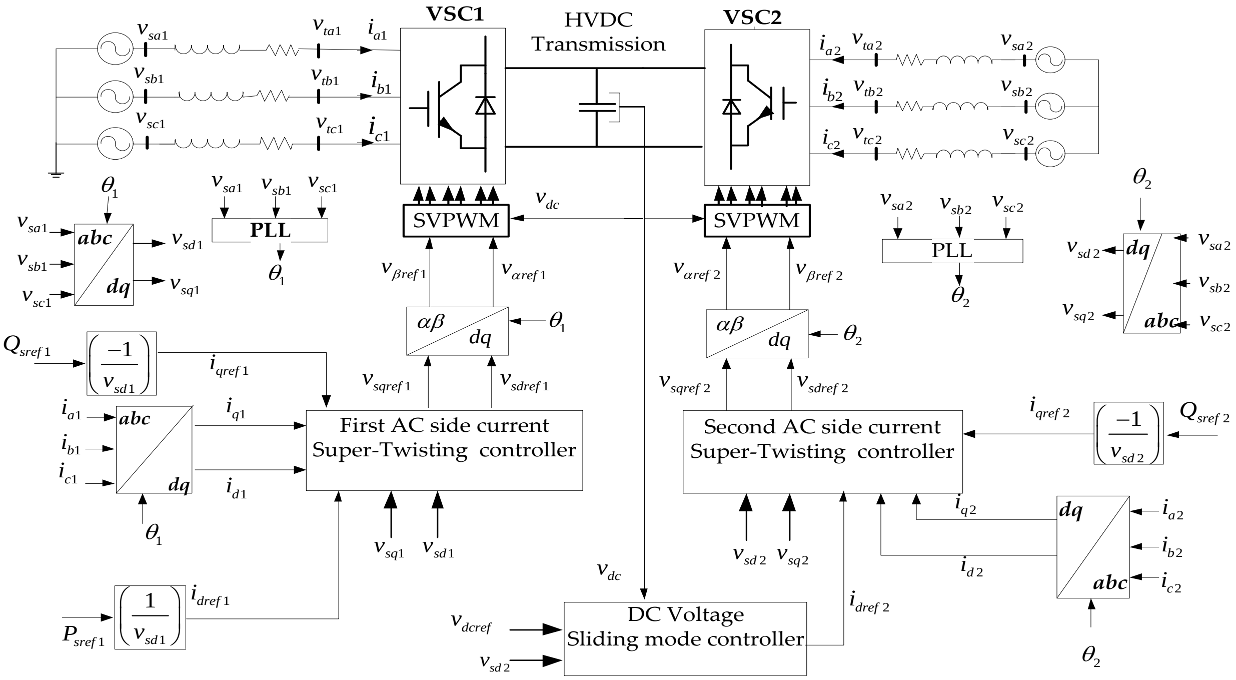
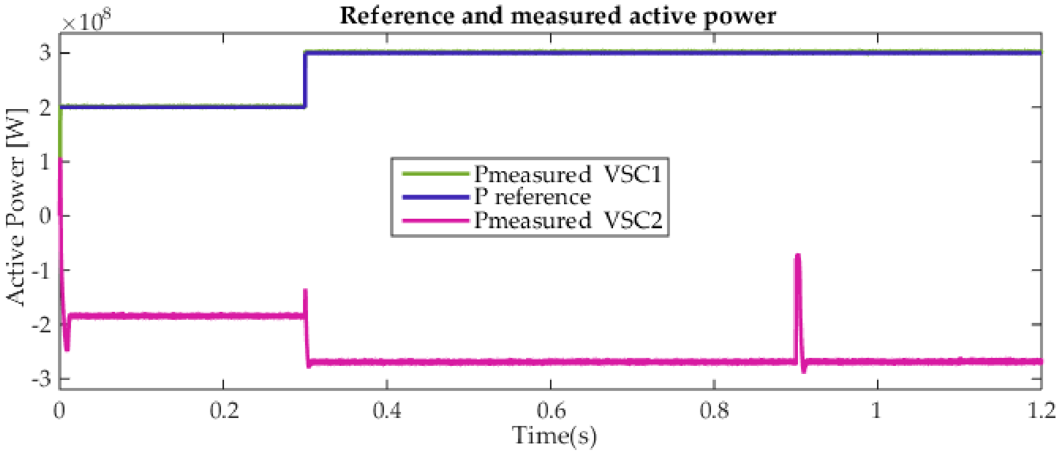


Figure (III.31): Block diagram of the second order SMC of VSC-based back-to-back HVDC system.

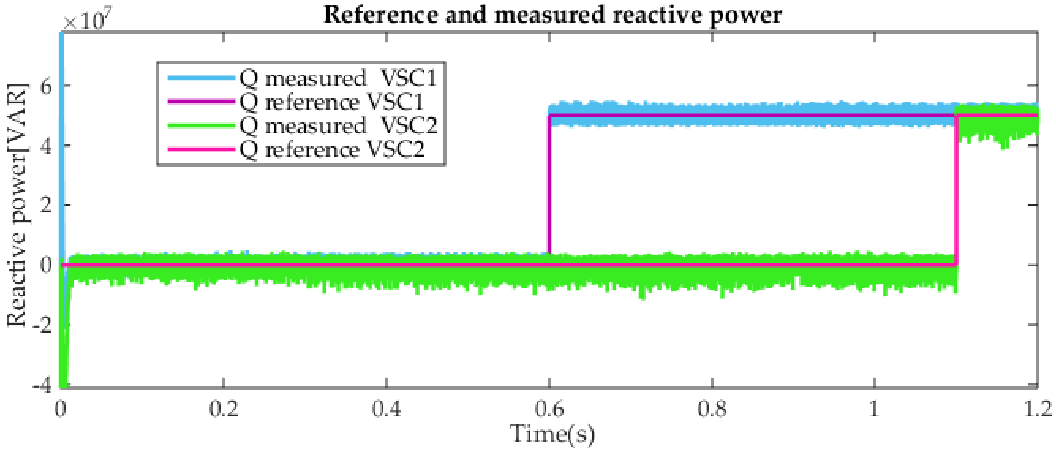
III.10.2 Second Order SMC Based Back-to-Back VSC-based HVDC Simulation

The objective of this section is to analyze the performance of the VSC-based back-to-back HVDC system control when transmitting power between two asynchronous networks, in which the first terminal is operating at 50 Hz and the second one at 60 Hz. These two terminals are controlled by super twisting controllers.

Figure (III.32) presents the active and reactive powers at each AC side of both terminals. As the plots reveal, the active and reactive powers at both ends of the converters are maintained constant at their predetermined reference during the steady-state operation. However, during a brief instant of time the active and reactive powers experience a spike due to the change in the DC voltage.



(a)



(b)

Figure (III.32): Reference and measured powers of VSC1 and VSC2 terminals: (a) active powers, (b) reactive powers

Figure (III.33) shows that the DC voltage matches its reference value with high precision after a short start transient regime. It can be observed at t=0.3s a less than 0.01% spike appears due to the change in the injected active power.

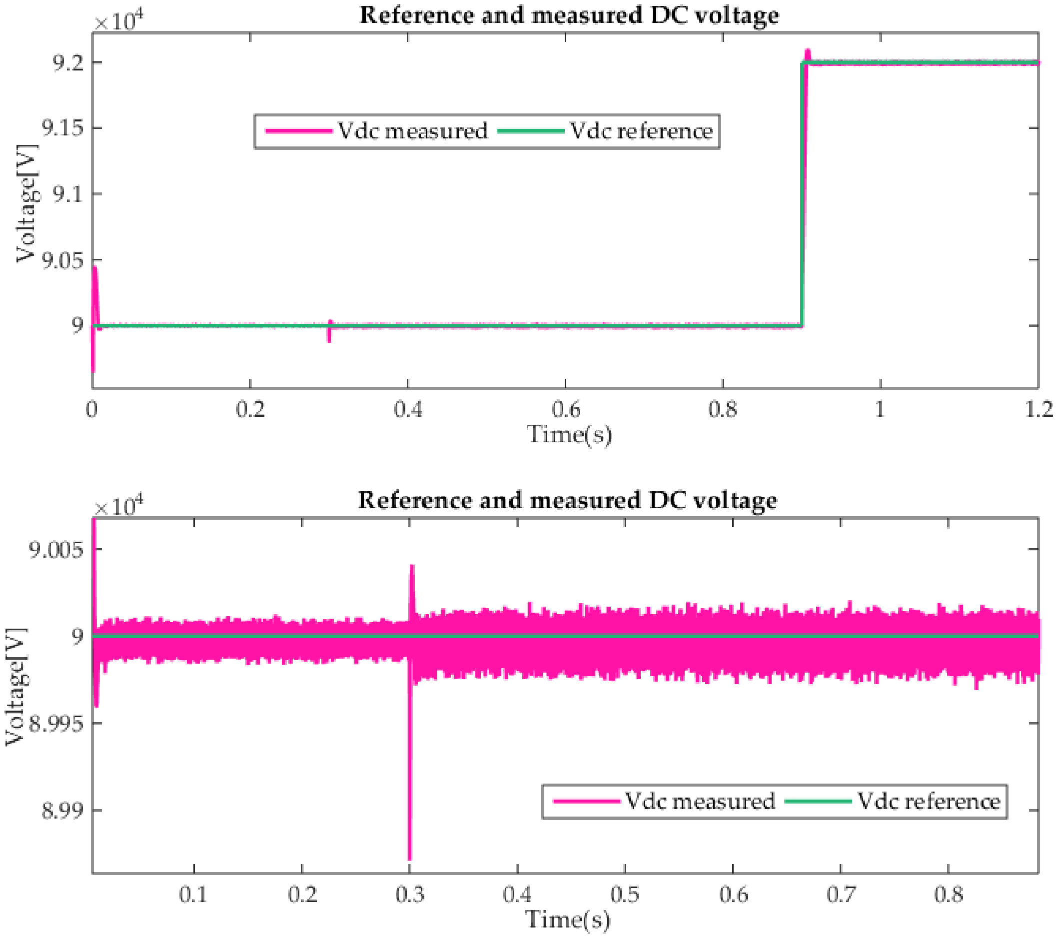


Figure (III.33): Reference and measured DC voltage

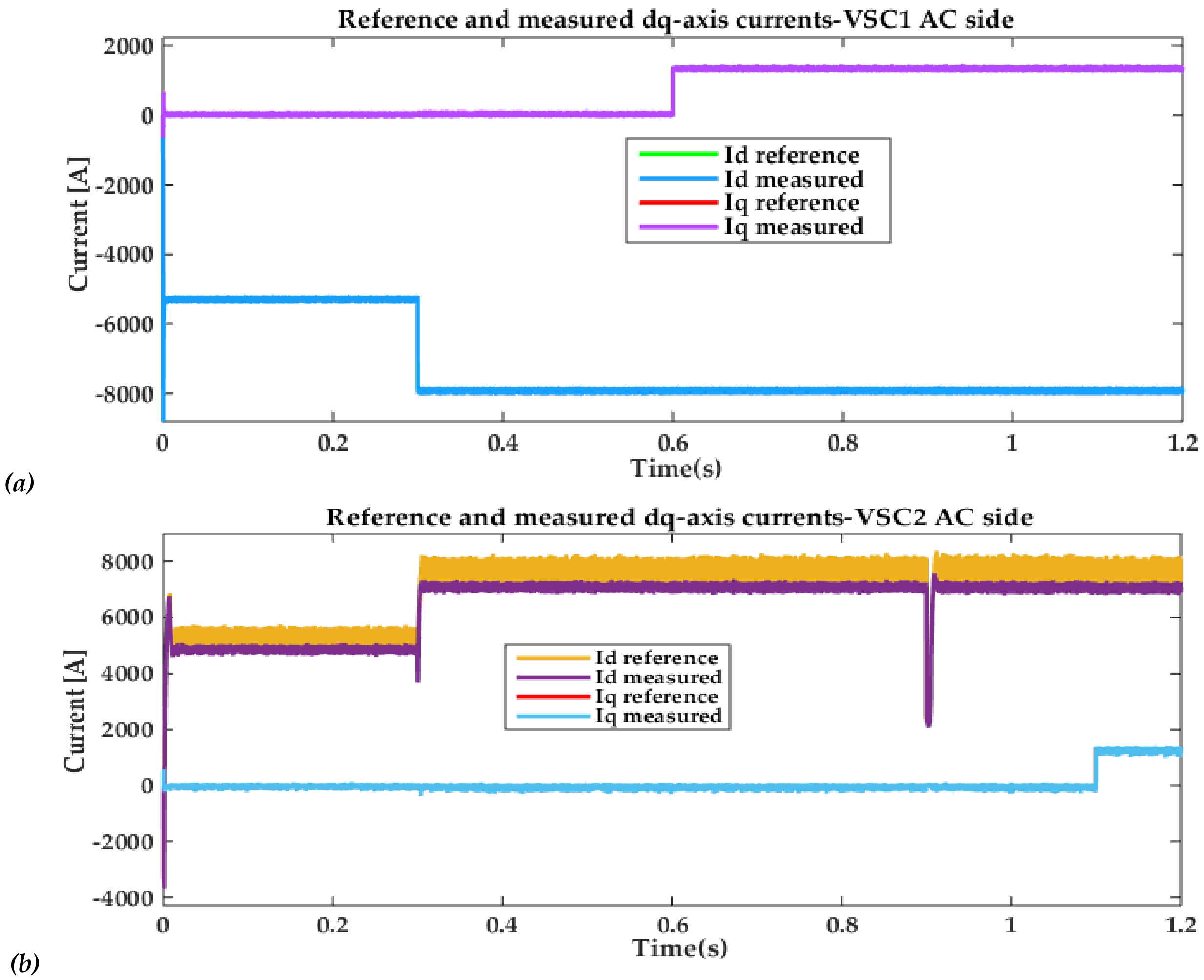
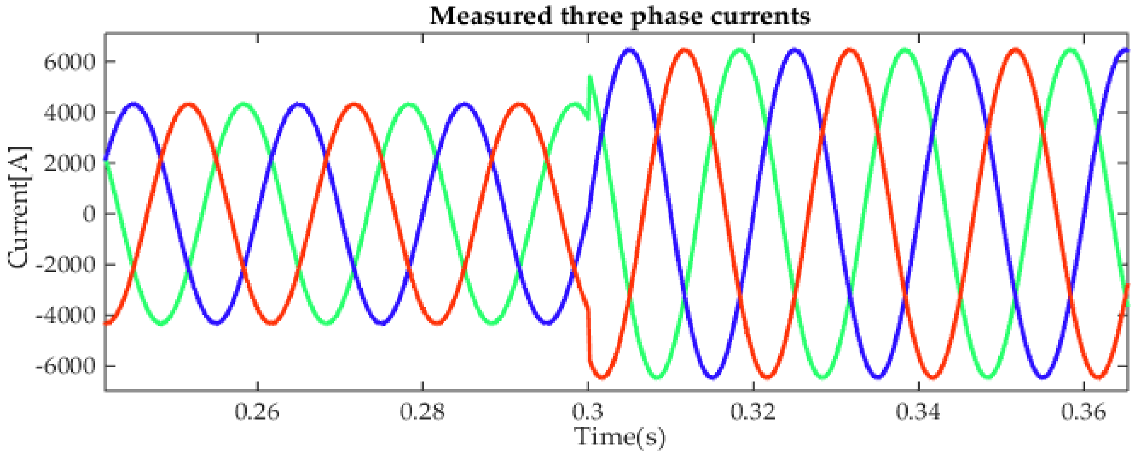


Figure (III.34): Reference and measured *dq*-axes currents: (a)VSC1 AC side currents, (b) VSC2 AC side currents.

The current *dq*-axes components at both ends of the HVDC system are plotted in Figure (III.34). From these plots it can be seen that the measured signals track very well their reference signals. The active current sudden decrease produced at t=0.9s is caused by the change in DC voltage. Interestingly, the *d*-axis current settles fast after the transient ends.



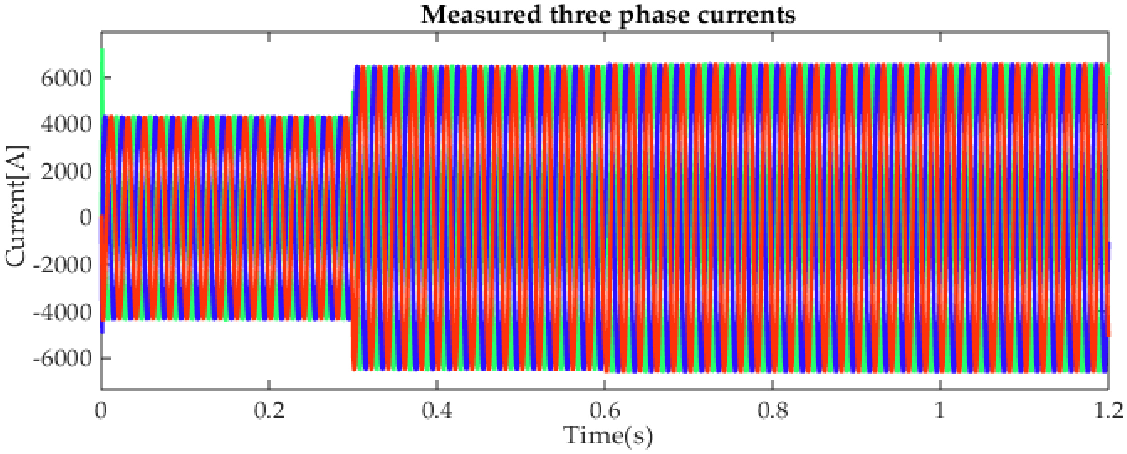


Figure (III.35): VSC1 AC side three phase currents

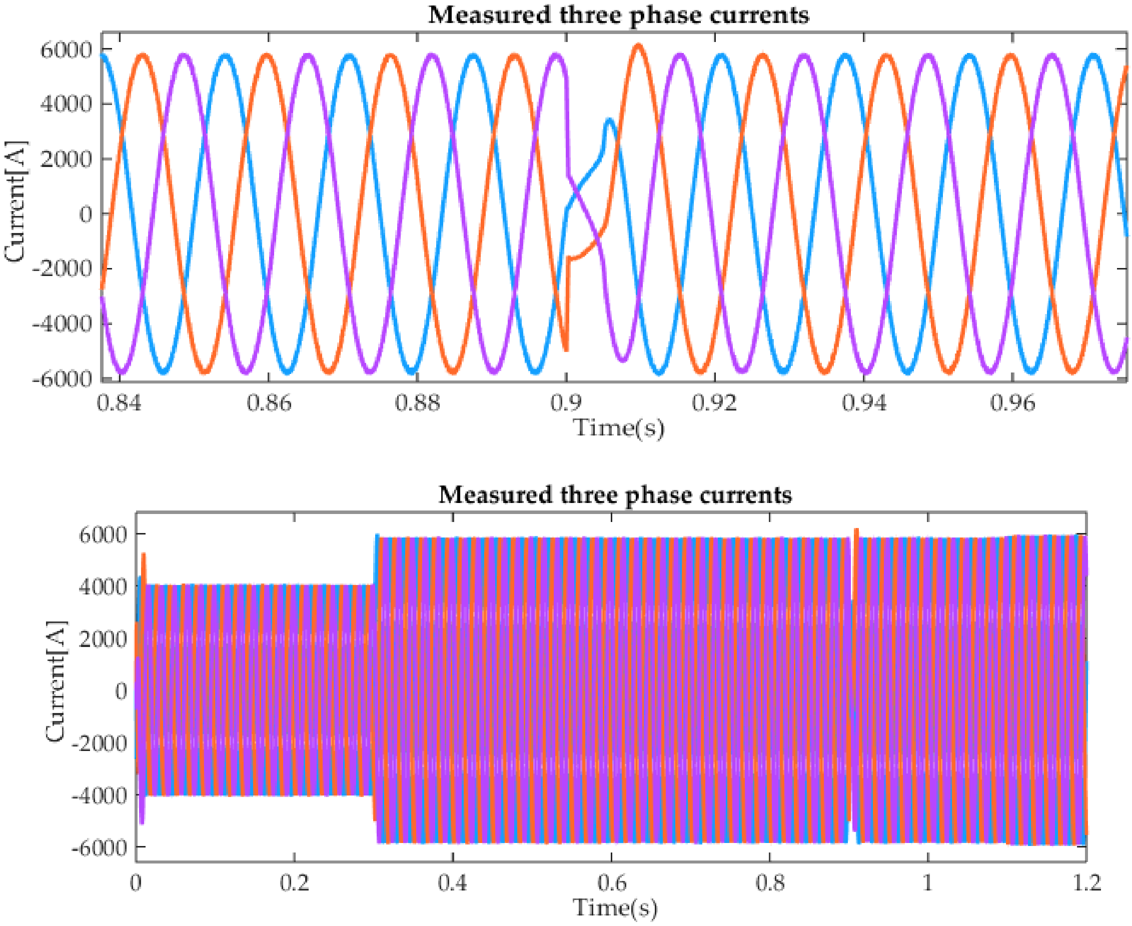
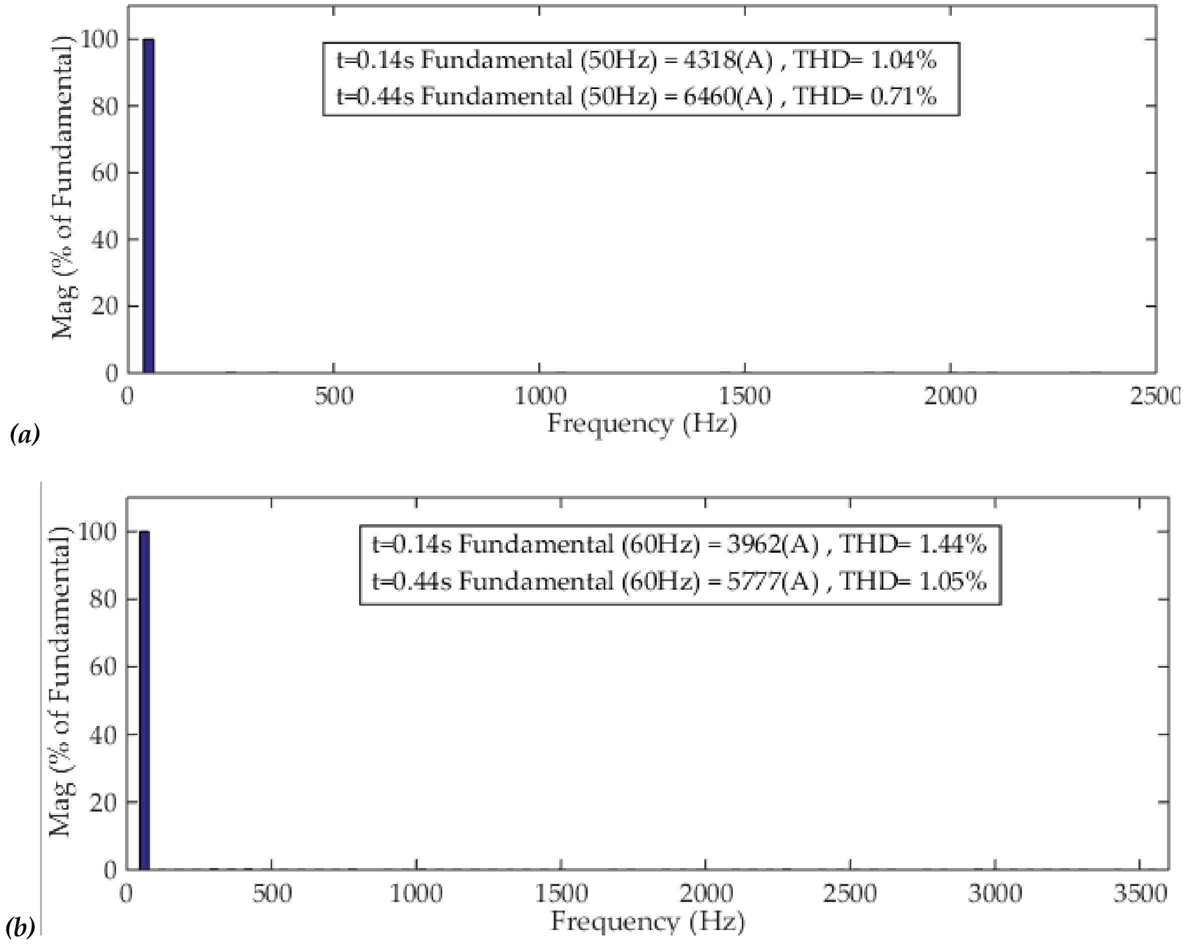


Figure (III.36): VSC2 AC side three phase currents

The phase currents at the AC sides of the HVDC are shown in Figures (III.35) and (III.36). These figures are showing a nearly pure sinusoidal waveform generated at both ends at different frequencies. By comparing these plots no differences in the dynamics of the currents can be seen except the transient that appears at the VSC2 side due to change in the DC voltages, which effects in its turn the active power.

Consequently, the synchronization and the power transfer between the two grids operating at different frequencies are well achieved.



Figure(III.37):Line currents harmonic spectra: (a) VCS1 AC side currents, (b) VCS2 AC side currents

Figure (III.37) shows the line currents harmonic spectra where the total harmonic distortion (THD) varies between 1.44% and 1.04% before the variation of the active power reference and 1.05% and 0.71% after its variation for VSC2 and VSC1, respectively. The obtained THD values are less than 5%, which is in agreement with IEEE 519 standard.

III.11Comparative Study between the First and Second Orders SMC

III.11.1 Point-to-Point VSC-based HVDC Configuration

As it appears in Figure(III.38) the super twisting algorithm(STA) control scheme enhanced the performance of the controller against the chattering even during the injected active power increase at t=0.3s; the chattering is still reduced in the STA compared to the SMC. On the other hand, at t=0.9s the instant where the DC voltage reference changes the STA has a more robust response than the first order SMC. What is more is the rapid response of DC voltage using STA compared to that obtained by first order SMC.

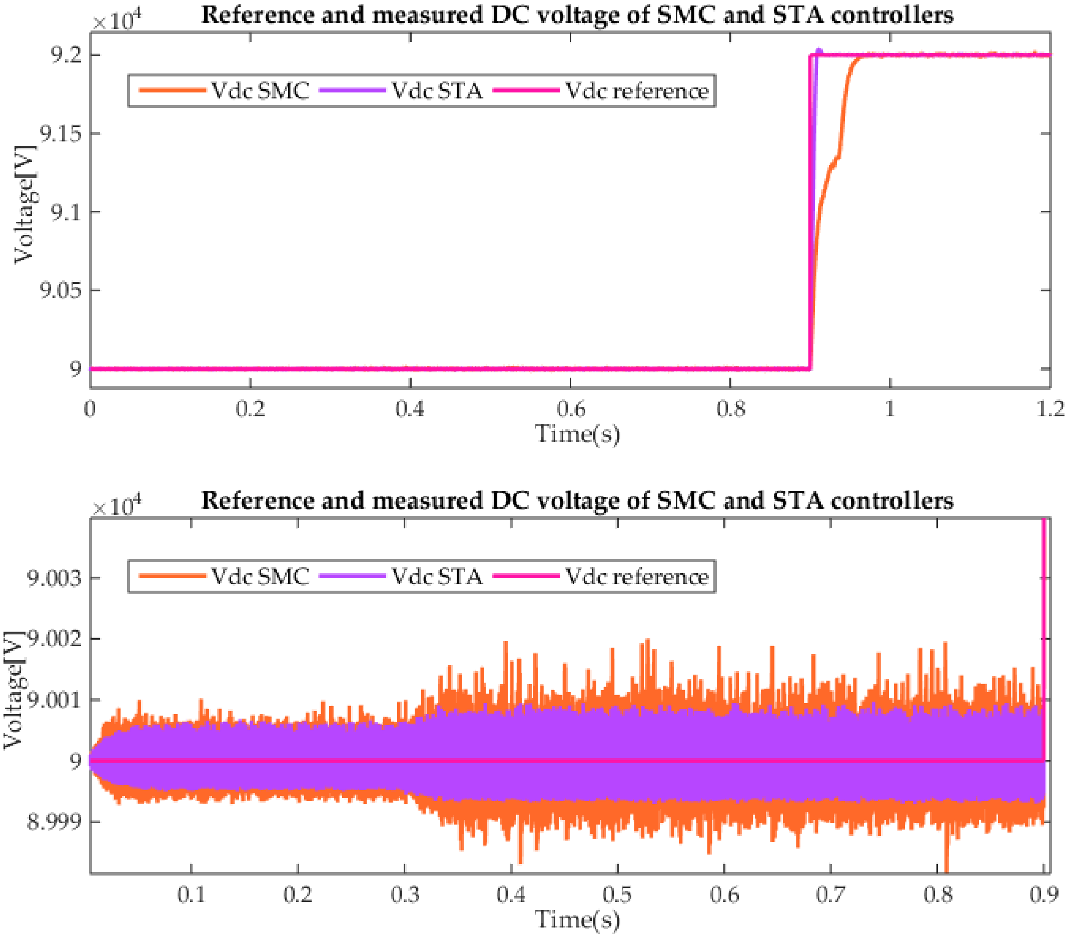
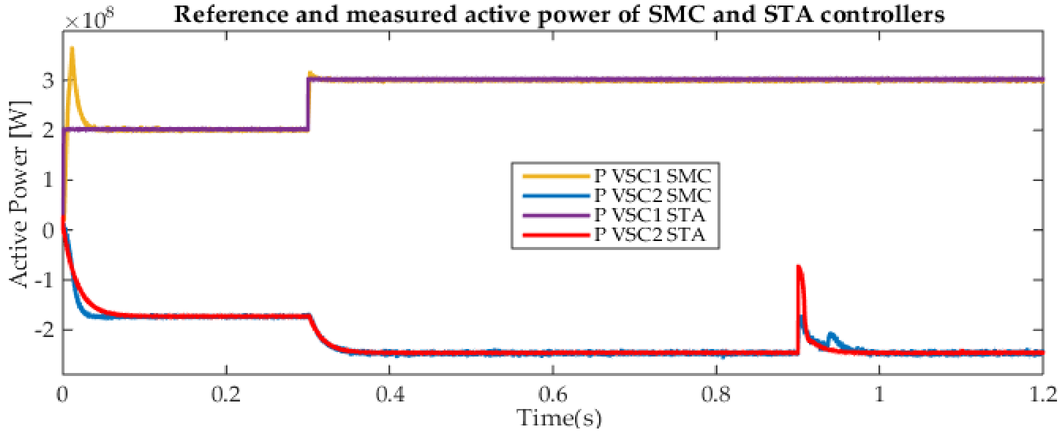
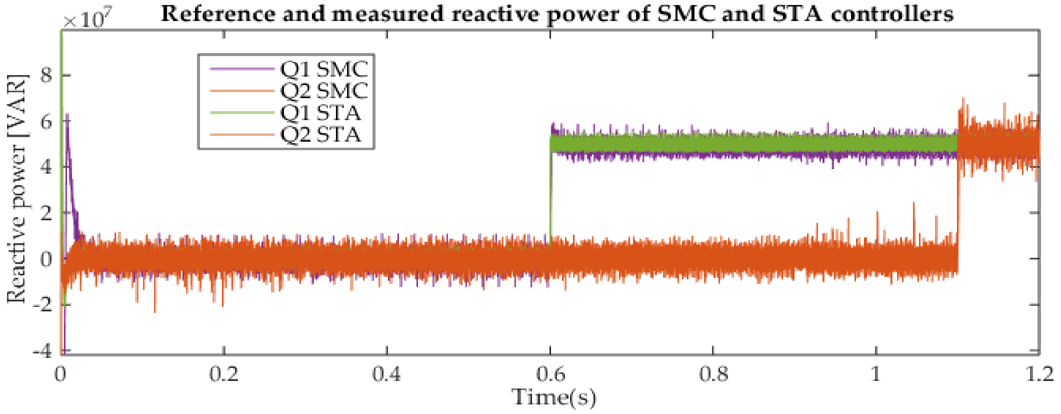


Figure (III.38): Reference and measured DC voltage

Figure (III.39) presents the active and reactive powers at each AC side of both terminals with both controllers. From power curves, there is less chattering using STA compared to the first order SMC case. At t=0.9s,after a brief transient on the VSC2 side, the active power response takes a larger overshoot using STA regulator than that using SMC one, but with reduced time response.



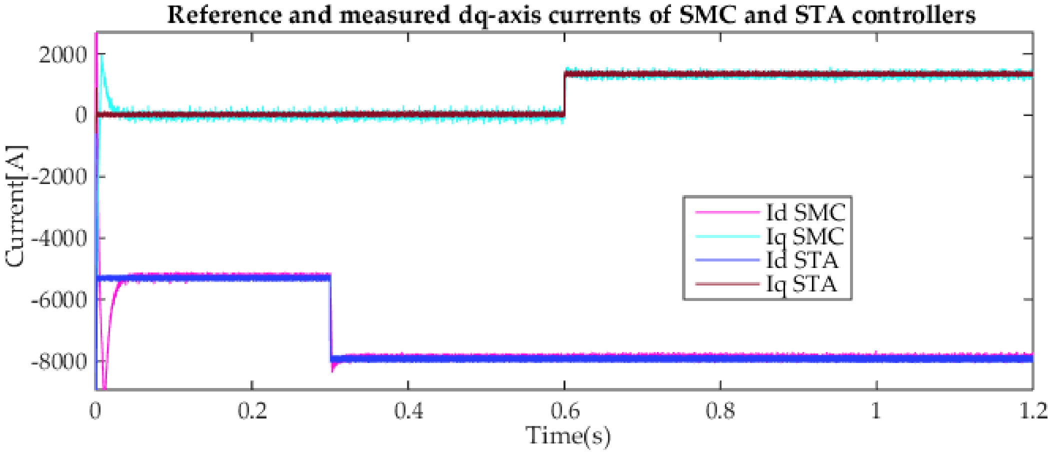
(a)



(b)

Figure (III.39): Reference and measured powers of VSC1 and VSC2 terminals: (a) active powers, (b) reactive powers

Figure (III.40) depicts the variations of the *dq*-axes currents of each converter using both control strategies. The use of STA to control the VDC1 terminal leads to much better responses in terms of convergence time and overshoot compared to those using first order SMC control. On the VSC2 side, after a relatively quick start transient, both controllers are effective in forcing the *dq*-axes currents to follow their references. In this, the SMC has faster responses, and most importantly the STA presents less chattering.



(a)

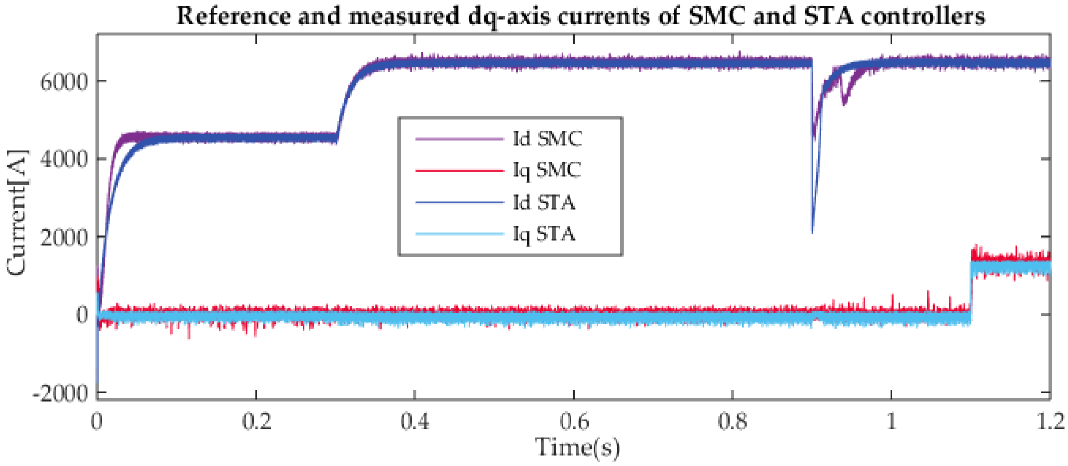


Figure (III.40): Reference and measured dq-axes currents: a)VSC1 AC side currents, b) VSC2 AC side currents.

III.11.2Back-to-Back VSC-based HVDC Configuration

According to Figure (III.41), using STA controller, the DC voltage has a better performance compared to the first order SMC controller in terms of transient rejection both at the start and at t=0.3s. Also, a t=0.9s, the STA leads to a DC voltage response without overshot and less chattering unlike the SMC controller.

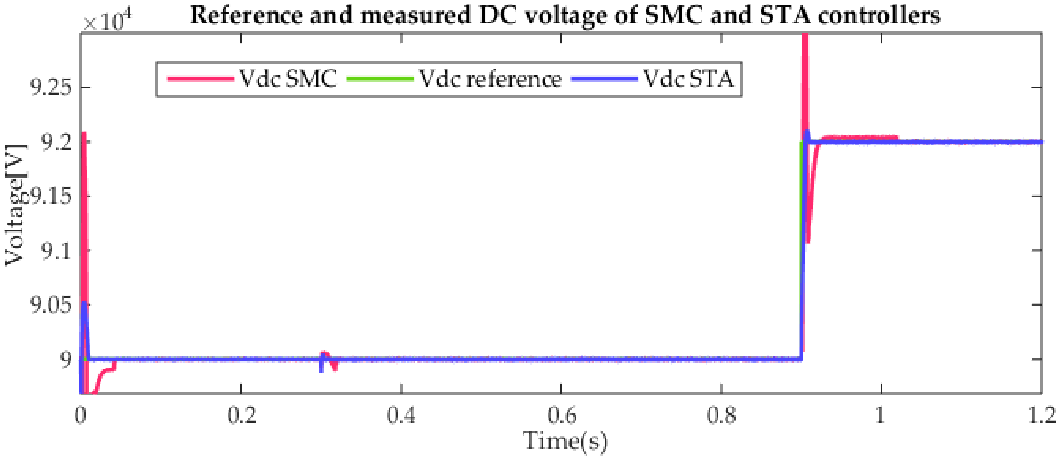


Figure (III.41): Reference and measured DC voltage out of SMC and STA controllers.

Figure (III.42) displays the active and reactive powers at each AC side of both terminals with both regulators. The VSC1 powers responses using STA have fewer chattering with nearly accurate reference tracking compared to the SMC controller. Furthermore, at t=0.9s, following a short transient occurs at the VSC2 side, the powers responses are perturbed with both SMC and STA regulators. However, the power spikes using STA are much smaller than those using SMC with faster responses.

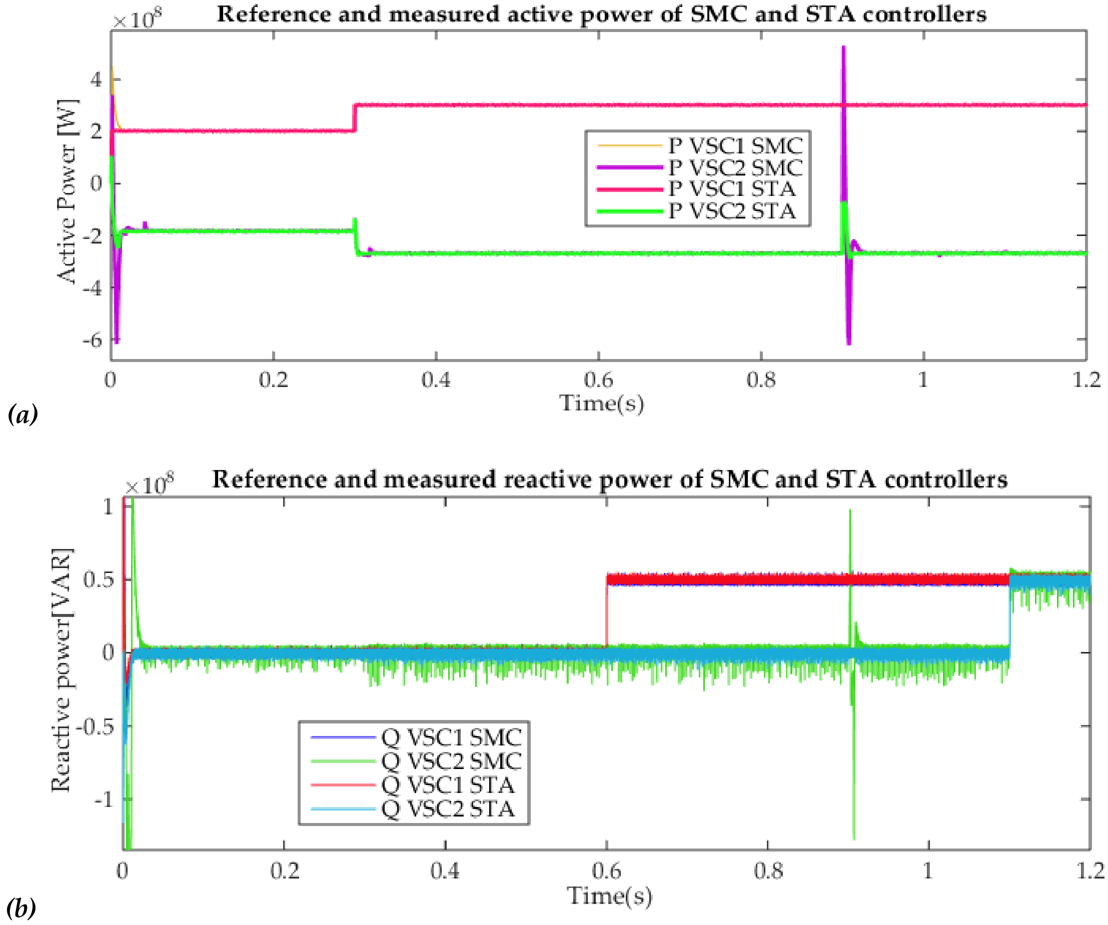
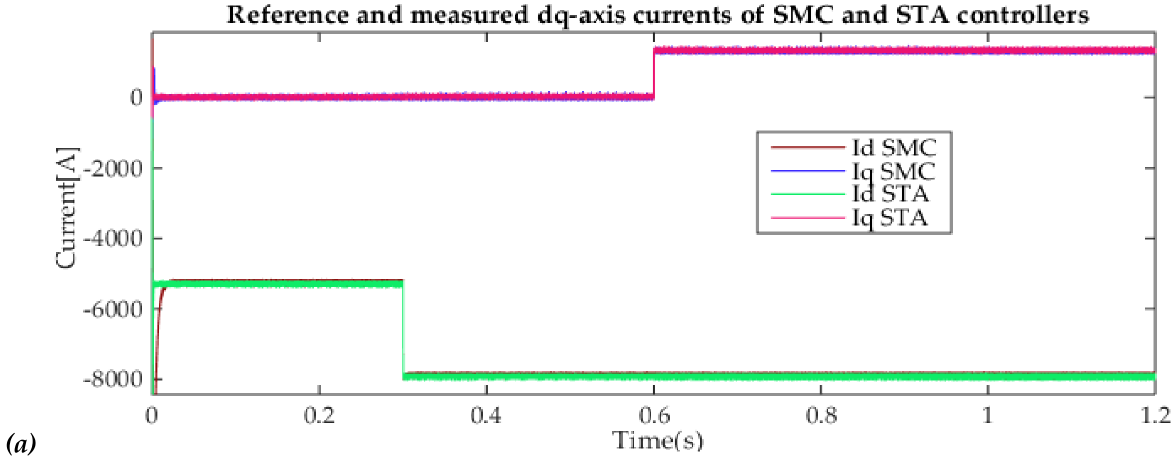
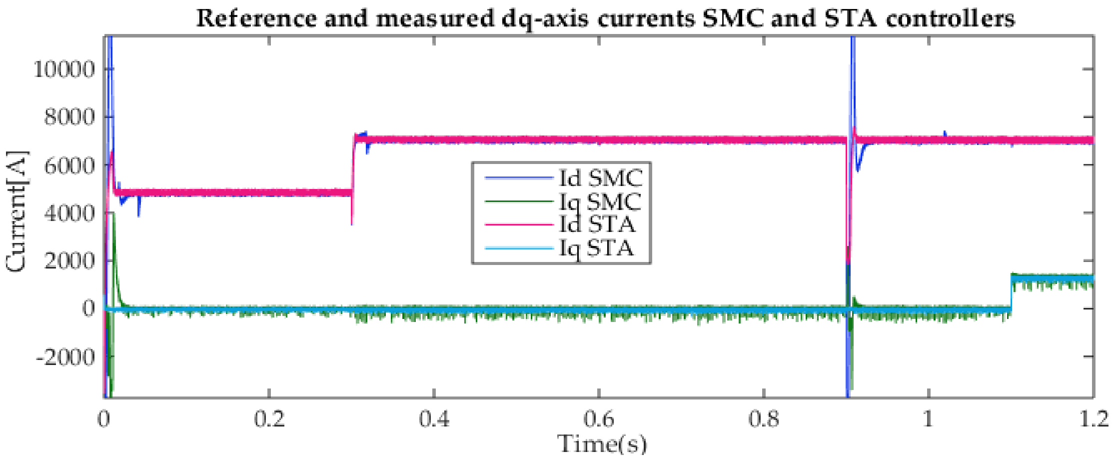


Figure (III.42): Reference and measured powers of VSC1 and VSC2 terminals: (a) active powers, (b) reactive powers

The *dq*-axes currents of each converter employing both controllers are shown in Figure (III.43). Again, the STA controller outperforms its counterpart first order SMC in terms of transient mastering and chattering reduction.





(b)

Figure (III.43) Reference and measured dq-axes currents: (a)VSC1 AC side currents, (b) VSC1 AC side currents.

III.12 Conclusion

This chapter reports the VSC-HVDC systems control schemes based on the concepts of the first order SMC and a second order SMC using super twisting algorithm. These control structures are applied on both point-to-point and back-to-back HVDC system topologies. For this end, the first part of this chapter is devoted to, after a short introduction to the first-order SMC theory, the design of appropriate 1-SMC controllers. In order to overcome the phenomenon of chattering, which manifests itself in the classic SMC, the same points previously cited are involved in the second part of this chapter accept 2-SMC controllers are used instead of 1-SMC controllers.

Simulation results show the effectiveness of the proposed2-SMC, which provides good pursuit of active and reactive powers as well as the DC-link voltage with quickly responses and almost free of chattering effect. Furthermore, the comparative study confirms that the two techniques 1-SMC and STA based 2-SMC bring remarkable improvements compared to the classic PI controller. Indeed, the STA control, particularly, offers good static and dynamic performances in terms of stability, speed, and precision. This has manifested, besides chattering effect reduction, in good reference tracking with shorter response time and no noticeable overshoot.

Chapter IV

SIL and PIL Simulation of Second Order SMC of HVDC Systems

IV.1.Introduction

The ever increasing demand for electrical power has somewhat been a push for greater integration of renewable energy, such as wind and solar energy. With the advancement in power electronics, VSC based HVDC transmission is taking over as the main choice for connecting the existing grids with far offshore or remote locations, thus minimizing the losses during transmission. The VSC based HVDC represents relatively complex electronic circuits, in which, processors performing all control algorithms, using a set of instructions in a specific language, e.g. MCU/DSP (C, C++), FPGA/ASIC (VHDL, VERILOG), and PLC (Structured Text), are used. As the rapid development of such complex systems, it is crucial to ensure high-quality control[63]. For this reason, digital simulation and laboratory measurement equipment were invented to help with the design and testing, in which each component is physically prototyped. However, due to the development risks and complexity of the before-mentioned systems make them physically hard, time-consuming furthermore financially costly to be conventionally tested.

Additionally, the hardware implementation of those controllers is not simple, although if these complicated systems can be realized by simulation tools like Simulink or PSIM. Nevertheless, once the hardware implementation takes place in digital devices like microcontroller, microprocessor, DSP and FPGA with handwritten code, numerous bugs can occur due to either the mismatches that can arise between the software and the specifications throughout the development process or considering that all the components used are real (DC/AC converter, sensors, actuators, and DSP). Therefore if a fault occurs, it is challenging to know accurately the responsible party of this defect. A research conducted in [64] discovered that a substantial number of flaws detected in the testing stage late in development processes are started at the beginning of the process as requirements faults. Besides, fixing these requirements faults in the testing period was ten times more costly than if they had been spotted earlier in the process through the design stage[65].

Consequently, in recent years new methodology has emerged in many disciplines, such as automotive and aeronautic that is a model-based design methodology, which has become the adopted method for designing, modeling and simulating complex dynamic systems. These trend workflows enable embedded controls engineers to quickly develop reliable products of the highest performance. Not only that, they can accelerate product creation, enhance performance, improve reliability, and decrease engineering cost. Furthermore, the risk and complexity alongside the difficulty of testing, debugging, and validating the complex systems makes them particularly suitable for this methodology[63].

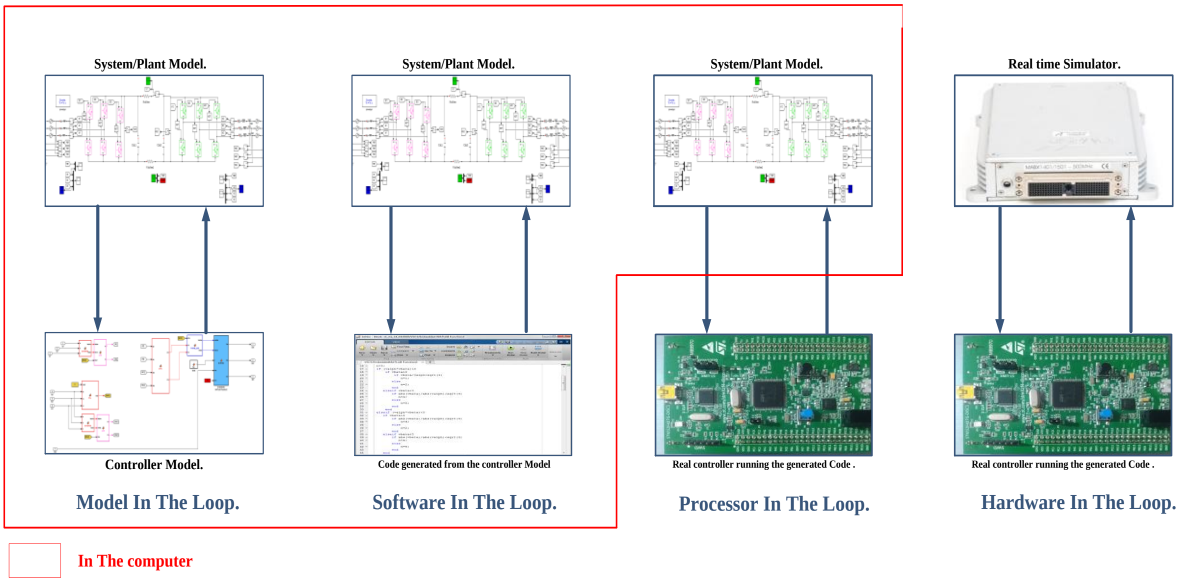
Model-Based Design is used in embedded control systems development (V-model) for rapid prototyping and provides workflow with consistent verification and validation of specifications. This approach is significant for designs seeking fault prevention and early glitches detection. Testing models through simulation is a precise method that allows the designer to quickly adjust and continuously test the design.

The goal of this chapter is to show the benefits of using a Model-Based Design approach to test the designed second order SMC for HVDC systems. The controller code is auto-generated in Simulink in order to validate the controller design throughout the SIL and PIL simulations. The purposed of using MBD approach is to validate the results of the model and the controller that are tested together using the Model-in-the-Loop (MIL) method.

IV.2. Model-Based Design

Model-Based Design (MBD) of engineering and dynamic systems is arising as a promising and useful method for engineers to create, simulate, and verify the system’s functionality. Furthermore, MBD tools allow the ability of automated code generation and downloading into the hardware. The benefits of MBD on industrial projects have been shown in the form of shortened project man/hours and decreased amount of software glitches also it facilitates the testing of different scenarios with the graphical model and makes it easy to find glitches in the early stages of development. The instantaneous feedback and the interaction with the model make it possible to verify and validate the testing of the control system, which leads to reduced development time. This also implies an influential factor that the software can be tested without any hardware. Simulink is a well-known tool for modeling, analyzing, and simulating a very wide variety of physical and mathematical systems, including those with nonlinear elements as it contains tools that offer advanced state of the art code generators can produce optimized, embeddable C/C++ source codes from these models[66][64].

The mentioned method consists of particular stages shown in Figure(IV.1).First, model-in the-loop (MIL) simulation, in which the system is modeled and the controller is tested in simulation using the model. The following is called software-in-the-loop (SIL) simulation; it can be done by testing the code (whether automatically generated or not) from the controller before downloading it on a real embedded system, like the STM32F4. This means performing a new simulation in the Simulink environment with the new block of the controller that contains the algorithm. The next stage is the processor-in-the-loop (PIL), in which the code generated from the controller will be loaded on the actual embedded system and tested again. Eventually, when the design phases finished and the system behaviors were proved to meet the specifications the hardware-in-the-loop (HIL) simulation can be adopted. In this approach, the generated code runs on a real embedded system with a physical simulator or with the real system instead of the virtual model[64][65][63].



Figure(IV.1): Various simulation types used in MBD testing[66].

IV.3. V-Model Work flow

Adopting Model-Based Design (MBD) workflow control engineers can visually construct systems utilizing mathematical models that describe complex elements and the communication in-between throughout the development process rather than using a real physical system. The V-model workflow diagram, depicted in Figure (IV.2), is commonly used as a design process. Conventionally, the left side of the V-model represents the embedded system design phases, while the right side represents the validation and verification phases of the embedded system. In the initial phase, the specifications and requirements of what the ideal system has to perform are established. The second phase is devoted to the system design, in which the developers analyze and understand the behavior of the system by studying the requirements documents and seeking to empower the requirements and specifications. This is accomplished through testing the model consistently utilizing MIL and fixing flaws that do not fit with the requirements and specifications. The next stage takes place after the code has been written or generated. This phase is all about the software design of the model. The idea is to ensure that the code is running accurately as desired and tested using SIL. After that, on the right side, a unit testing stage is going one step further and takes into account the processor by loading the code into the targeted processor. In PIL testing, the processor controls the virtual system on the host PC [66].The next phase is where the generated code is combined with the hardware and HIL testing is performed. These tests are made to see if the controller that was made in the system design stage works in the system. This links System Design together with the Integration Testing part. The last step is to validate if the results fulfill the requirements[66].

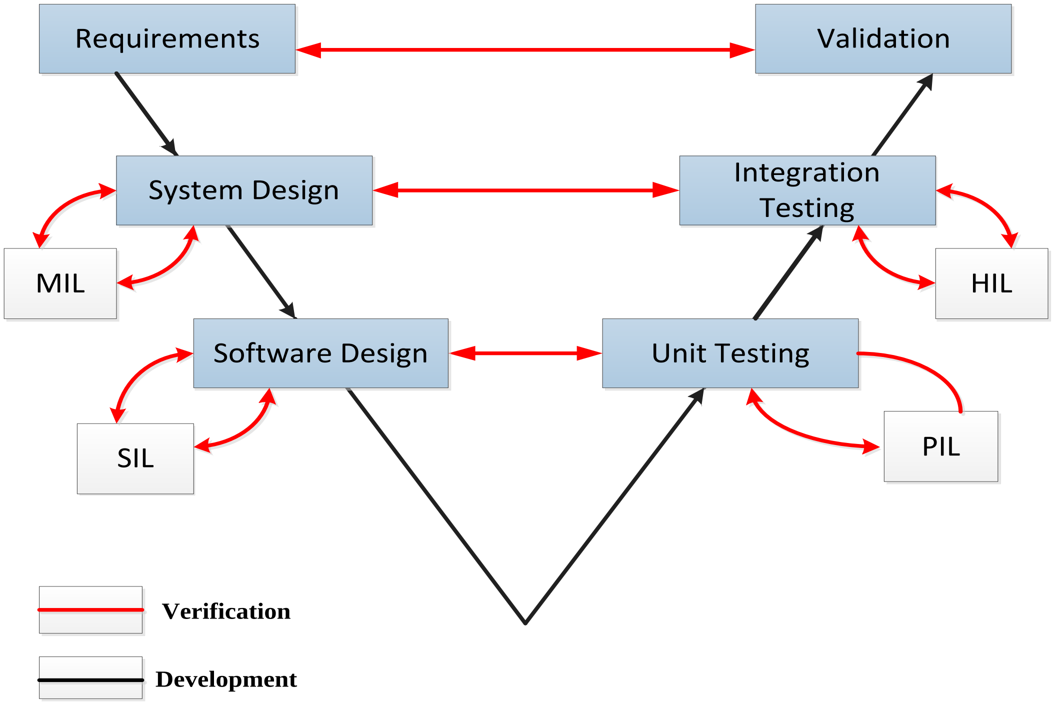


Figure (IV.2): An overview of the V-model[66]

IV.4. Software-in-the-Loop Simulation of HVDC Systems

The Software-in-the-Loop stage in the MBD methodology starts with code being generated from the controller model. This code is later tested in a virtual environment, without any hardware, to test how well the software manages the simulated system. Tests are done to guarantee that the code operates identically to the model when applying various types of input conditions, functions, and mathematical algorithms. SIL testing is a good strategy when simulating a real-time system that demands fast redundancies, to make sure that the software is capable to control the specifications as presented in Figure (IV.3).

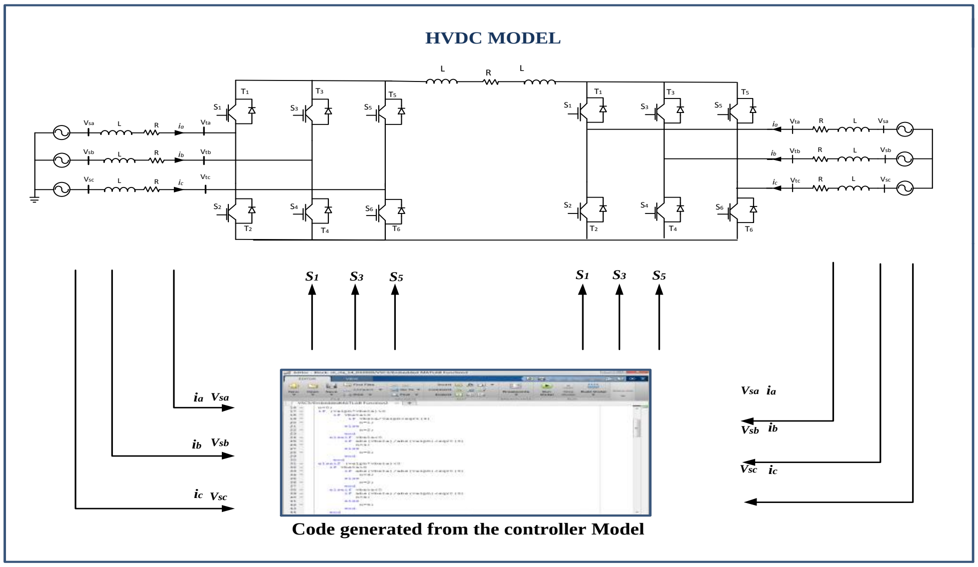
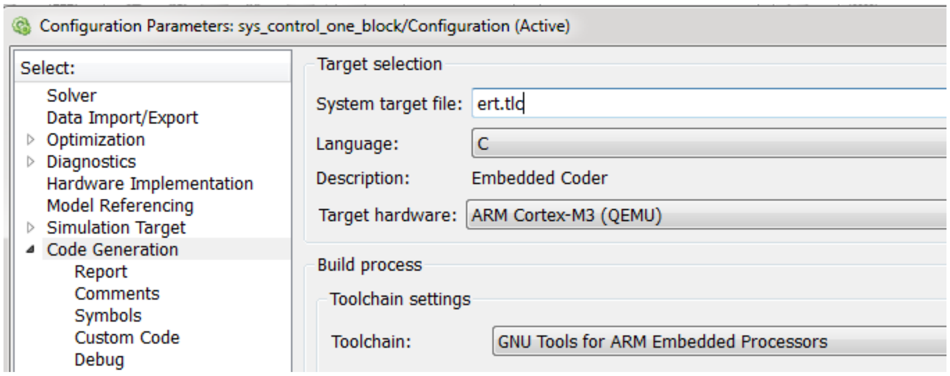


Figure (IV.3): SIL Concept

The main idea is that the controller must be built into C/C++ code. The controller auto-generated code, which is usually in C programming language, will be applied to run the simulation again. The simulation code of the plant/system remains the same, that is, in the original language of the simulation environment. These simulations are achieved by the Embedded Coder included in Simulink. The STMicroelectronics STM32F4- Discovery package must be installed to auto-generate an optimized code for the STM32F407.

IV.4.1 SIL Configuration

To perform HVDC system SIL simulation a *Simulink* model must be designed. After regrouping the controller in one subsystem the model must be configured before being ready to generate a C/C++ code block. Open the Configuration Parameters window and go to Code Generation. Choose 'ert.tlc' as the desired System Target File and the *ARM Cortex-M3 (QEMU)* as the Target Hardware. Select the *Toolchain* that will be used for the final code generation with the *Waijung* toolbox. In this project the *GNU* ARM *toolchain* will be used. The window must look like as in Figure (IV.4).


Configuration Parameters: sys_control_one_block/Configuration (Active)

Target selection

System target file: ert.tlc

Language: C

Description: Embedded Coder

Target hardware: ARM Cortex-M3 (QEMU)

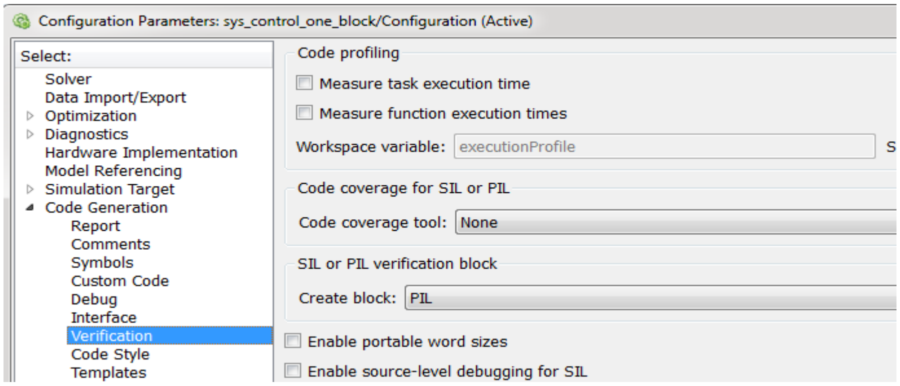
Build process

Toolchain settings

Toolchain: GNU Tools for ARM Embedded Processors

Figure (IV.4):Code generation parameters for the Embedded Coder Support Package for STMicroelectronics STM32F4-Discovery Board toolbox

Go to Code Generation>> Verification and make sure that the creation block is set to PIL as shown in Figure (IV.5).


Configuration Parameters: sys_control_one_block/Configuration (Active)

Code profiling

☐ Measure task execution time

☐ Measure function execution times

Workspace variable: executionProfile

Code coverage for SIL or PIL

Code coverage tool: None

SIL or PIL verification block

Create block: PIL

☐ Enable portable word sizes

☐ Enable source-level debugging for SIL

Figure (IV.5): Parameters verification for the Embedded Coder Support Package for STMicroelectronics STM32F4-Discovery Board toolbox

The SIL simulation could also be done using a particular SIL block, but in this case, the distinction between performing a SIL or a PIL simulation will be provided by the selected target. The target previously selected was the *QEMU*, which is an emulator that executes the PIL block on the host computer without the necessity of having an STM32F4 connected.

Other emulators can be employed such as*(Microsoft Windows SDK Software Development Kit*, *ARM fast models*,*Imperas -OVPSIM and DEV*, etc..*)* depending on the targeted hardware and the software of the host computer.
QEMU is Quick Emulator, open-source software that supports the virtualization of hardware boards, and it particularly holds good support for ARM guests. *QEMU* supports full-system mode emulation that is, emulating peripherals, memory, and I/O along with processors. *QEMU* is supported on both Linux and Windows PC, downloadable both as binary files or source code and executable. QEMU already has various hardware boards emulated such as *Raspberry Pi, TI Stellaris, versatile PB*, and many more[67].

Before proceeding further make sure that to set the current workspace to a specific location for this generated code to avoid any error. The next step is to build the block. Go to the model, right-click on the subsystem that contains the controller and click C/C++ Code>> Deploy this Subsystem to Hardware, Figure (IV.6).

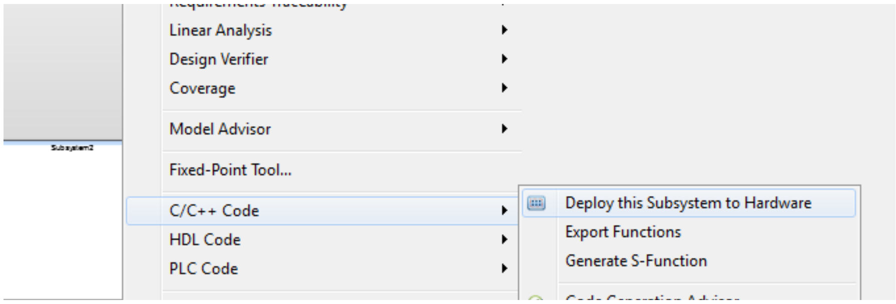


Figure (IV.6): Auto code generation option

A new window will appear the generated block is shown in Figure (IV.7), click the Build key. After the process is finished, a different model will be opened including a PIL block. Copy it and paste it into the previous Simulink model replacing with it the original controller block as shown in Figure(IV.8); simulate to compare its behavior with the real model.

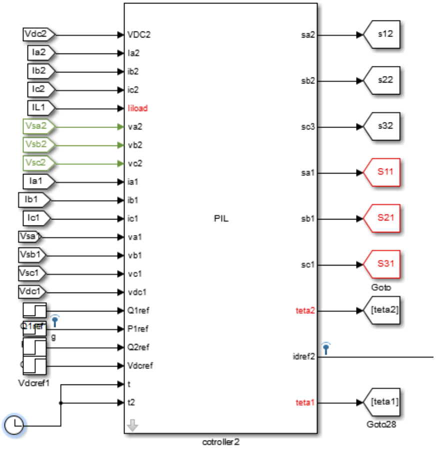


Figure (IV.7): Generated block that contains the controller C code.

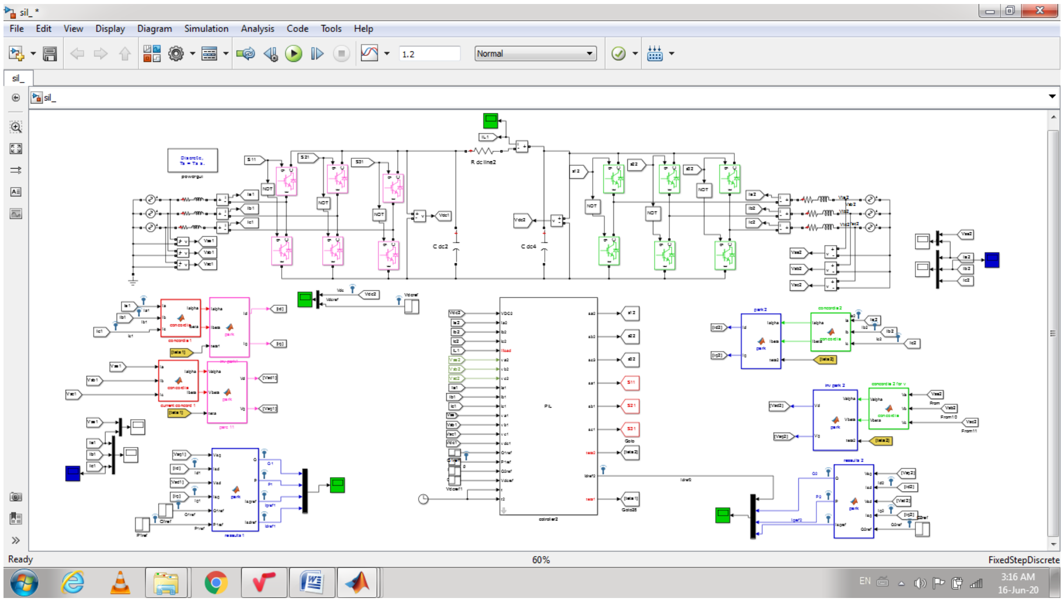


Figure (IV.8): Simulink model for HVDC SIL simulation.

IV.4.2 SIL Simulation Results

In order to validate the effectiveness of proposed 2-SMC controller, the control part was implemented in the Matlab/Simulink environment using the block (Embedded Matlab Function) and co-simulated by SIL technique using an emulator of Digital Signal Processor STM32F4DISCOVERY.

IV.4.2.1SIL simulation of Point-to-Point VSC-based HVDC Power Transmission System

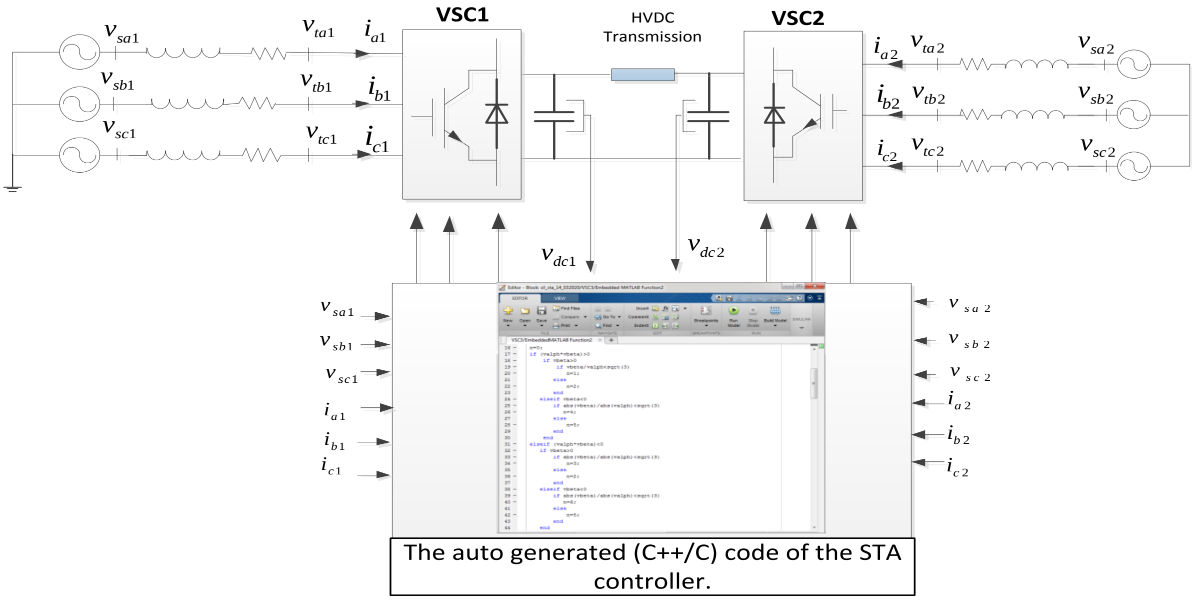
The VSC based HVDC system presented in Figure (VI.9) is co-simulated using the parameters provided in the Appendix A. The co-simulation test consists of evaluating the performance and the dynamic of the designed control system by varying the reference values of the active and reactive powers at the VSC1 terminal and the DC reference value as well. The adopted test scenarios are as follows:

- At t=0.3 s, the active power reference is increased from 200 MW to 300 MW.

- At t=0.6 s, theVSC1 reactive power reference is changed from 0 to 50 MVAR.

- At t=0.9 s, the DC voltage reference is increased from 90 kV to 92 kV.

- At t=0.11 s, the VSC2 reactive power reference is changed from 0 MVAR to 50 MVAR.



```
n=0;
if (valph*vbeta)>0
    if vbeta>0
        if vbeta/valph<sqrt(3)
            n=1;
        else
            n=2;
        end
    elseif vbeta<0
        if abs(vbeta)/abs(valph)<sqrt(3)
            n=4;
        else
            n=5;
        end
    end
elseif (valph*vbeta)<0
    if vbeta>0
        if abs(vbeta)/abs(valph)<sqrt(3)
            n=3;
        else
            n=2;
        end
    elseif vbeta<0
        if abs(vbeta)/abs(valph)<sqrt(3)
            n=6;
        else
            n=5;
        end
    end
```

Figure (IV.9): SIL simulation of 2-SMC VSC-based Point-to-Point HVDC system.

Figures (IV.10) show the dynamic responses of point-to-point VSC-HVDC system while performing the aforementioned scenarios.

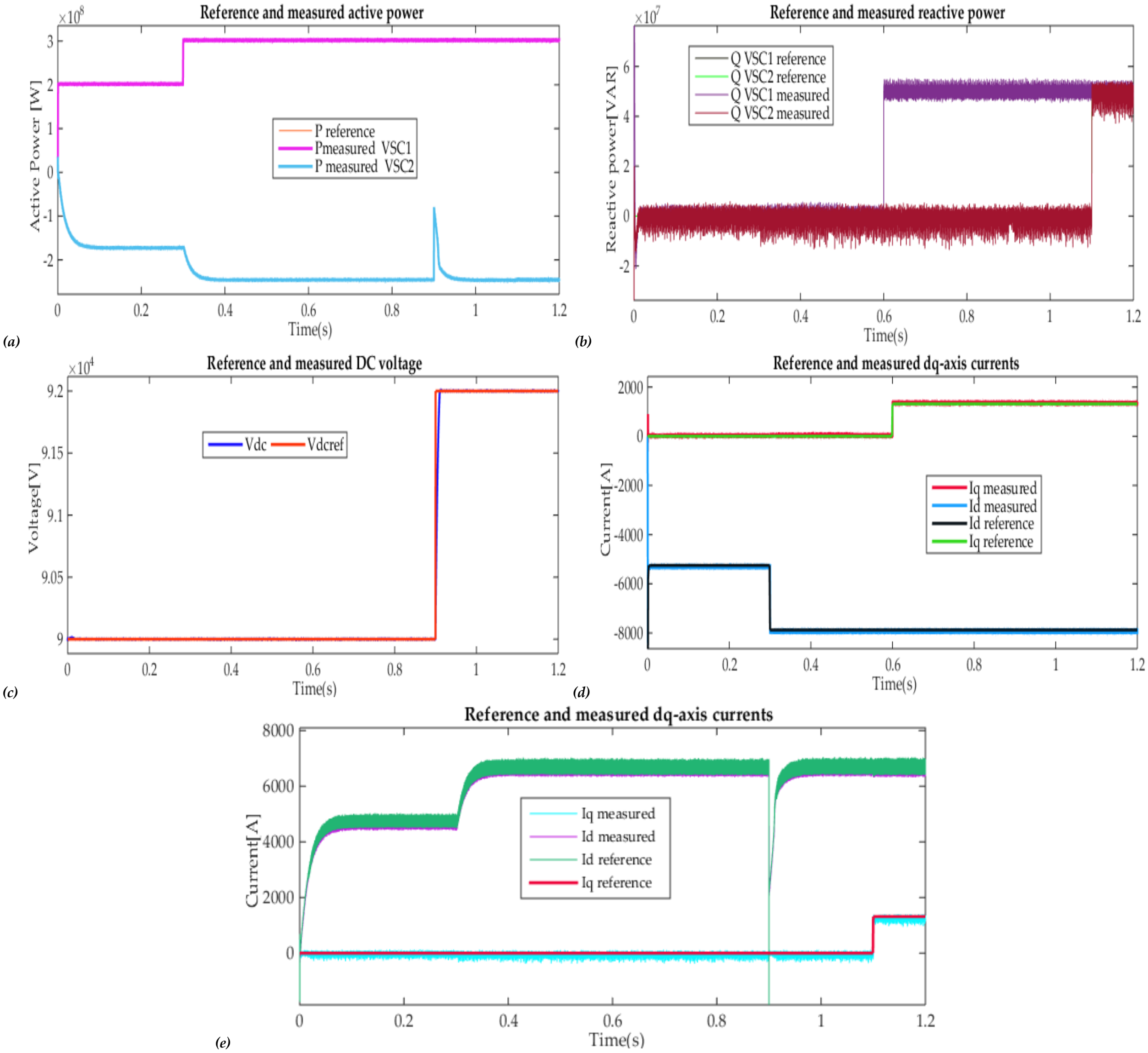
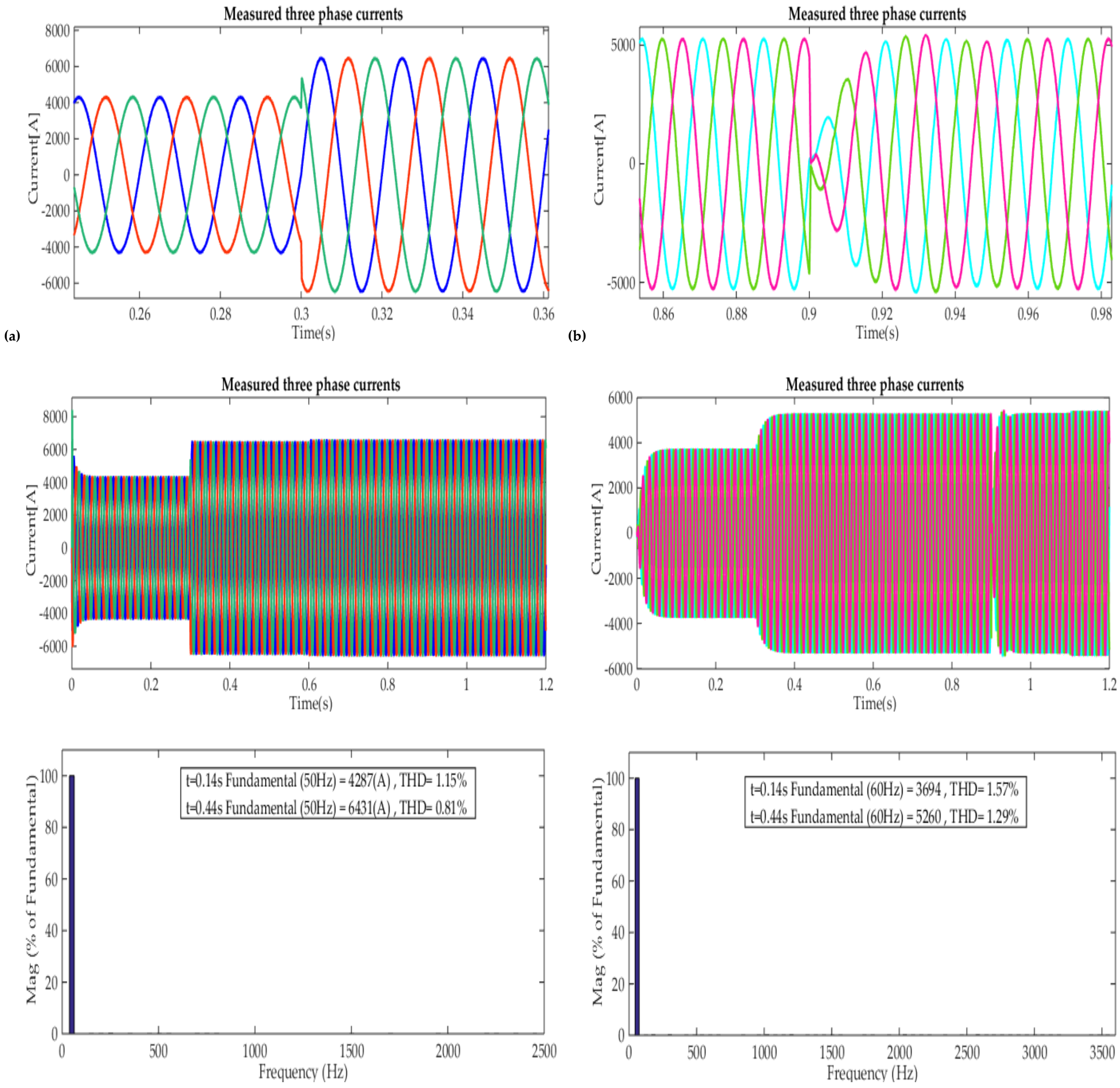


Figure (IV.10): the dynamic responses of point-to-point VSC-HVDC, (a) Reference and measured active powers, (b) Reference and measured reactive powers ,(c) DC-bus voltage and its reference , (d) VSC1 AC side reference and measured *dq*-axes currents , (e) VSC2 AC side reference and measured *dq*-axes

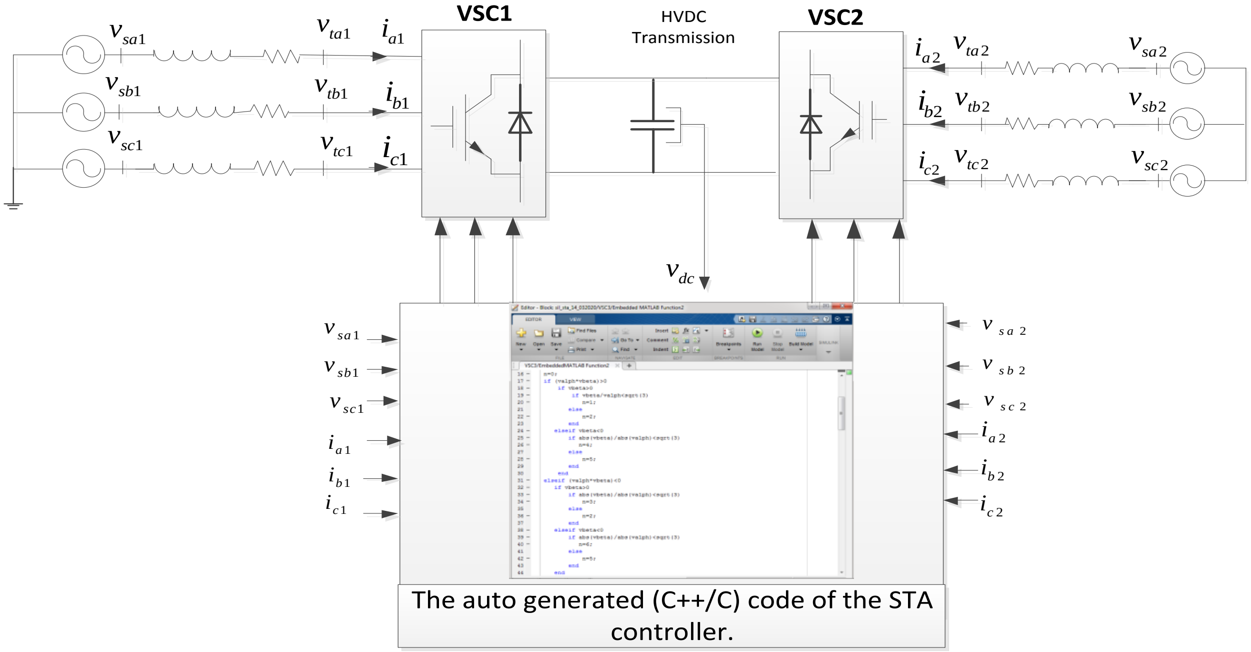
Figures(IV.11) present the three-phase currents on both sides of the HVDC system and their harmonic spectra.



Figure(IV.11): the AC side three phase currents and the Line current harmonic spectrum for: (a) VCS1 (b)VSC2

IV.4.2.2SIL simulation of Back-to-Back VSC-based HVDC Power Transmission System

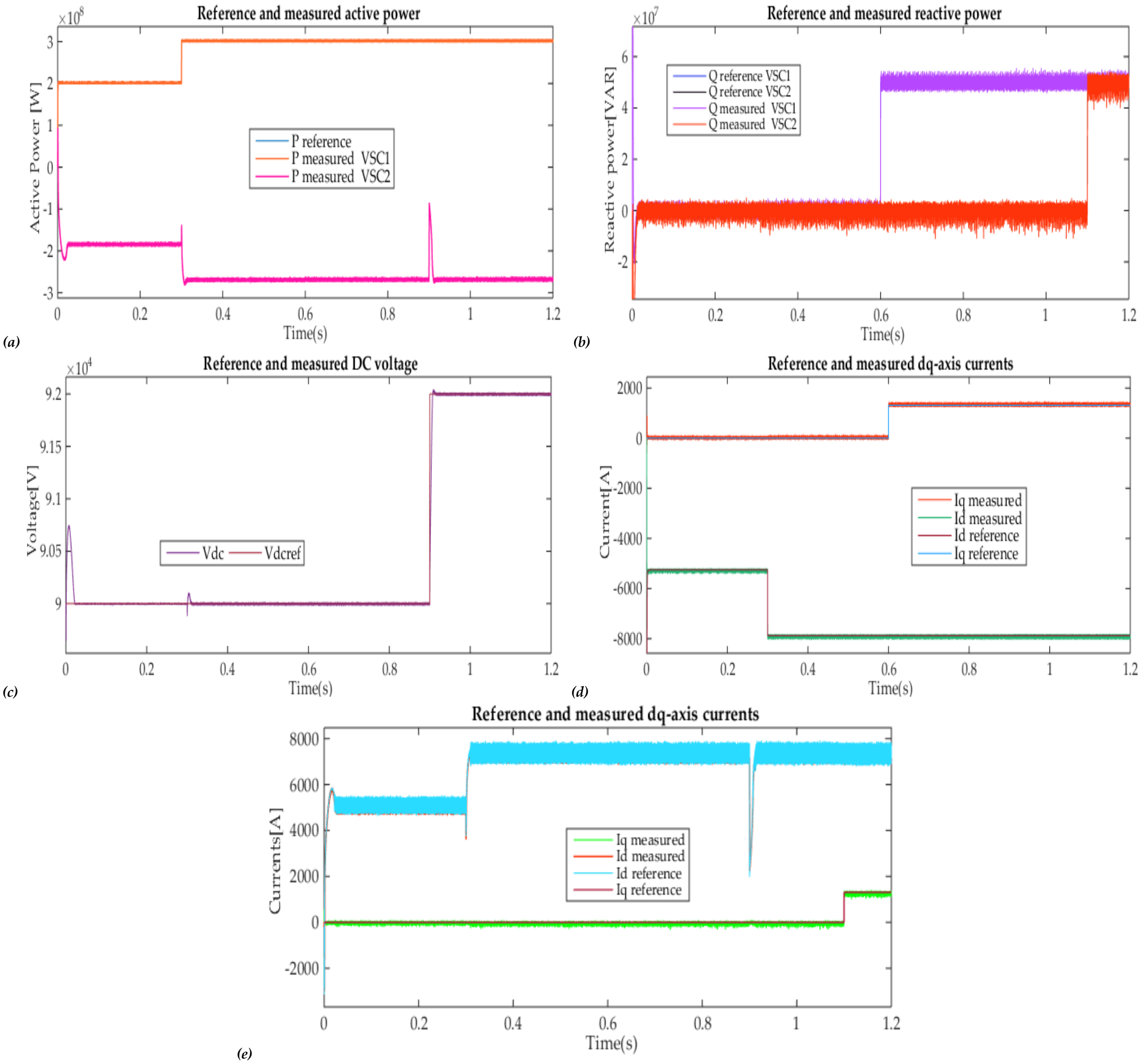
Figure (IV.12) presents the block diagram of software in the loop simulation of Back-to-Back VSC-HVDC system controlled by second order sliding mode controllers.



```
n=0;
if (valph*vbeta)>0
     if vbeta>0
         if vbeta/valph<sqrt(3)
            n=1;
        else
            n=2;
        end
    elseif vbeta<0
        if abs(vbeta)/abs(valph)<sqrt(3)
           n=4;
        else
            n=5;
        end
     end
elseif (valph*vbeta)<0
    if vbeta>0
        if abs(vbeta)/abs(valph)<sqrt(3)
            n=3;
        else
            n=2;
        end
    elseif vbeta<0
        if abs(vbeta)/abs(valph)<sqrt(3)
           n=6;
        else
            n=5;
        end
    end
```

Figure (IV.12): SIL simulation of 2-SMC of Back-to-Back VSC-HVDC system

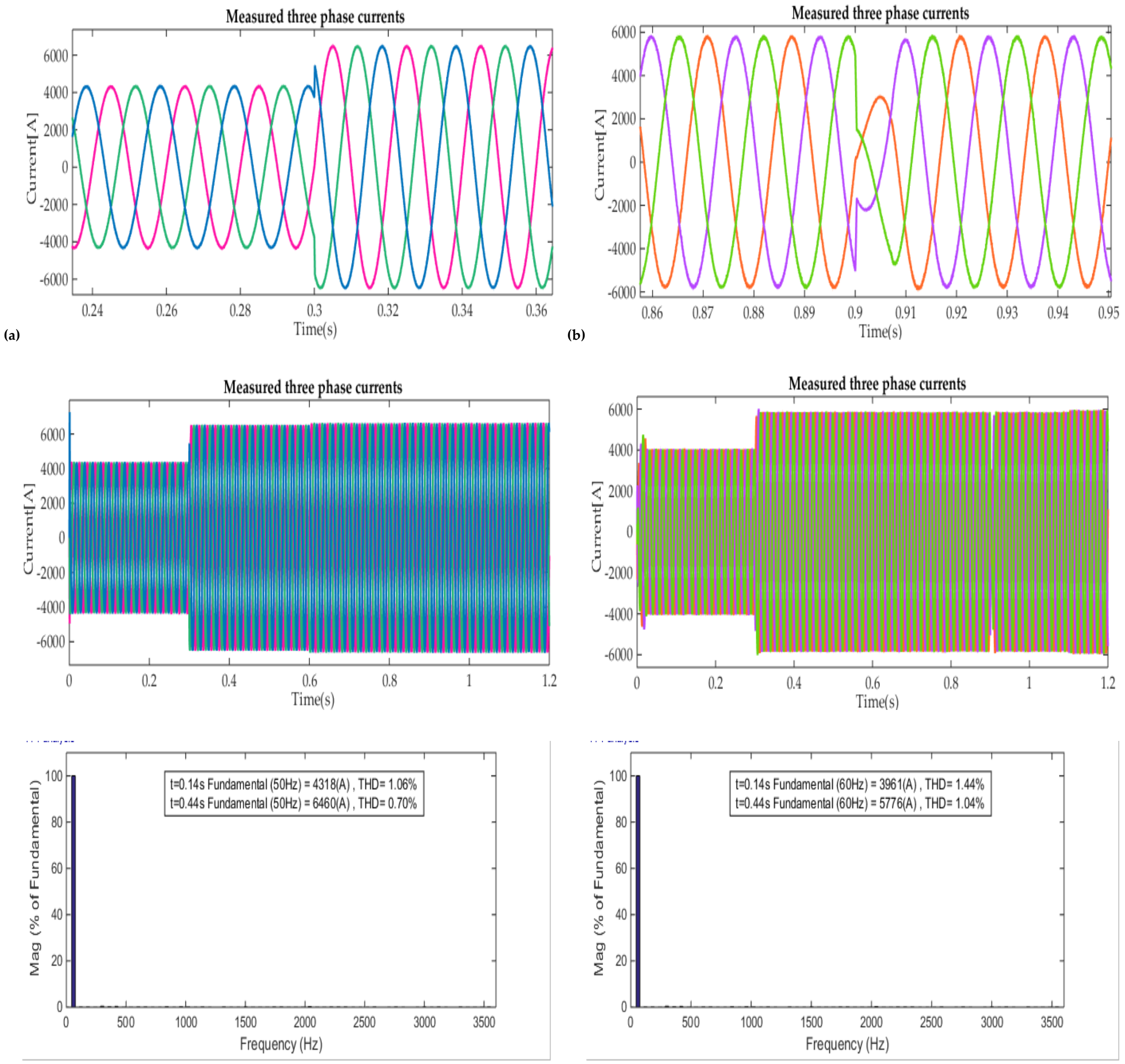
Figures (IV.13) illustrate the dynamic responses issued from SIL simulation of the Back-to-Back VSC-HVDC system controlled by 2-SMC.



(a) (b) (c) (d) (e)

Figure (IV.13): the dynamic responses of Back-to-Back VSC-HVDC, (a) Reference and measured active powers, (b) Reference and measured reactive powers ,(c) DC-bus voltage and its reference , (d) VSC1 AC side reference and measured *dq*-axes currents ,(e) VSC2 AC side reference and measured *dq*-axes

Figures(IV.14) present the three-phase currents on both sides of the HVDC system and their harmonic spectra.



Figure(IV.14): the AC side three phase currents and the Line current harmonic spectrum for: (a) VCS1 (b)VSC2

In this section, the results concerning the SIL testing of the 2-SMCof VSC based HVDC systems are given. The SIL simulation is performed by implementing the HVDC system model in the Simulink environment while the generated code block controls the system. According to these results the active and reactive powers as well as the DC voltage follow their references properly even during the shift of their reference values. What is interesting here is that the SIL results are in accordance with MIL results presented in chapter III, which means that the code generated from the model for the host computer reflects appropriately the proposed controller.

IV.5 Processor-in-the-Loop (PIL)Simulation of HVDC Systems

The PIL test is an essential stage in the development of an MBD control algorithm. In this test it is necessary to install and use the Embedded Coder to auto-generate the code to be executed in the processor. The purpose of the Embedded Coder is to auto-generate an optimized code for the embedded system; which is, in our case, the STM32 Discovery board. To achieve the PIL test, the Embedded Coder tool from MathWorks Inc. is used to generate code particular for the ARM platform. Once the code has been generated, it can be downloaded to the control hardware and the result can be sent back to the software through serial communication as illustrated in Figure (IV.15). The results of the PIL simulation are transferred to Simulink to verify the numerical equivalence of the simulation and the code generation results.

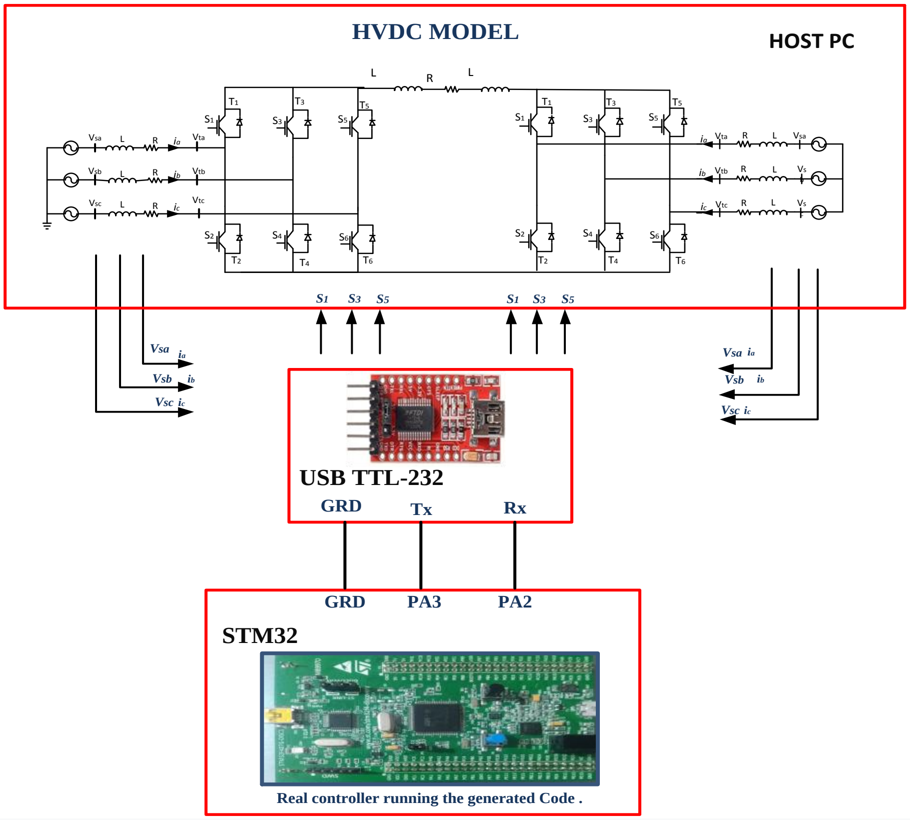


Figure (IV.15):PIL concept and communication link.

IV.5.1 PIL Configuration

In this part, a Simulink model will be configured to run Processor-In-the-Loop (PIL) and Monitor the simulations. In a PIL simulation, the generated code runs on the STM32 Discovery board. The PIL verification process is a crucial part of the development cycle to ensure that the behavior of the deployment code matches the design.

IV.5.1.1. Required Hardware

- STMicroelectronics STM32F407G-Discovery

The STM32F4DISCOVERY board is a low-cost and easy-to-use development kit that allows users to easily develop applications with the STM32F407VG high-performance microcontroller with the ARM® Cortex®-M4 32-bit core. It includes everything required either for beginners or for experienced users to get quickly started. Based on STM32F407VG, it includes an ST-LINK/V2 or ST-LINK/V2-A embedded debug tool, two ST-MEMS digital accelerometers, a digital microphone, one audio DAC with integrated class D speaker driver, LEDs, pushbuttons and a USB OTG micro-AB connector. For more specifications, refer to the STM32F4DISCOVERY and STM32F407VGT6 datasheets [63] [64]. A picture of this board is shown in Figure (IV.16).

Figure (IV.16):STM32F4-Discovery board

- USB type A to Mini-B cable

- USB TTL-232 cable - TTL-232R 3.3V (serial communication for STM32F4-Discovery board)

Note: This project was tested with the YP-05 FTDI F232RL adapter shown in Figure (IV.17).

Figure (IV.17): YP-05 FTDI F232RL adapter

IV.5.1.2. Choosing a Communication Interface for PIL Simulation

The STM32F4-Discovery board supports two distinct communication interfaces for PIL: ST-LINK and serial. The ST-LINK communication interface does not require any extra cables or hardware besides a USB type A to Mini-B cable used to connect the STM32F4-Discovery board to the host computer. The serial communication interface requires a USB TTL-232 cable. Running a PIL simulation using the serial communication interface is much faster than running a PIL simulation using ST-LINK. It is recommended to use the serial interface for PIL whenever possible.

Follow the hardware setup instructions below:

- Connect the ground pin of the USB TTL-232 cable to one of the GND pins on the STM32F4-Discovery board.

- Connect the RX pin of the USB TTL-232 cable to the PA2 pin on the STM32F4-Discovery board.

- Connect the TX pin of the USB TTL-232 cable to the PA3 pin on the STM32F4-Discovery board.

- Connect the USB side of the USB TTL-232 cable to your host computer.

- Power on your board by connecting a USB type A to Mini-B cable to the STM32F4-Discovery board.

Once you finish the above measures, a novel serial / COM port should be ready for use on your host computer. To find the COM port associated with your adapter cable, follow the steps hereafter:

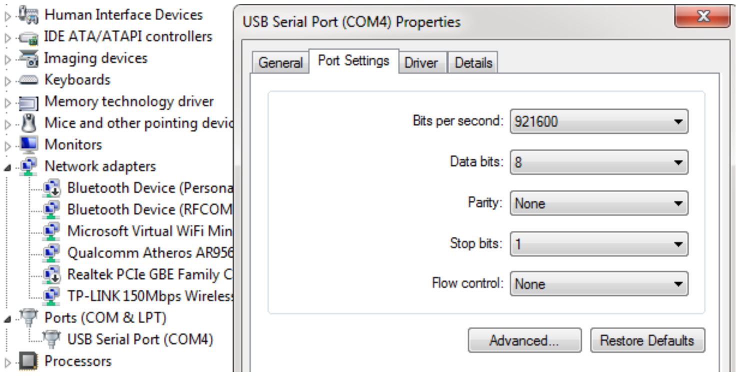
- Open Devices and Printers in Windows.

- Double-click the entry for your USB TTL-232 adapter device.

- In the device properties dialog, click the Hardware tab, click on the USB serial port and then click the Properties button.

- Click the Port Settings tab.

- Copy the COM port number to the Simulink model and change the transfer speed of data to maximum (bits per second) as shown in Figure (IV.18).



Bits per second: 921600
Data bits: 8
Parity: None
Stop bits: 1
Flow control: None

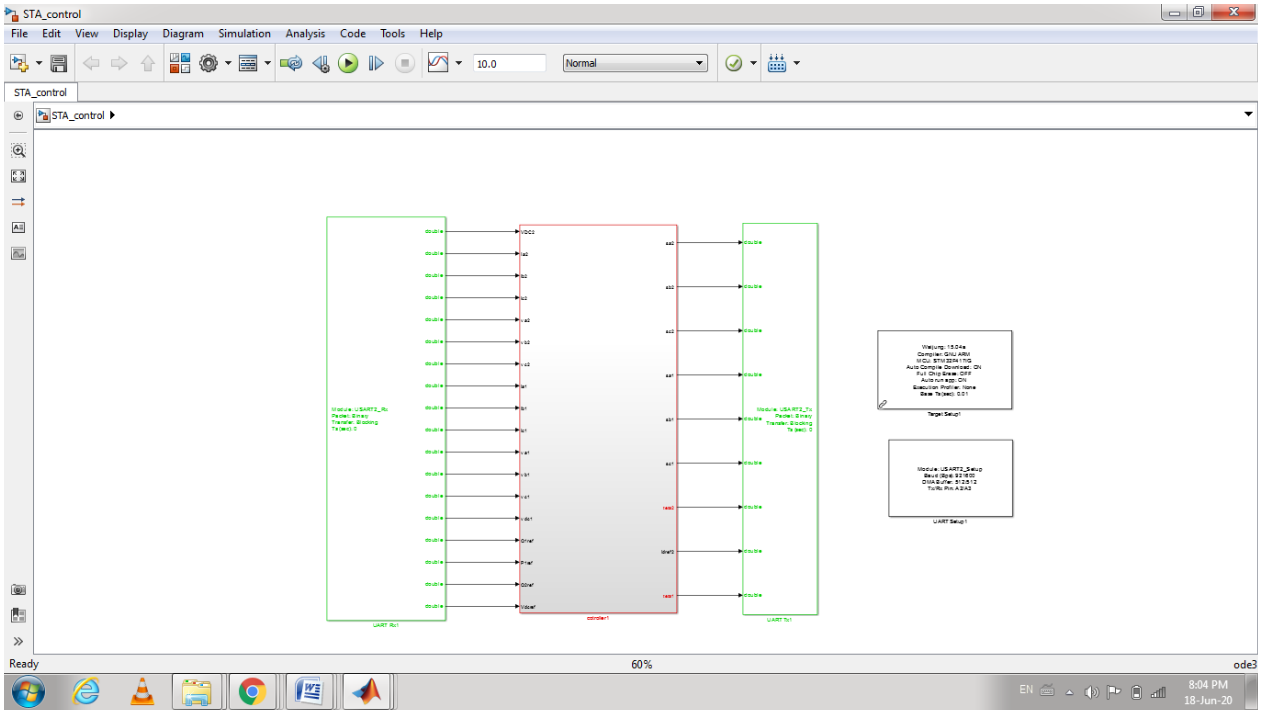
Figure (IV.18): COM port properties of USB Serial Ports in the Device manger in windows.

Note: beware that increasing the baud rate will increase the date transfer process, but speeding up the process too much will affect the accuracy of the results.

After changing the baud rate make sure to press the reset button on The STM32F4-Discovery board.

IV.5.1.3. Model Configuration for Code Generation

First, open a new Simulink model and add the regrouped controller in that model in the Simulink Library browse for the Waijung-Blockset and add the Target setup, UART Setup, UART Rx and the UART Tx to the recently constructed model as presented in Figure (IV.19).



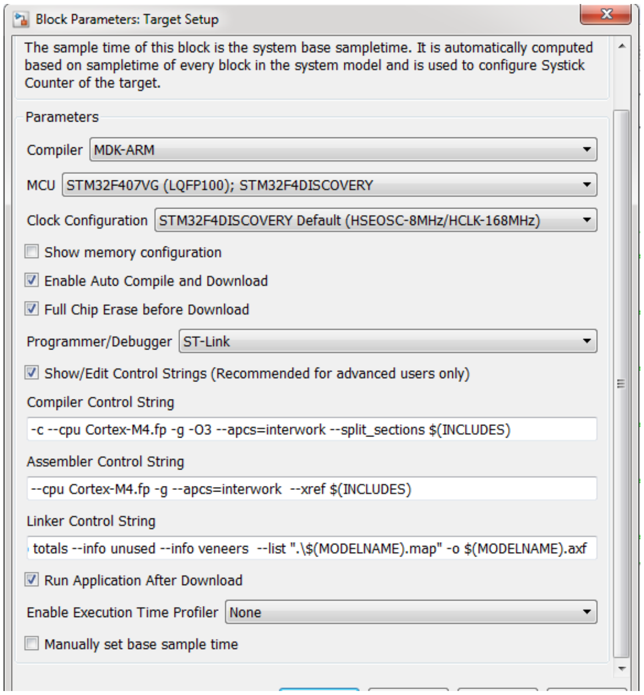
Waijung: 15.04a
Compiler: GNU ARM
MCU: STM32F417IG
Auto Compile Download: ON
Full Chip Erase: OFF
Auto run app: ON
Execution Profiler: None
Base Ts(sec): 0.01

Module: USART2_Setup
Baud (Bps): 921600
DMA Buffer: 512/512
Tx/Rx Pin: A2/A3

Figure (IV.19): Gathering of all VSC-HVDC system control algorithms in a single subsystem

IV.5.1.4. Target Setup Configuration

Double click on the Target setup, choose the desired compiler and the MCU also check the "Full chip erase before download" option is selected and click OK to save as presented in figure (IV.20).



The sample time of this block is the system base sampletime. It is automatically computed based on sampletime of every block in the system model and is used to configure Systick Counter of the target.

Parameters

Compiler MDK-ARM

MCU STM32F407VG (LQFP100); STM32F4DISCOVERY

Clock Configuration STM32F4DISCOVERY Default (HSEOSC-8MHz/HCLK-168MHz)

☐ Show memory configuration

☑ Enable Auto Compile and Download

☑ Full Chip Erase before Download

Programmer/Debugger ST-Link

☑ Show/Edit Control Strings (Recommended for advanced users only)

Compiler Control String

```
-c --cpu Cortex-M4.fp -g -O3 --apcs=interwork --split_sections $(INCLUDES)
```

Assembler Control String

```
--cpu Cortex-M4.fp -g --apcs=interwork  --xref $(INCLUDES)
```

Linker Control String

```
totals --info unused --info veneers  --list ".\$(MODELNAME).map" -o $(MODELNAME).axf
```

☑ Run Application After Download

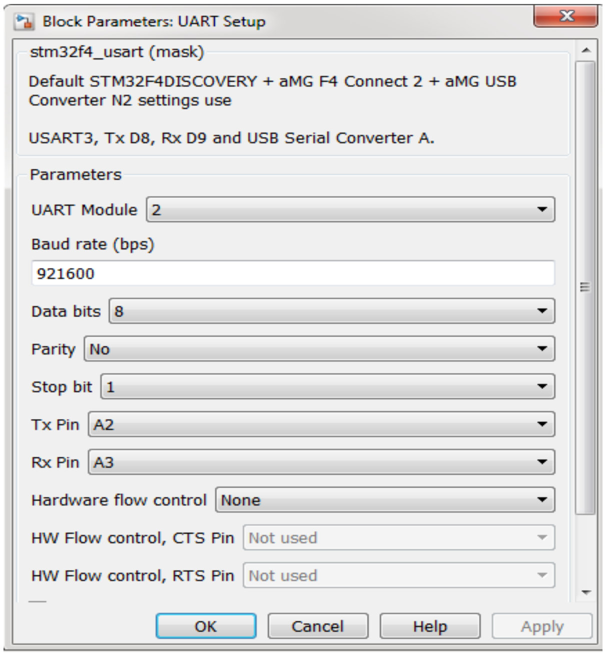
Enable Execution Time Profiler None

☐ Manually set base sample time

Figure (IV.20):Target setup configuration

IV.5.1.5. UART Setup Configuration

Double click on the UART Setup and choose the UART module (in our situation UART 2 that is the Pin PA2 and the Pin PA3. As discussed earlier, STM32F407 includes 4 USART and 2 UART modules). Next choose the Baud rate as chosen earlier and set the Rx pin and Tx pin accordingly to the hardware wiring as shown in figure (IV.21).



stm32f4_usart (mask)

Default STM32F4DISCOVERY + aMG F4 Connect 2 + aMG USB Converter N2 settings use

USART3, Tx D8, Rx D9 and USB Serial Converter A.

Parameters

UART Module 2

Baud rate (bps)

921600

Data bits 8

Parity No

Stop bit 1

Tx Pin A2

Rx Pin A3

Hardware flow control None

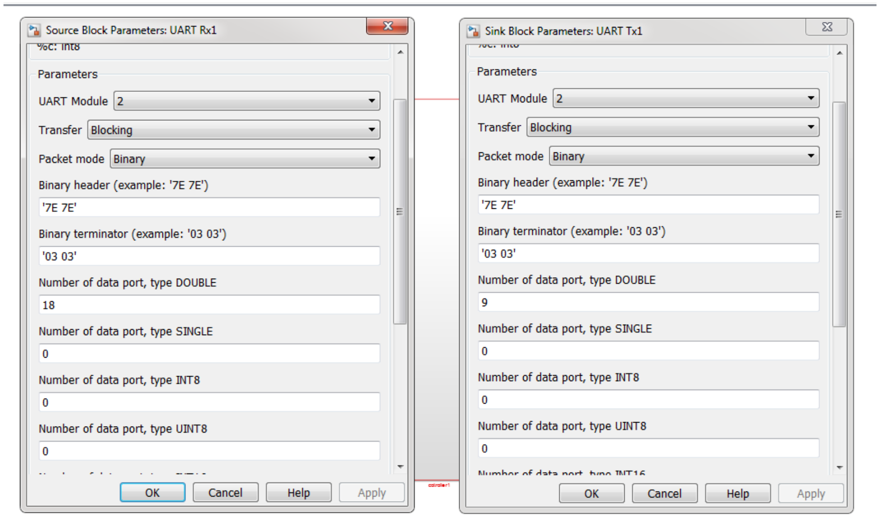
HW Flow control, CTS Pin Not used

HW Flow control, RTS Pin Not used

Figure (IV.21).UART setup configuration

IV.5.1.6. UART Tx and Rx blocks Configurations

Double click on the UART Tx and Rx and set the same UART model chosen before further set the Pocket mode to Binary and set the Number of data port to your need (in our model 18 inputs and 9 outputs) as displayed in figure (IV.22).



Source Block Parameters: UART Rx1

Parameters

UART Module: 2

Transfer: Blocking

Packet mode: Binary

Binary header (example: '7E 7E'): '7E 7E'

Binary terminator (example: '03 03'): '03 03'

Number of data port, type DOUBLE: 18

Number of data port, type SINGLE: 0

Number of data port, type INT8: 0

Number of data port, type UINT8: 0

Sink Block Parameters: UART Tx1

Parameters

UART Module: 2

Transfer: Blocking

Packet mode: Binary

Binary header (example: '7E 7E'): '7E 7E'

Binary terminator (example: '03 03'): '03 03'

Number of data port, type DOUBLE: 9

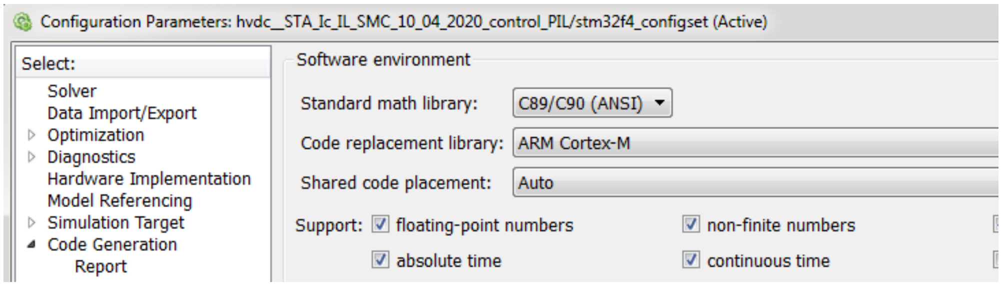
Number of data port, type SINGLE: 0

Number of data port, type INT8: 0

Number of data port, type UINT8: 0

Figure (IV.22): UART Tx and Rx blocks configurations

Finally, before building and deploying the model to STM32F407 you can use an option in the configuration Parameters>code generation> interface and set the code replacement library to ARM Cortex-M to optimize the generation of the code. This is optional as presented in figure (IV.23).



Configuration Parameters: hvdc__STA_Ic_IL_SMC_10_04_2020_control_PIL/stm32f4_configset (Active)

Software environment

Standard math library: C89/C90 (ANSI)

Code replacement library: ARM Cortex-M

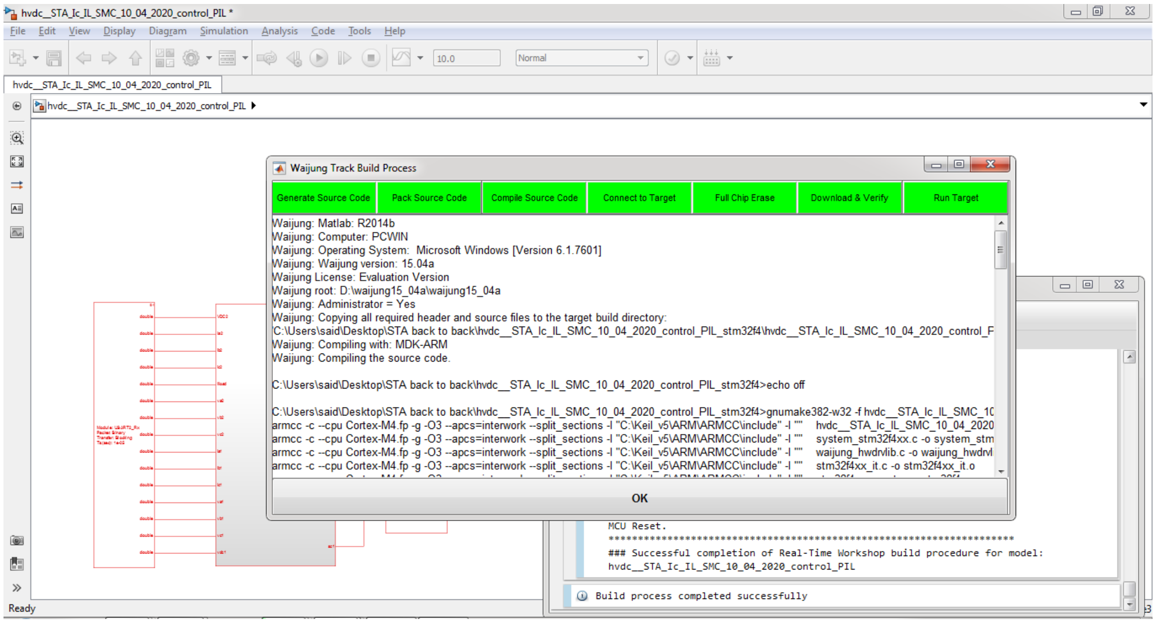
Shared code placement: Auto

Support: ☑ floating-point numbers ☑ non-finite numbers

☑ absolute time ☑ continuous time

Figure (IV.23): Code replacement library option selection

After deploying the code to the microcontroller as illustrated in Figure (IV.24), close the Simulink model and open the one with the plant/system, the communication with the microcontroller is done through the USART2, which uses pins PA2 and PA3 for transmitting and receiving, respectively. Before proceeding the USART2 must be configured. In order to do that, Drag a USART Host serial setup, Host serial Tx and Host serial Rx from the *Waijung* block-set into a configured model for PIL simulation, double click the setup block and select the module number 2. The baud rate has been set to 921600 bps, which gives good results and fast enough for this project. The rest of the parameters are configured as shown in the Figure (IV.25).



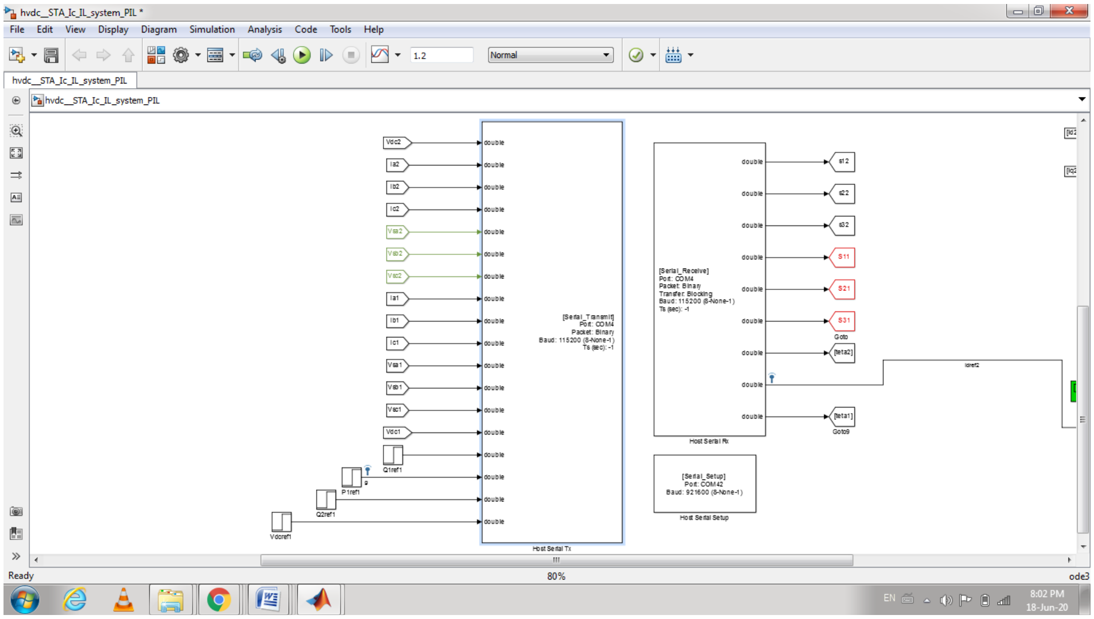
```
Waijung: Matlab: R2014b
Waijung: Computer: PCWIN
Waijung: Operating System:  Microsoft Windows [Version 6.1.7601]
Waijung: Waijung version: 15.04a
Waijung License: Evaluation Version
Waijung root: D:\waijung15_04a\waijung15_04a
Waijung: Administrator = Yes
Waijung: Copying all required header and source files to the target build directory:
C:\Users\said\Desktop\STA back to back\hvdc__STA_Ic_IL_SMC_10_04_2020_control_PIL_stm32f4\hvdc__STA_Ic_IL_SMC_10_04_2020_control_F
Waijung: Compiling with: MDK-ARM
Waijung: Compiling the source code.

C:\Users\said\Desktop\STA back to back\hvdc__STA_Ic_IL_SMC_10_04_2020_control_PIL_stm32f4>echo off

C:\Users\said\Desktop\STA back to back\hvdc__STA_Ic_IL_SMC_10_04_2020_control_PIL_stm32f4>gnumake382-w32 -f hvdc__STA_Ic_IL_SMC_10
armcc -c --cpu Cortex-M4.fp -g -O3 --apcs=interwork --split_sections -I "C:\Keil_v5\ARM\ARMCC\include" -I ""    hvdc__STA_Ic_IL_SMC_10_04_2020
armcc -c --cpu Cortex-M4.fp -g -O3 --apcs=interwork --split_sections -I "C:\Keil_v5\ARM\ARMCC\include" -I ""    system_stm32f4xx.c -o system_stm
armcc -c --cpu Cortex-M4.fp -g -O3 --apcs=interwork --split_sections -I "C:\Keil_v5\ARM\ARMCC\include" -I ""    waijung_hwdrvlib.c -o waijung_hwdrvl
armcc -c --cpu Cortex-M4.fp -g -O3 --apcs=interwork --split_sections -I "C:\Keil_v5\ARM\ARMCC\include" -I ""    stm32f4xx_it.c -o stm32f4xx_it.o
```

```
MCU Reset.
**********************************************************************
### Successful completion of Real-Time Workshop build procedure for model:
hvdc__STA_Ic_IL_SMC_10_04_2020_control_PIL
```

```
Build process completed successfully
```

Figure (IV.24):Interface representing the process of control algorithms building into the Microcontroller.

After that,set the communication and follow the same configuration previously also chose the COM PORT accordingly to match the built-in model as shown in Figure (IV.22).



[Serial_Transmit]
Port: COM4
Packet: Binary
Baud: 115200 (8-None-1)
Ts (sec): -1

[Serial_Receive]
Port: COM4
Packet: Binary
Transfer: Blocking
Baud: 115200 (8-None-1)
Ts (sec): -1

[Serial_Setup]
Port: COM42
Baud: 921600 (8-None-1)

Figure (IV.25):Configurations blocks and communications links of the UART host/client in the Simulink environment.

Eventually you will be able to run a processor in the loop simulation.

IV.5.2 PIL Simulation Results

IV.5.2.1PIL simulation of Point-to-Point VSC-based HVDC Power Transmission System

The 2-SMC algorithms implemented in the STM32F4 discovery board are identical to those designed in chapter III using the same parameters listed in Appendix A and those used in M IL simulation.

Figure (IV.26) presents the block diagram of process in the loop simulation of Point-to-PointVSC-HVDC system controlled by second order sliding mode controllers.

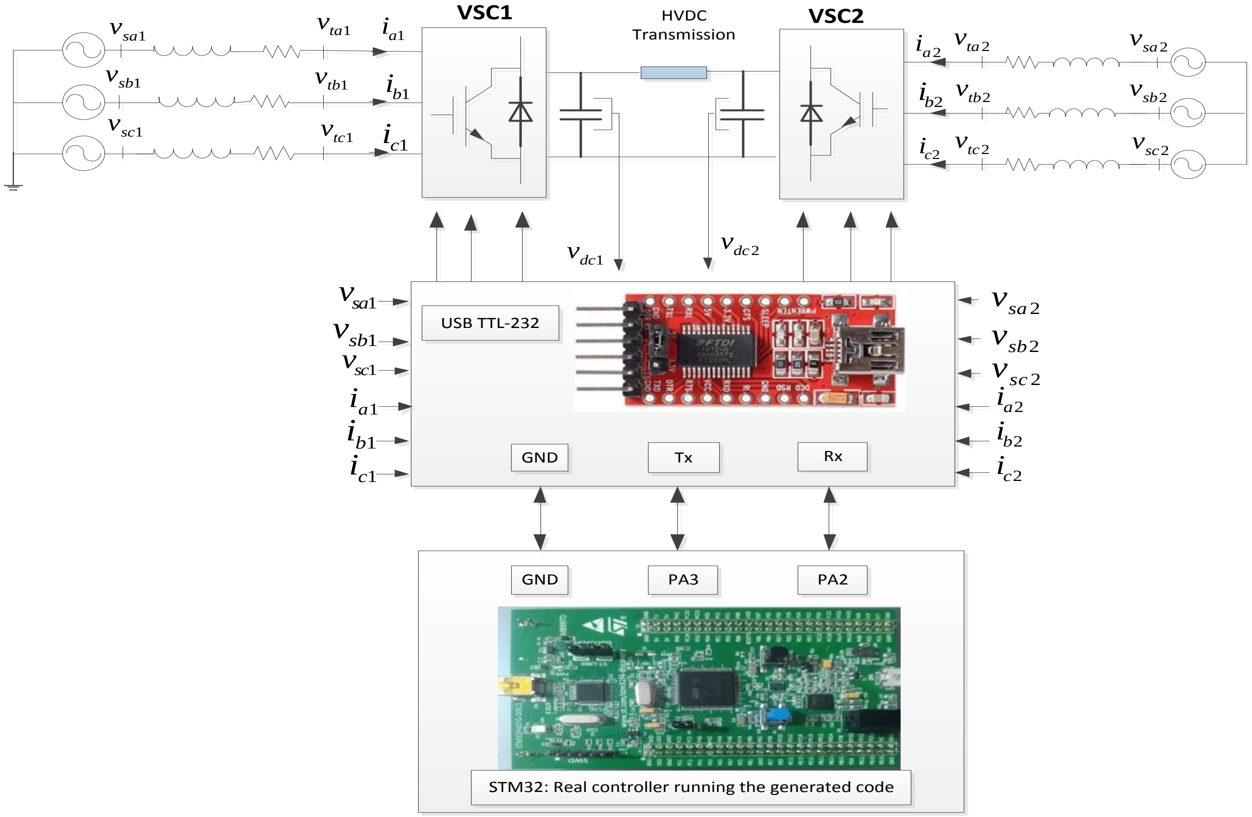


Figure (IV.26): PIL simulation of 2-SMC of Point-to-Point VSC-HVDC system.

The obtained results are presented in Figures (IV.27). According to these figures, it can be seen that the active and reactive powers as well as DC-link voltage follow their references well even in the presence of a variation of the reference values. So, these results validate the 2-SMCcontrol scheme and confirm the results obtained by MIL simulation in chapter III.

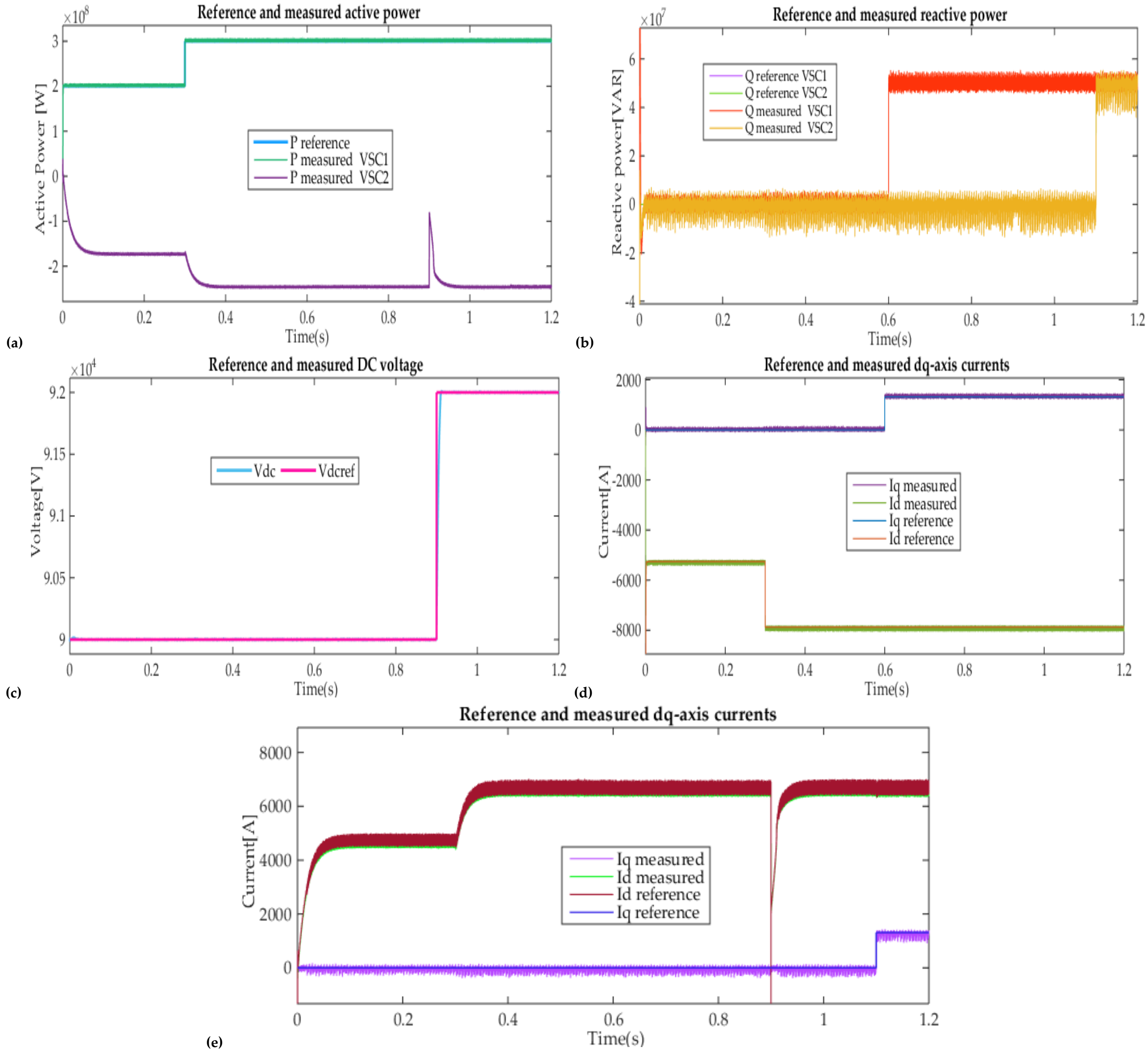
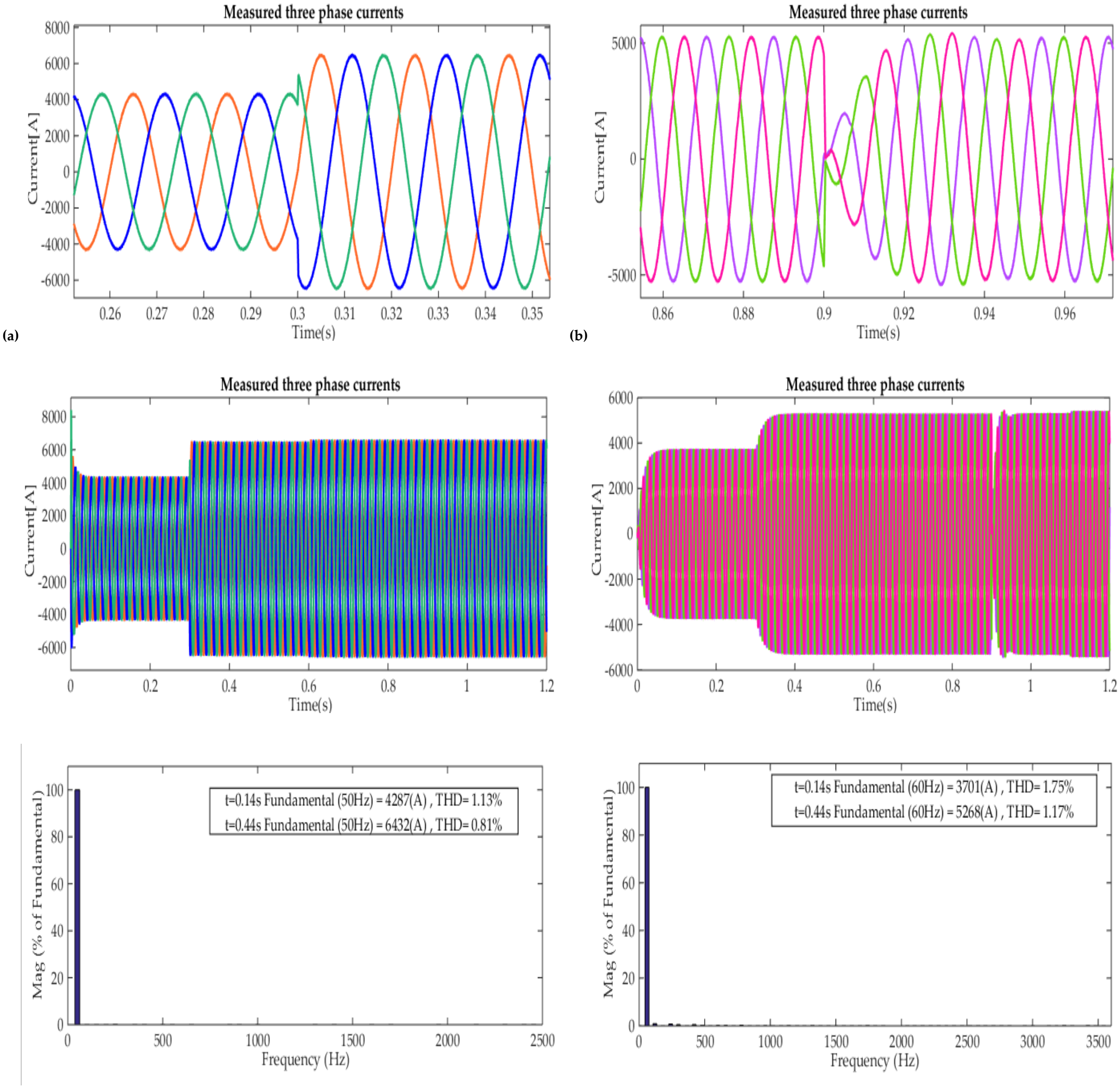


Figure (IV.27): the dynamic responses of point-to-point VSC-HVDC, (a) Reference and measured active powers, (b) Reference and measured reactive powers ,(c) DC-bus voltage and its reference , (d) VSC1 AC side reference and measured *dq*-axes currents ,(e) VSC2 AC side reference and measured *dq*-axes

Figures(IV.28) present the three-phase currents on both sides of the HVDC system and their harmonic spectra.



Figure(IV.28): the AC side three phase currents and the Line current harmonic spectrum for: (a) VCS1 (b)VSC2

PIL simulation results presented above validate again the 2-SMC design and confirm the results obtained by simulation in the previous chapter.

IV.5.2.2PIL simulation of Back-to-Back VSC-based HVDC Power Transmission System

Figure (IV.29) presents the block diagram of process in the loop simulation of back-to-back VSC-HVDC system controlled by second order sliding mode controllers.

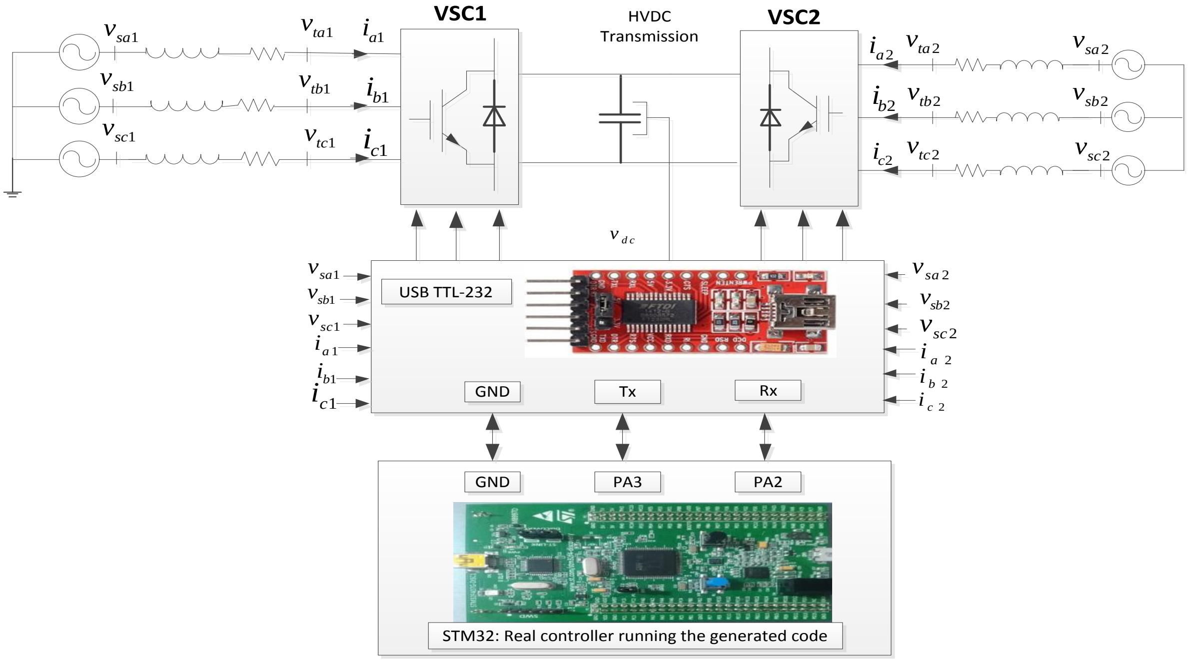


Figure (IV.29): PIL simulation of 2-SMC of back-to-back VSC-HVDC system.

Figures (IV.30) show the dynamic responses of the Back-to-Back VSC-HVDC system during changes in powers and DC voltage reference values. These results are almost similar to those obtained by MIL simulation.

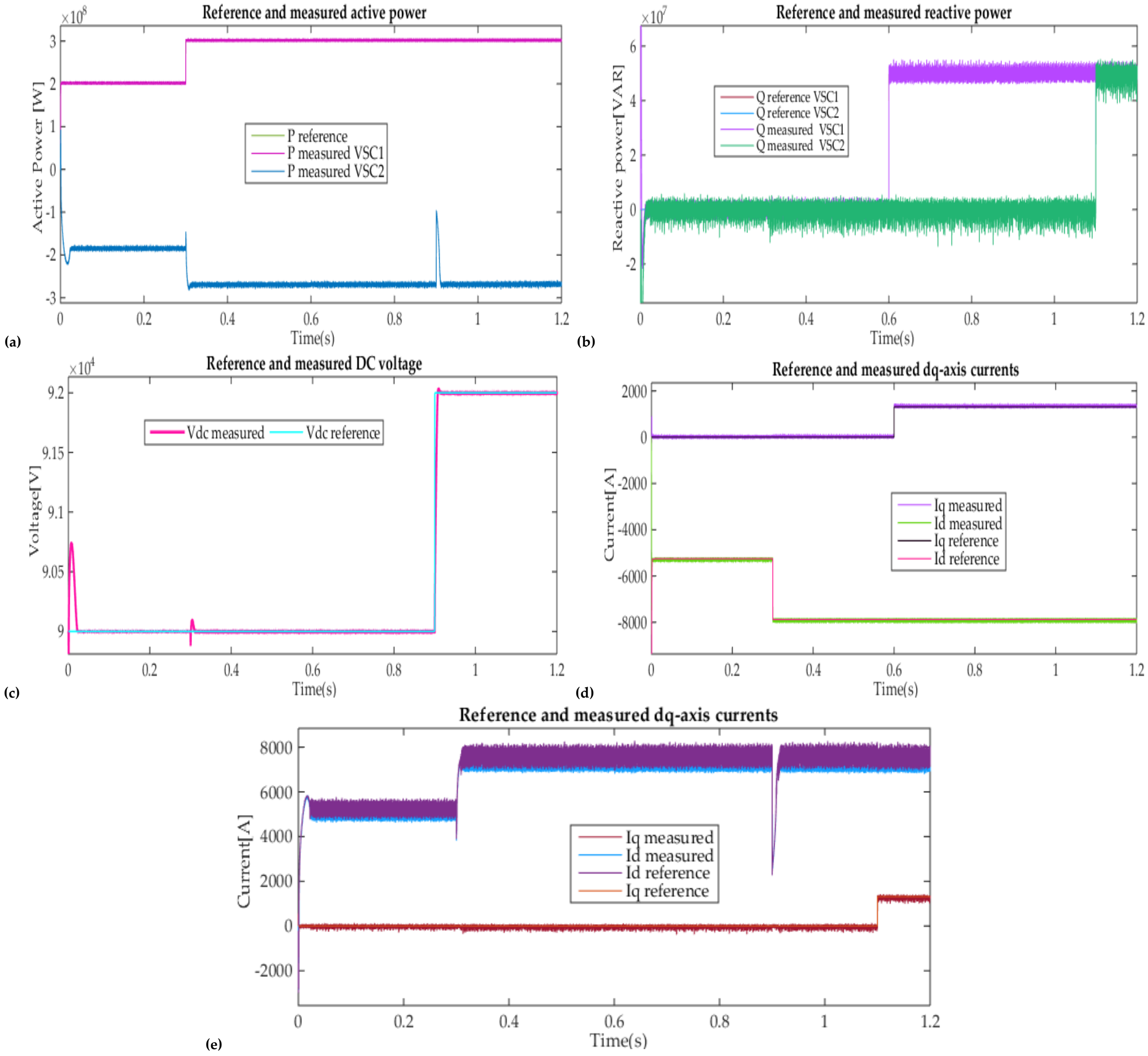
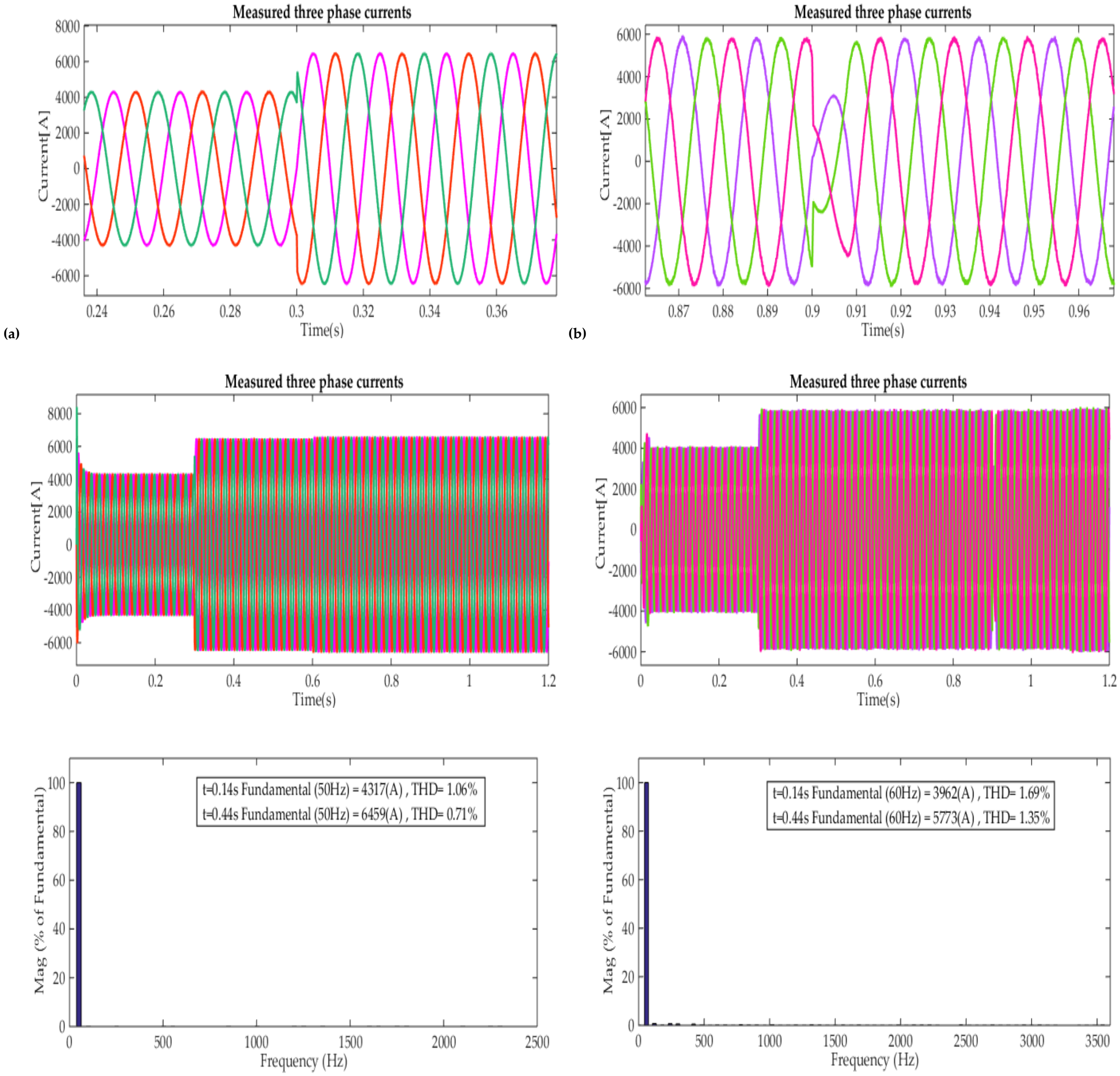


Figure (IV.30): the dynamic responses of Back-to-Back VSC-HVDC, (a) Reference and measured active powers, (b) Reference and measured reactive powers ,(c) DC-bus voltage and its reference , (d) VSC1 AC side reference and measured *dq*-axes currents ,(e) VSC2 AC side reference and measured *dq*-axes

Figures(IV.31) present the three-phase currents on both sides of the HVDC system and their harmonic spectra. As it is can be see, there is no significant difference between these curves and those obtained by simulation.



Figure(IV.31): the AC side three phase currents and the Line current harmonic spectrum for: (a) VCS1 (b)VSC2

In this section PIL tests are performed by implementing the VSC based HVDC models on the host computer using the Simulink environment while the 2-SMC controller is loaded on the STM32F407Discovery board. By examining the HVDC systems behavior during normal and transient periods, it is clear that the PIL results validate the MIL and SIL results previously presented, which means that the generated control using STM32F4 Board is able to be implemented in real time.

IV.6. Conclusion

This chapter has presented the benefits of employing the Model-Based Design approach when developing control design. The strong benefit of employing MBD is that flaws can be detected and identified in early stages of development. In addition, using this approach it is simple to try out new functions. The capability to investigate control design code before any hardware can be seen as advantage in control system design. Certainly, it is easy to see a great advantage this gives in a real development situation with many different developers working on a different section of the same project.

Simulation results confirm that there is no significant difference in performance between running Simulink in normal mode and SIL/PIL simulation. As an outcome of that, the results of co-simulation based on the MBD approach reveal that the VSC-HVDC systems based on STA controller successfully establish the powers flow control, as well as the DC voltage control. This implies that the proposed STA based on SMC can be implemented in real time application.

General Conclusion

The broad idea of this work is to develop an effective nonlinear control scheme to improve the traditional oriented vector control of VSC based HVDC systems, in which the PI control is commonly used. Indeed, employing advanced control techniques could accomplish further reliable, safe, and effective power transmission. In this context, a second order sliding mode control based on super twisting algorithm of VSC based HVDC systems was investigated and validated by SIL and PIL co-simulation tools using STM32F407VG discovery board.

In the first chapter of this memorandum, a brief overview of HVDC systems discussed in the literature was presented and then the attention was focused on VSC based HVDC system, which shows many advantages compared to the others including bidirectional power flow, independent control of active and reactive powers, and reduce network losses, to name just a few.

In the second chapter, a suitable model of the VSC based HVDC system was developed. This model is used to design conventional PI controllers needed for the oriented vector control of VSC-based HVDC systems. In addition, to enhance the DC voltage regulation a nonlinear feed-forward compensation and an extended state observer based PI control were tested. Simulation results confirm that according the adopted VSC-HVDC configuration the control system is able to ensure power transmission between two distant terminals or to connect two asynchronous grids. In this, the control of both VSC substations can regulate the active and reactive powers at each end separately.

Two nonlinear control schemes have been developed in the third chapter to stabilize, and enhance the performance of the VSC-HVDC systems and improve their dynamic behaviors in terms of control and disturbances rejection and references tracking. The first approach is based on the integral sliding mode control technique and the second strategy is based on the super twisting algorithm. Simulation results corroborate that the control of the VSC-HVDC system is completely possible using integral ISMC strategy. Improved performance and robustness in the presence of disturbances and reference value tracking are obtained compared to the traditional controllers except the chattering problem, which is the main drawback of this approach. To handle this problem while maintaining the main advantages of the conventional SMC, second order SMC is applied. The simulation results show that the use of super twisting algorithm in the VSC-HVDC systems control remarkably improves their performances and reduce the chattering in waveforms. The results show also that the super twisting algorithms is able to maintain a consistent control performance with no overshoot during the power shifts and restore the system rapidly after DC voltage reference variations. One can conclude that this method of control brings good performance and significant improvements compared to classic PI and sliding mode regulators.

To validate and examine the performance of both configurations of VSC-Based HVDC system controlled by super twisting algorithm co-simulation is performed in the fourth chapter using SIL and PIL as part of the model-based design approach. The interesting finding is that the results of VSC based HVDC co-simulations using SIL and PIL are in perfect consistent with MIL simulations. From this result, one can infer that the proposed controller is ready to be implemented in real time situation.

There are many possibilities and courses in which this work could guide to. Suggestions for future works include:

- Application of other nonlinear and intelligent control algorithms for VSC-HVDC systems;

- Enhancement of the HVDC systems by using new power converters such as modular multilevel VSC;

- Application of the dSpace based hardware in the loop HIL technique for controlling the VSC-HVDC systems;

- Extension of this study to multi-terminal HVDC systems.

Appendix A

System and Controllers Parameters

A.1)VSC-HVDC System Parameters

Parameter	Value
Max AC voltage	$V_{m1} = V_{m2} = 31.1\,k$ V
Girds frequencies	$f_1 = 50Hz$, $f_2 = 60Hz$
DC Line resistance	$R_{dc} = 3\ \Omega$
DC-Link Capacitance	$C_{dc} = 6\ mF$
Line Resistances	$R_{l1} = R_{l2} = 0.25\,\Omega$
Line Inductances	$L_{l1} = L_{l2} = 0.006\ mH$
Phased Looked Loop PI gains	$\omega_{npll} = 1800;\ \xi_{pll} = 1$
Switching Frequency	$f_s = 6kHz$

Table (A.1): VSC-HVDC System Parameters

A.2)VSC-HVDC Point to Point PI Controllers Parameters

A.2.1)PI Controllers without Compensation

Controller	Parameter	Value
First AC side line current controller	ξ_{i1}	1
	ω_{ni1}	400
Second AC side line current controller	ξ_{i2}	1
	ω_{ni2}	400
DC-link voltage controller	ξ_{dc}	0.9
	ω_{ndc}	90

Table (A.2): Parameters of PI controllers without compensation

A.2.2) PI Controllers with Nonlinear Feed-Forward Based Compensation

Controller	Parameter	Value
First AC side line current controller	ξ_{i1}	1
	ω_{ni1}	400
Second AC side line current controller	ξ_{i2}	1
	ω_{ni2}	400
DC-link voltage controller	ξ_{dc}	0.9
	ω_{ndc}	200
	k_f	36×10^3

Table (A.2): Parameters of PI controllers with nonlinear feed-forward based compensation

A.2.3) PI Controllers with Extended State Observer Based Compensation

Controller	Parameter	Value
First AC side line current controller	ξ_{i1}	1
	ω_{ni1}	500
Second AC side line current controller	ξ_{i2}	1
	ω_{ni2}	800
DC-link voltage controller	ξ_{dc}	1
	ω_{ndc}	250
	ω_{neso}	400
	ξ_{eso}	1

Table (A.3): Parameters of PI controllers without extended state observer based compensation

A.2.4) VSC-HVDC Point to Point Sliding Mode Control Parameters

Controller	Parameter	Value
First AC side line current controller	k_{i11}	10×10^5
	k_{i21}	10×10^5
	k_{i1}	1.5×10^5
Second AC side line current controller	k_{i12}	8.5×10^5
	k_{i22}	8×10^5
	k_{i2}	1.5×10^2
DC-link voltage controller	k_{dc}	20500
	k_{idc}	800

Table (A.4): Parameters of integral sliding mode controllers

A.2.5) VSC-HVDC Point to Point STA Parameters

Controller	Parameter	Value
First AC side line current controller	λ_{d1}	25×10^6
	λ_{q1}	9×10^6
	α_{d1}	3×10^5
	α_{q1}	3×10^5
Second AC side line current controller	λ_{d2}	25×10^5
	λ_{q2}	10×10^5
	α_{d2}	4×10^3
	α_{q2}	4×10^3
DC-link voltage controller	λ_{dc}	75×10^2
	α_{idc}	12×10^6

Table (A.5): Parameters of super twisting controllers

A.3)VSC-HVDC Back- to-Back PI Controllers Parameters

A.3.1) PI Controllers without Compensation

Controller	Parameter	Value
First AC side line current controller	ξ_{i1}	1
	ω_{ni1}	800
Second AC side line current controller	ξ_{i2}	1
	ω_{ni2}	800
DC-link voltage controller	ξ_{dc}	0.8
	ω_{ndc}	300

Table (A.6): Parameters of PI controllers without compensation

A.3.2) PI Controllers with Nonlinear Feed-Forward Based Compensation

Controller	Parameter	Value
First AC side line current controller	ξ_{i1}	1
	ω_{ni1}	400
Second AC side line current controller	ξ_{i2}	1
	ω_{ni2}	400
DC-link voltage controller	ξ_{dc}	0.9
	ω_{ndc}	300
	k_f	50×10^3

Table (A.7): Parameters of PI controllers with nonlinear feed-forward based compensation

A.3.3) PI Controllers with Extended State Observer Based Compensation

Controller	Parameter	Value
First AC side line current controller	ξ_{i1}	1
	ω_{ni1}	500
Second AC side line current controller	ξ_{i2}	1
	ω_{ni2}	800
DC-link voltage controller	ξ_{dc}	1
	ω_{ndc}	250
	ω_{neso}	400
	ξ_{eso}	0.7

Table (A.8): Parameters of PI controllers without extended state observer based compensation

A.3.4) VSC-HVDC Back- to-Back Sliding Mode Control Parameters

Controller	Parameter	Value
First AC side line current controller	k_{i11}	10×10^7
	k_{i21}	6×10^7
	k_{i1}	1 ×10^2
Second AC side line current controller	k_{i12}	15×10^8
	k_{i22}	8×10^8
	k_{i2}	1×10^2
DC-link voltage controller	k_{dc}	50060
	k_{idc}	680

Table (A.4): Parameters of integral sliding mode controllers

A.3.5) VSC-HVDC Back- to-Back STA Parameters

Controller	Parameter	Value
First AC side line current controller	λ_{d1}	25×10^6
	λ_{q1}	9×10^6
	α_{d1}	3×10^5
	α_{q1}	3×10^5
Second AC side line current controller	λ_{d2}	25×10^5
	λ_{q2}	18×10^5
	α_{d2}	4×10^3
	α_{q2}	5×10^3
DC-link voltage controller	λ_{dc}	85×10^2
	α_{dc}	18×10^6

Table (A.5): Parameters of super twisting controllers

Appendix B

PIL Simulation Software Requirements

This index aims to clarify which software are required in order to carry out Matlab/Simulink from MathWorks (version R2014b or later).

Environment for graphical modeling, simulating and analyzing dynamical systems, based on the interconnection of high-level blocks that represents logical and mathematical functions. Some add-ons are required for this work:

B.1.Embedded Coder

Embedded Coder generates readable, compact, and fast C and C++ code for embedded processors used in mass production. It extends MATLAB Coder and Simulink Coder with advanced optimizations for precise control of the generated functions, files, and data. These optimizations improve code efficiency and facilitate integration with legacy code, data types, and calibration parameters. You can incorporate a third-party development tool to build an executable for turnkey deployment on your embedded system or rapid prototyping board.

B.2. Embedded Coder Support Package for STMicroelectronics Discovery Boards

Embedded Coder Support Package for STMicroelectronics Discovery Boards provides support to Embedded Coder that includes automated build and execution, processor-optimized code for ARM Cortex-M.

This toolbox is provided by MathWorks. The package can be installed from MATLAB going to Add-Ons>> Get Hardware Support Packages. After choosing the installation method, select the package STMicroelectronics STM32F4-Discovery and continue with the installation. Some additional packages may be automatically installed or updated, such as the GNU Toolchain. At some point of the process, the installer will ask the user to provide the path of the Cortex Microcontroller Software Interface Standard (CMSIS) folder. The latest CMSIS is available for download at the official webpage [68][69]. The CMSIS is a third party hardware abstraction layer (HAL) for Cortex-M processors; this layer provides a standard interface for the software regardless the used hardware.

Note: a high speed internet is needed for the package to be properly installed also to avoid any error make sure to update Java SE Runtime Environment, also the Matlab need to be installed in no space directory.

B.3. STM32CubeMX

STMicroelectronics (version 4.21.0 or later) is a graphical software configuration tool that allows the generation of C initialization code for STM32 MCUs using graphical wizards.

B.4. STM32 Embedded Target toolbox

STMicroelectronics (version 4.4.2) is a Matlab extension that links a Simulink model to a STM32CubeMX file in order to enable the peripheral blocks of the STM32 MCUs. Its purpose is to graphically connect a modeled system to the MCU for generating a totally integrated code using Embedded Coder.

B.5. KEIL uVision IDE from KEIL (version 5 or later)

Integrated Development Environment with the MDK-ARM toolchain to compile and load a C project onto the STM32 MCUs. Furthermore, the STM32F4 ST-LINK must be installed in order to provide all the drivers for the STM32F4.

B.6. WaijungToolbox from Aimagin Co., Ltd

The toolbox is produced by the STMicroelectronics' and a third party member Aimagin Co., Ltd. This block set is issued for evaluation purposes only, so to get technological support as well as additional features such as approval for business use, a special license need be purchased. The toolbox can be quickly downloaded from the web site [70]. The file needs to be uncompressed and the resulting folder to be saved in a fixed path of the PC. To install the package, execute the install_waijung.m MATLAB script file that is placed inside the folder. Be certain that the STM32F4 ST-LINK is correctly installed. Nevertheless, a warning message will appear stating that the STM32F4 ST-LINK does not exist. Simply proceed with the installation process, the message is an application defect if the toolbox was not able to connect to the microcontroller re-install STM32F4 ST-LINK that is provided within the Waijung folder in >>waijung15_04a>targets>stm32f4_target>stm32f4>utils>STLinkUtility.

The package involves the GNU toolchain from ARM Cortex-M & Cortex-R processors, but the user can install its own compiler.

Once the script has been executed, the toolchain will be available to use. There is a wide quantity of usable blocks, but the essentially used will be the On-chip Peripherals of the STM32F4 Target, which are shown in Figure (B.1).

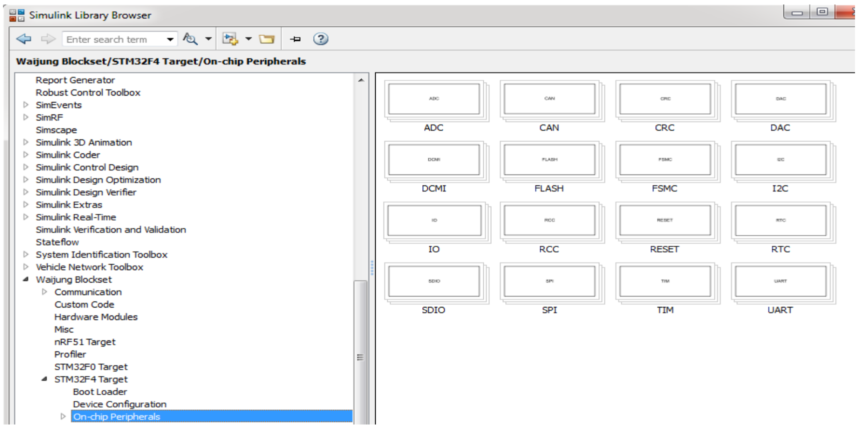


Figure (B.1): On-chip Peripherals of the STM32F4 Target

This toolbox has a broad diversity of peripherals, such as CAN (Controller Area Network) and ISP (Interface Serial Peripheral) communication. The blocks in this toolbox can be immediately configured for nearly any potential use as if programming it manually. To start the algorithm design, open a new Simulink model. Configuring the target is automatically done simply by dragging a Target Setup block into the model. This block is can found inside the Device Configuration collection block of the STM32F4 Target. Its purpose is to configure settings such as the clock or the compiler. It can be verified that the system target file has been automatically set to 'stm32f4.tlc', otherwise it should be set manually. Now the algorithm can be formulated using the required blocks. Once the design is done, it can be coded, compiled, and loaded simply by clicking the Build Model button. The benefit of this toolbox is the high level of configuration directly from Simulink. This enables the designer to save a lot of time. The simplicity and the capability of the blockset have been the reasons to choose this toolbox for generating the code and flashing the microcontroller of this project.

Appendix C
STM32F4 Application Examples

C.1. Introduction

PC users can view messages or see images via a monitor such as Cathode Ray Tube (CRT), Liquid Crystal Display (LCD) and high-resolution Light Emitting Diode (LED) monitors.For any microcontroller project, interfacing a display unit with it would make the project a lot easier and engaging for the user to interact with. The most commonly used display unit for microcontrollers is the 16×2 alphanumeric displays.

This appendix aims to make the use of the STM32f4 discovery board with the Waijung toolbox in Simulink/Matlab easy and simple. For this, an example showing how we can interface a 16×2 LCD display with the STM32F407 STM32 Development board with the Waijung toolbox in Simulink/Matlab will be detailed.

C.2 Short Introduction to 16×2 Dot-Matrix LCD Display

The Waijung toolbox in Simulink provides an easy way to use blocks, which makes the interfacing a simple process therefore it is not necessary to know anything about the display module. But, it is important to understand the basic functioning of the LCD module in use.

The LCD display includes a liquid crystal screen and control display (LCD controller). The LCD controller is responsible for controlling the message on the display screen such as line spacing, line breaks and an ON-OFF pixel to represent a character or image. Character and language, which are displayed on the screen, depend on the manufacturer.

Figure (C.1): 16x2 LCD Display Module

Figure (C.1) shows an LCD display of size 16×2. The name 16×2 implies that the display has 16 Columns and 2 Rows, which together (16×2) forms 32 boxes. One single box would resemble like that in the figure(C.2)

Figure (C.2):Single character

A single box has 40 pixels (dots) with a matrix order of 5 Rows and 8 columns, these 40 pixels together forms one character. Similarly, 32 characters can be displayed using all the boxes.

Figure (C.3) display a schematic of the LCD1602A that will be used in this appendix. The role of each pin is shown in the Table (C.1).

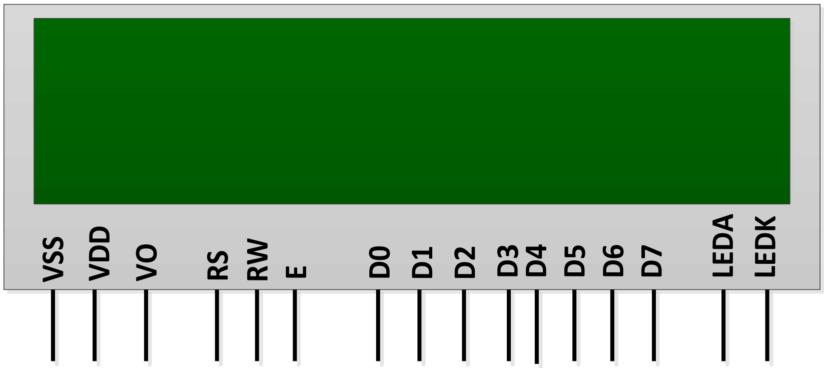


Figure (C.3): Schematic of The LCD1602A display

PinNumber	**PinName**	**Acronym**	**Pin Description**
Pin 1	VSS	Voltage Source	The ground pin of the LCD
Pin 2	VDD	Voltage Drain	The Supply voltage pin of the LCD
Pin 3	VO	Voltage Contrast	Variable voltage between 0 and 5V to adjust the contrast of the display
Pin 4	RS	Register Select	Toggles between Command/Data Register
Pin 5	RW	Read Write	Toggles the LCD between Read/Write Operation
Pin 6	E	Enable	Must be held high to perform Read/Write Operation
Pin 7 to 10	D0 to D3	Data 0 to 3	Parallel sending of 4 additional bits for an 8-bit word
Pin 11 to 14	D4 to D7	Date 4 to 7	Data transfer for 4 bits in parallel
Pin 15	LEDA	Anode	These pins are used to turn on the backlight of LCD if needed
Pin 16	LEDK	Cathode	

Table (C.1): Pins Description of a 16x2 LCD Module

C.2.1. 4-bit and 8-bit Mode of LCD

The LCD can operate in two distinctive modes, particularly the 4-bit mode and the 8-bit mode. In 4-bit mode, the data is transferred nibble by nibble, first upper nibble and then lower nibble. A nibble is a group of four bits, the lower four bits (D0-D3) that form the lower nibble, while the upper four bits (D4-D7) form the higher nibble. This enables us to send 8-bit data.

In 8-bit mode**,** 8-bit of data can be transferred directly in one stroke since we use all the 8 data lines.

However, even though the 8-bit mode is faster and flawless than 4-bit mode. But the major drawback is that it needs 8 data lines connected to the microcontroller. This will make us run out of I/O pins on our MCU, hence the 4-bit mode is widely used.

No control pins are used to set these modes; it is just the way of programming that change.

C.3. Interfacing 16X2 LCD with STM32F4

The LCD module will be configured in 4-Bit mode so that only 4 data pins are used totransmit the data that is to be displayed on the LCD.

C.3.1 Circuit Diagram

The figure (C.4) presents the schematic diagram LCD1602A for the connection to an STM32F407VG microcontroller. The components required to interface 16X2 LCD with STM32F4 are:

- STM32F4
- 16X2 Character LCD Module
- Connecting Wires
- 1k resistor
- 1k resistor or variable resistor.

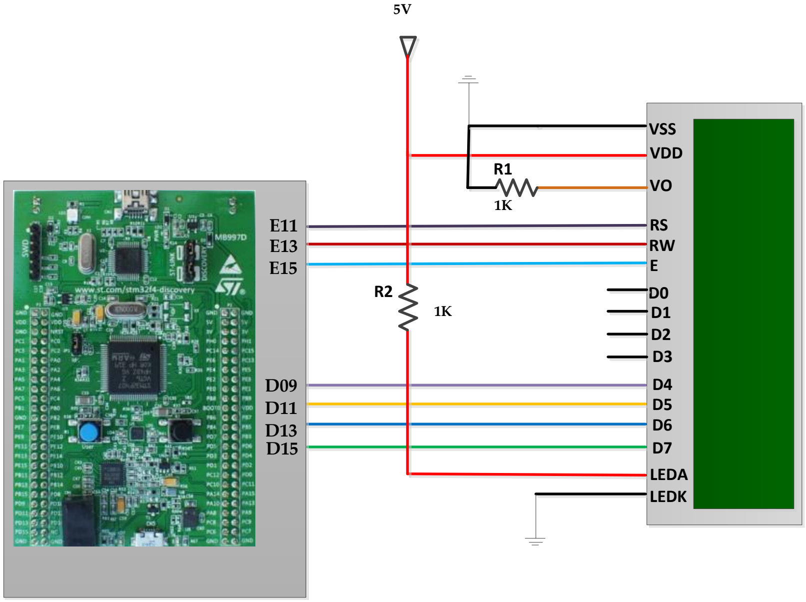
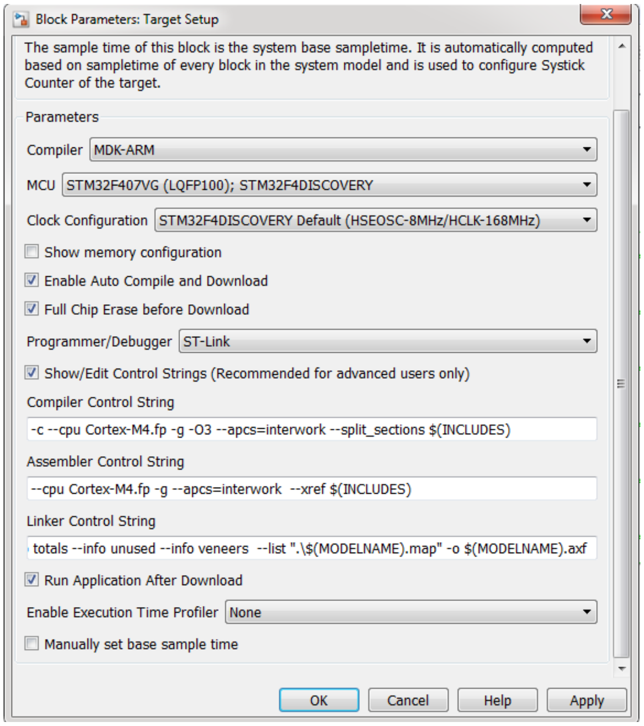


Figure (C.4): LCD1602A - STM32F4 Schematic

The LCD display is powered by 5V. The 5V and GND output pins on the STM32F4 Discovery board can be used to power it.Resistor R1 connected to pin 'VO' is a contrast adjustment setting;a0.8-1k resistor should do the job. However, in order to adjust the contrast of the display to your liking, it is recommended to replace R1 with a 1k variable resistor.

C.3.2 Peripherals Configuration in Matlab/Simulink Environment

First, After loading Matlab and Simulink the "Target Setup" block and be found the WaijungBlockset, this block is needed to generate the code for STM32F4. Double click on the Target setup, choose the desired compiler and the MCU also check the “Full chip erase before download” option is selected and click OK to save as presented in figure



The sample time of this block is the system base sampletime. It is automatically computed based on sampletime of every block in the system model and is used to configure Systick Counter of the target.

Parameters

Compiler: MDK-ARM

MCU: STM32F407VG (LQFP100); STM32F4DISCOVERY

Clock Configuration: STM32F4DISCOVERY Default (HSEOSC-8MHz/HCLK-168MHz)

☐ Show memory configuration

☑ Enable Auto Compile and Download

☑ Full Chip Erase before Download

Programmer/Debugger: ST-Link

☑ Show/Edit Control Strings (Recommended for advanced users only)

Compiler Control String

```
-c --cpu Cortex-M4.fp -g -O3 --apcs=interwork --split_sections $(INCLUDES)
```

Assembler Control String

```
--cpu Cortex-M4.fp -g --apcs=interwork  --xref $(INCLUDES)
```

Linker Control String

```
totals --info unused --info veneers  --list ".\$(MODELNAME).map" -o $(MODELNAME).axf
```

☑ Run Application After Download

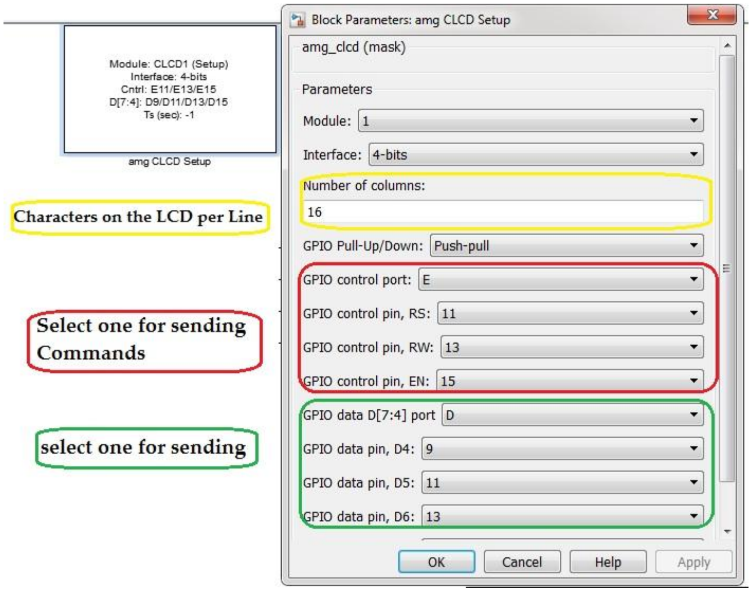
Enable Execution Time Profiler: None

☐ Manually set base sample time

Figure (C.5):Target setup configuration

In WaijungBlockset block, there is a related module called "amg CLCD Setup" in the library, which can be accessed via *WaijungBlockset>> Hardware Modules >> Character LCD >>Simple amgCLCD Display Setup >> LCD Setup*. Figure (C.5) shows the block parameters of "amg CLCD Setup".

In this example, the E-port is used for sending control commands, and the D-Port is used for sending the text, any GPIO can be used.



amg_clcd (mask)

Parameters

Module: 1

Interface: 4-bits

Number of columns: 16

GPIO Pull-Up/Down: Push-pull

GPIO control port: E

GPIO control pin, RS: 11

GPIO control pin, RW: 13

GPIO control pin, EN: 15

GPIO data D[7:4] port D

GPIO data pin, D4: 9

GPIO data pin, D5: 11

GPIO data pin, D6: 13

Characters on the LCD per Line

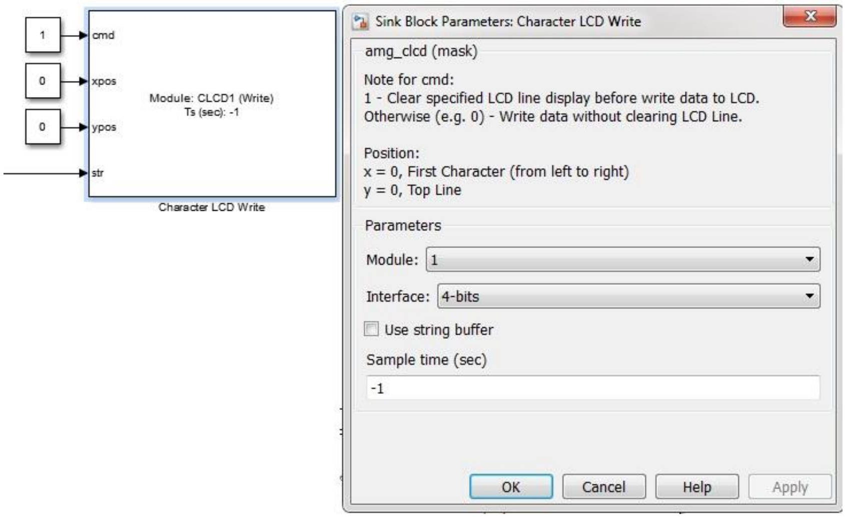
Select one for sending Commands

select one for sending

Figure (C.5): Block parameters for Character LCD Setup

The next step is to send data and display text on the LCD, this can be done by using a module called "Character LCD Write" in the library, which can be accessed via *WaijungBlockset*>> *Hardware Modules* >> *Character LCD*. Figure (C.6) shows the block parameters of "Character LCD Setup".

In order to send the data to the LCD, the coordinates (xpos, ypos) need to be mention, (0, 0) is the point at the top left corner of the screen (which is the starting and reference point) and (15, 2) is at the bottom right corner, which is the last one. As it is shown figure (C.6); the “CMD” input is set to one to clean the screen and the coordinates (xpos, ypos) are set to (0, 0).



amg_clcd (mask)

Note for cmd:
1 - Clear specified LCD line display before write data to LCD.
Otherwise (e.g. 0) - Write data without clearing LCD Line.

Position:
x = 0, First Character (from left to right)
y = 0, Top Line

Parameters

Module: 1

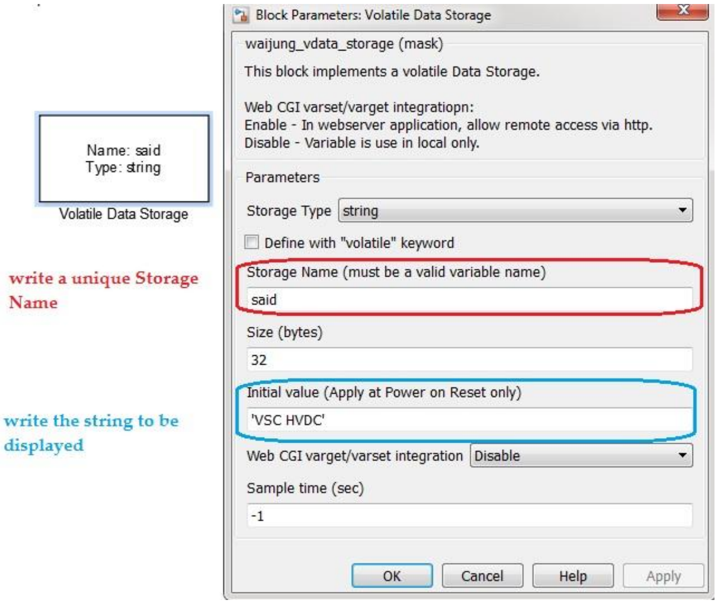
Interface: 4-bits

☐ Use string buffer

Sample time (sec): -1

Figure (C.6): Parameters for Character LCD Write Block

Character LCD Write Block is a text input block for display and is used for message passing using a "volatile data storage Read" block. The "Volatile Data Storage" block that is used to store the data that will be displayed. Both located in *Simulink Library >>WaijungBlockset>>Misc>> Data Storage*.



write a unique Storage Name

write the string to be displayed

waijung_vdata_storage (mask)

This block implements a volatile Data Storage.

Web CGI varset/varget integratiopn:
Enable - In webserver application, allow remote access via http.
Disable - Variable is use in local only.

Parameters

Storage Type: string

☐ Define with "volatile" keyword

Storage Name (must be a valid variable name): said

Size (bytes): 32

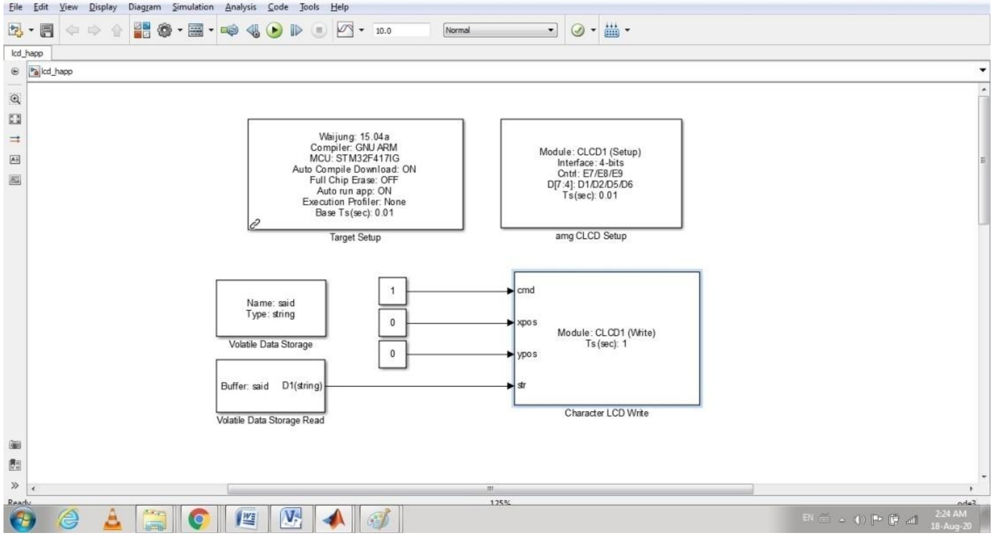
Initial value (Apply at Power on Reset only): 'VSC HVDC'

Web CGI varget/varset integration: Disable

Sample time (sec): -1

Figure (C.7): Characteristics of Volatile Data Storage Block

The name of the storage name should be unique and the initial value box is the text to be displayed, as it is shown in the figure (C.8).



Waijung: 15.04a
Compiler: GNU ARM
MCU: STM32F417IG
Auto Compile Download: ON
Full Chip Erase: OFF
Auto run app: ON
Execution Profiler: None
Base Ts(sec): 0.01

Module: CLCD1 (Setup)
Interface: 4-bits
Cntrl: E7/E8/E9
D[7:4]: D1/D2/D5/D6
Ts(sec): 0.01

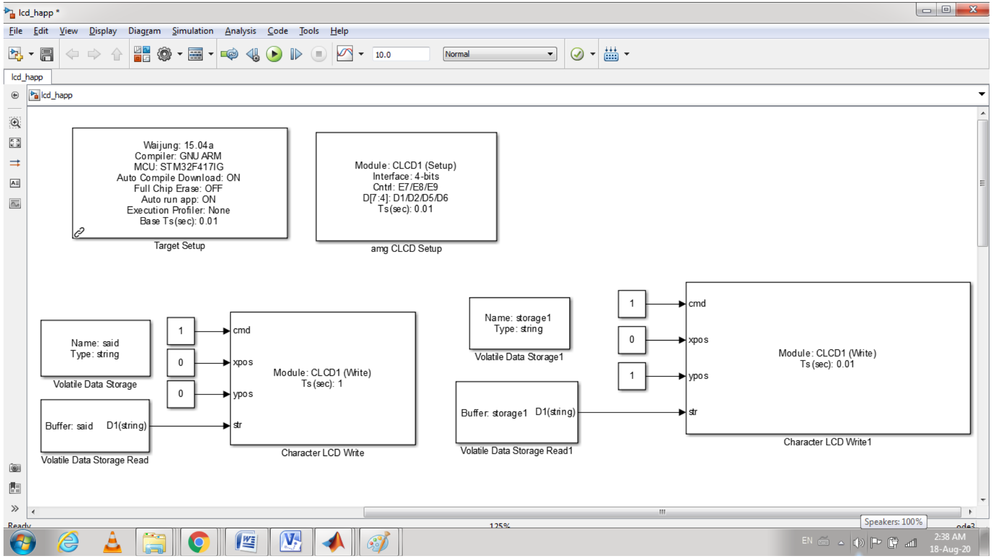
Module: CLCD1 (Write)
Ts (sec): 1

Figure (C.8): Simulink model for two line LCD display

As it appear in the figure (C.8), the “volatile data storage Read” block is set to buffer the string in the “volatile data storage” named “said” in this example.

- When using the string buffer, the user must add "volatile data storage read" block for reading text from a variable and a character LCD Write Block;
- When using string buffer, user need to define variables to be displayed in "character LCD Write Block".

To use the second line in the LDC display the same process is repeated where a new "Character LCD Write" should be used, in which the coordinates (xpos, ypos) are set to (0, 1). Alongside with new "volatile data storage Read" and "Volatile Data Storage" blocks;as it is presented in figure (C.9).



Waijung: 15.04a
Compiler: GNU ARM
MCU: STM32F417IG
Auto Compile Download: ON
Full Chip Erase: OFF
Auto run app: ON
Execution Profiler: None
Base Ts(sec): 0.01

Module: CLCD1 (Setup)
Interface: 4-bits
Cntrl: E7/E8/E9
D[7:4]: D1/D2/D5/D6
Ts(sec): 0.01

Name: said
Type: string

Buffer: said D1(string)

Module: CLCD1 (Write)
Ts (sec): 1

Name: storage1
Type: string

Buffer: storage1 D1(string)

Module: CLCD1 (Write)
Ts (sec): 0.01

Figure (C.9): Simulink model for two line LCD display

C.4ExperimentalResults

Figure (C.10)shows the resultsobtained after loading the Simulink model to the STM32F4.

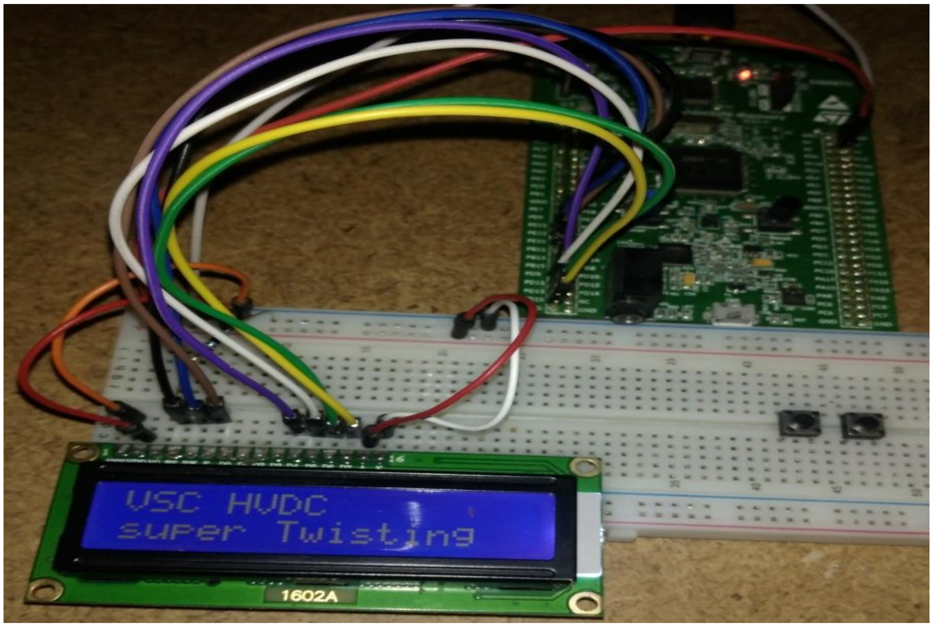


Figure (C.10): LCD display connected to an STM32F4

C.5 Analog to Digital and Digital to Analogue Conversion

Applications of embedded systems are in all domain of life including control, instrumentation system, robotics, and electrical appliance. In instrumentation systems, sensors play an important role in detecting/measuring a physical quantities such as distance, speed, force, pressure, humidity, light intensity, temperature, etc. The next step is to convert these properties into electrical signals, which are mostly analogue voltage (0-5V) or current (4-20mA).

A physical quantity cannot only be detected by the microcontroller analogue pin but can also be detected by the digital I/O depending upon the need of the application. For example, in case of a photodiode; which is a device that converts the light energy to the current, the current can be fed to an analogue I/O or digital I/O. If that current is applied to the analogue I/O then the I/O pin will read the value between 0-1024, which can be then interpreted between 0-5V by scaling. If the photodiode current is applied to the digital I/O, it will classify it either '0' or '1' based on the defined threshold.

Data received from the sensor or the data, which is being processed inside the microcontroller, requires sometime the analogue to digital conversion or digital to analogue conversion. This makes the data fit to become the input or output of a certain modules. This requires the presence of a module Analog to Digital Converter (ADC) or Digital to Analog Converter (DAC) inside the microcontroller. Most of the modern MCUs have these modules and STM32F4DISCOVERY is no exception to it.

C.5.1 Number of Channels

Number of channels of analogue signals can be known from the datasheet of the microcontroller. Figure (C.11) highlights the pins for ADC to read the voltage from an external device and DAC to send voltage to external devices.

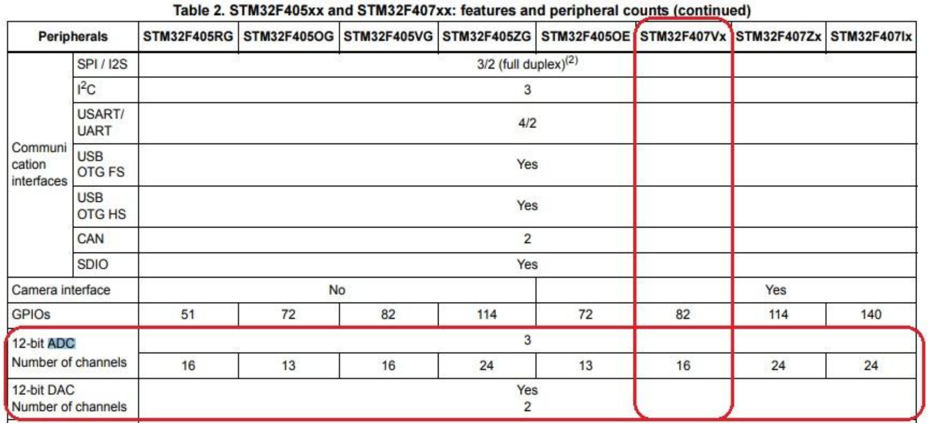


Table 2. STM32F405xx and STM32F407xx: features and peripheral counts (continued)

Peripherals		STM32F405RG	STM32F405OG	STM32F405VG	STM32F405ZG	STM32F405OE	STM32F407Vx	STM32F407Zx	STM32F407Ix
Communi cation interfaces	SPI / I2S	3/2 (full duplex)(2)							
	I^{2}C	3							
	USART/ UART	4/2							
	USB OTG FS	Yes							
	USB OTG HS	Yes							
	CAN	2							
	SDIO	Yes							
Camera interface		No				Yes			
GPIOs		51	72	82	114	72	82	114	140
12-bit ADC		3							
Number of channels		16	13	16	24	13	16	24	24
12-bit DAC Number of channels		Yes 2							

Figure (C.11): ADC and DAC modules for STM32F4DISCOVERY [71]

C.5.2Voltage Characteristics

Figure (C.12) shows the voltage characteristics of the ADC. The conversion of voltage range should be between 0V to VREF+. Power reference voltage should not exceed 3.6V and should not be less than 1.8V.

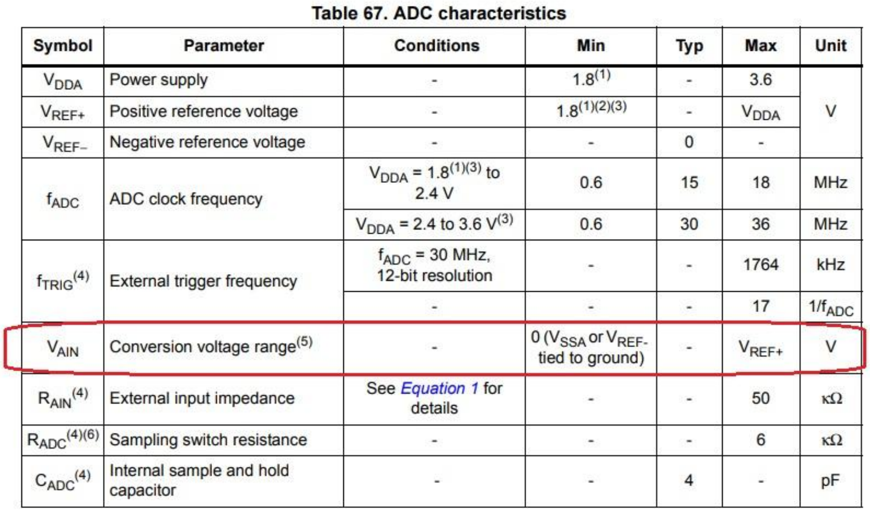


Table 67. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	1.8(1)	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.8(1)(2)(3)	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	-	0	-	
f_{ADC}	ADC clock frequency	V_{DDA} = 1.8(1)(3) to 2.4 V	0.6	15	18	MHz
		V_{DDA} = 2.4 to 3.6 V(3)	0.6	30	36	MHz
f_{TRIG}(4)	External trigger frequency	f_{ADC} = 30 MHz, 12-bit resolution	-	-	1764	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(5)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(4)	External input impedance	See *Equation 1* for details	-	-	50	κΩ
R_{ADC}(4)(6)	Sampling switch resistance	-	-	-	6	κΩ
C_{ADC}(4)	Internal sample and hold capacitor	-	-	4	-	pF

Figure (C.12): ADC characteristics [71]

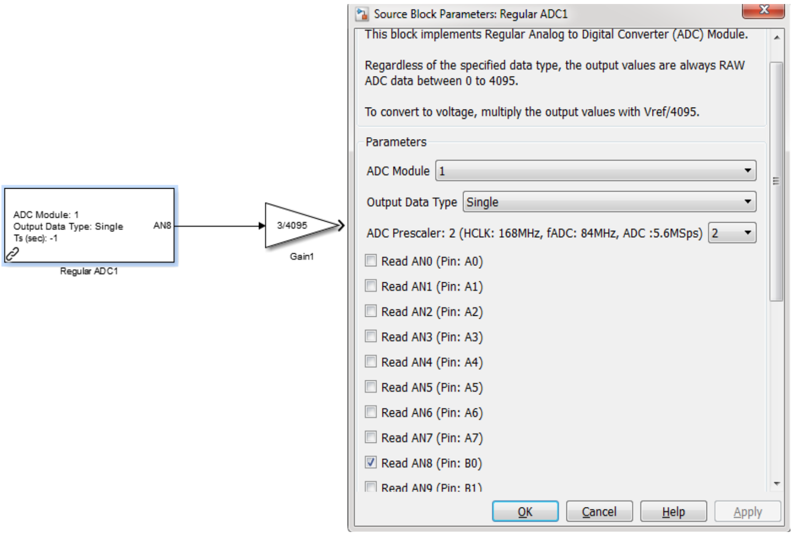
C.5.3**ADC peripherals on an STM32F407VG**

The STM32F407 has three 12-bit analogue-to-digital converters are embedded and each ADC shares up to 16 external channels (as highlighted in the figure(C.12)) that can be used to convert analogue voltage signal to digital signals.

C.5.4**Analog-to-Digital Converter Configuration**

In this example and the next one, the nominal value of 3 volts is used.

The typical configuration used in this project for ADC reading is shown in figure (C.13).Regular ADC block converts the analog signal into digital data. Regular ADC block has the following characteristics.



Source Block Parameters: Regular ADC1

This block implements Regular Analog to Digital Converter (ADC) Module.

Regardless of the specified data type, the output values are always RAW ADC data between 0 to 4095.

To convert to voltage, multiply the output values with Vref/4095.

Parameters

ADC Module 1

Output Data Type Single

ADC Prescaler: 2 (HCLK: 168MHz, fADC: 84MHz, ADC :5.6MSps) 2

- ☐ Read AN0 (Pin: A0)
- ☐ Read AN1 (Pin: A1)
- ☐ Read AN2 (Pin: A2)
- ☐ Read AN3 (Pin: A3)
- ☐ Read AN4 (Pin: A4)
- ☐ Read AN5 (Pin: A5)
- ☐ Read AN6 (Pin: A6)
- ☐ Read AN7 (Pin: A7)
- ☑ Read AN8 (Pin: B0)
- ☐ Read AN9 (Pin: B1)

Figure (C.13): Parameters for Regular ADC block

The ADC port output is an integer value between 0 and 4095 regardless of the selected data output. This range is given by the fact that the ADCsimplemented in the STM32F4 have 12- bits resolution. In this example, the output has been set to single, but it can be set to a fitter range data type as long as the consistency of the signals is kept along with the algorithm.

It is not convenient to display the values from 0 to 4095 on STM32F4. The values from 0 to 4095 do not give us meaningful information therefore it is better to translate this information from 0 to 3V. Thus, the ADC port output is translated into volts by multiplying it by again according to the equation (C.1).

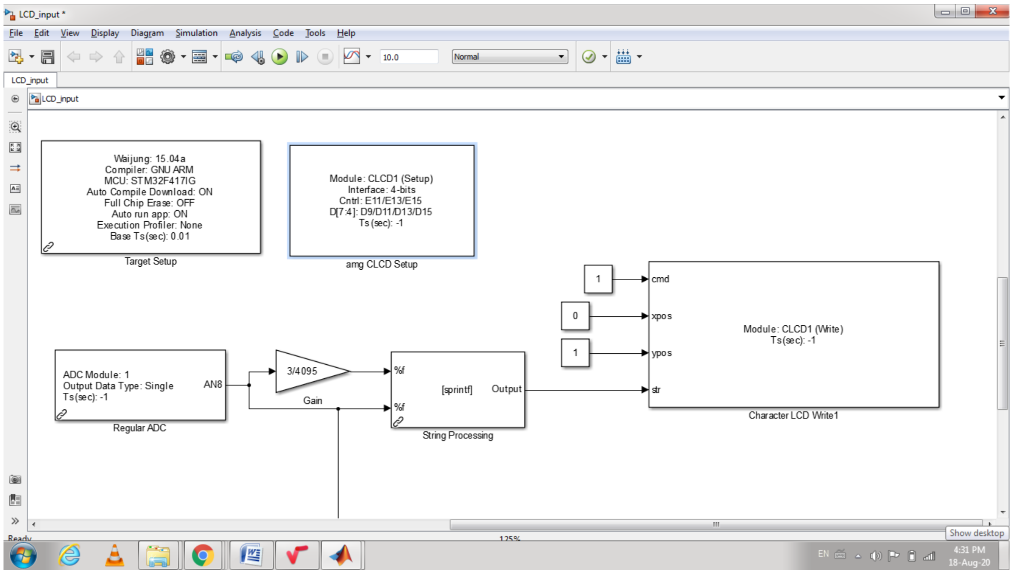
$$V_{port} = \frac{U_{port} V_{ref}}{4095} \tag{C.1}$$

where U_{port} is the raw reading from 0 to 4095, V_{ref} is the reference voltage and V_{port} is the read voltage in volts.

Finally, the sample time must be set to T_s. Here, a single ADC1 port is read, but more pins can be selected from the same ADCx block. To use another ADC, say ADC2, an additional Regular ADC block must be inserted.

C.5.5Using the Display of the LCD

The data processed through ADC can be visualized through the LCD panel connected to the microcontroller. This can be shown in Figure (C.14).



Waijung: 15.04a
Compiler: GNU ARM
MCU: STM32F417IG
Auto Compile Download: ON
Full Chip Erase: OFF
Auto run app: ON
Execution Profiler: None
Base Ts(sec): 0.01

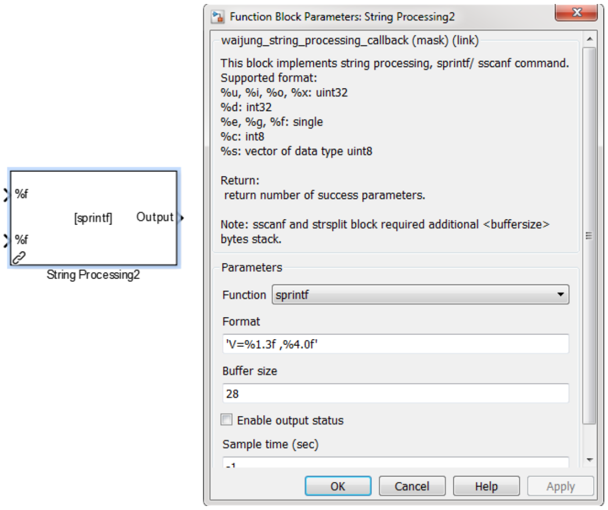
Module: CLCD1 (Setup)
Interface: 4-bits
Cntrl: E11/E13/E15
D[7:4]: D9/D11/D13/D15
Ts(sec): -1

ADC Module: 1
Output Data Type: Single
Ts(sec): -1

Module: CLCD1 (Write)
Ts(sec): -1

Figure (C.14): Simulink model for displaying the value of ADC using LCD display

The "String Processing" module can be selected for the blockset *in Simulink library>>WaijungBlockset>>Misc>> String Manipulate. Where it will use the input value and replace it with a %f in the output as it is shown in the figure (C.15).*



Function Block Parameters: String Processing2

waijung_string_processing_callback (mask) (link)

This block implements string processing, sprintf/ sscanf command.
Supported format:
%u, %i, %o, %x: uint32
%d: int32
%e, %g, %f: single
%c: int8
%s: vector of data type uint8

Return:
return number of success parameters.

Note: sscanf and strsplit block required additional <buffersize> bytes stack.

Parameters

Function: sprintf

Format: 'V=%1.3f ,%4.0f'

Buffer size: 28

☐ Enable output status

Sample time (sec): -1

Figure (C.15): Characteristics of String Processing Block.

Note: The first number after the % sign is the number of spaces allocated for the number to be displayed on the LCD. The second number, which comes after the dot is the specifier of the number of digits after the decimal point for the number to be displayed on the LCD. For example %1.3 will display a one number and 3 digits after the decimal point.

C.5.6 Experimental results

In this example, we will measure the voltage of a 1.2V of the battery shown in figure (C.16).

Figure (C.16): 1.2V battery

The battery has showed a measurement of 1.33V on the Multimeter as presented in figure (C.17).

Figure (C.17): the measurement of the 1.2V shown on the Multitester

Figure (C.18) shows the value measured by the STM32F407VG and displayed on the LCD.

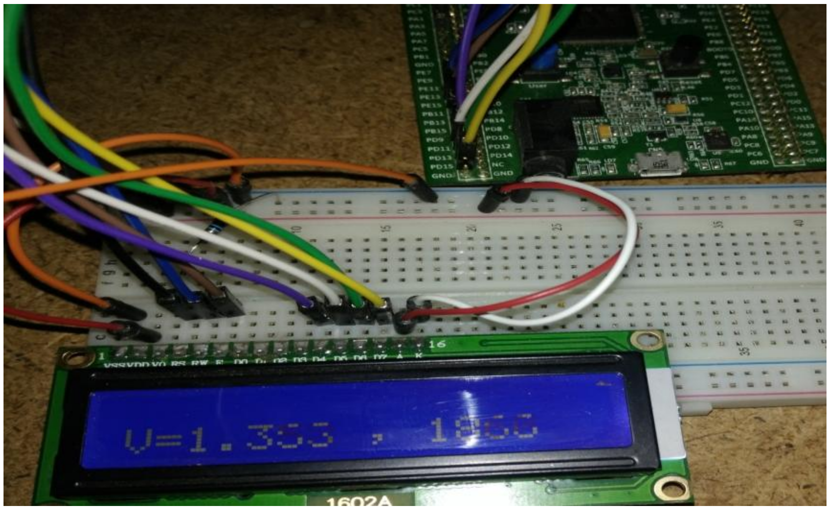


Figure (C.18): Battery voltage measurement of the ADC shown on the LCD

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Abstract:

Nowadays, enhancing the performance and operation of power transmission is necessary due to the persistent increase in the need for electric power. One new engaging technology that facilitates the control of power flow and offers extra degrees of freedom is Voltage-Source Converter High Voltage Direct Current (VSC-HVDC) transmission. The main aims of this work are stabilizing and controlling the transmitted powers, regulating the DC-bus voltage, and achieving the highest sources power factor. To achieve these goals, a second-order sliding mode control based on a super twisting algorithm is proposed to control the VSC-Based HVDC systems. This control strategy has as objectives to enhance the system performances and resolve some limitations of the conventional first-order integral sliding mode control and PI-based regulators. For this, all the controllers are designed based on a suitable model of the VSC based HVDC system and validated by SIL and PIL co-simulation tools using STM32F407VG discovery board. This gives an idea on their feasibility of implementation in real time.

Key words: HVDC system; Integral sliding mode control; Second order sliding mode control; super twisting algorithm, Software-in-the loop, Process-in-the-loop.

Résumé :

De nos jours, il est nécessaire d'améliorer les performances et le fonctionnement du transport d'énergie en raison de l'augmentation constante des besoins en énergie électrique. Une nouvelle technologie intéressante qui facilite le contrôle du flux d'énergie et offre des degrés de liberté supplémentaires est la transmission de courant continu à haute tension (CCHT)à base de convertisseurs de tension (VSC). Les principaux objectifs de ce travail sont la stabilisation et le contrôle des puissances transmises, la régulation de la tension du bus continu et l'obtention de facteur de puissance des sources le plus élevé possible. Pour atteindre ces objectifs, une commande par mode glissant de second ordre basée sur un algorithme de super twisting est proposée pour contrôler les systèmes CCHT à base de VSC. Cette stratégie de contrôle a pour objectif d'améliorer les performances du système et de résoudre certaines limitations de la commande par mode glissant intégrale de premier ordre classique ainsi que celles de la commande à base de régulateurs PI. Pour ce faire, tous les régulateurs sont conçus sur la base d'un modèle approprié du système CCHT à base de VSC et validés par des outils de co-simulation SIL et PIL utilisant la carte discovery STM32F407VG. Cela donne une idée sur leur faisabilité de mise en œuvre en temps réel.

Mots clés : Système CCHT ; Commande par mode glissant intégrale; Commande par mode glissant de second ordre ; Algorithme super twisting, Logiciel dans la boucle, Processus dans la boucle.