MOHAMED BOUDIAF UNIVERSITY OF M'SILA
FACULTY OF TECHNOLOGY
DEPARTMENT OF ELECTRONICS

جامعة محمد بوضياف – المسيلة
كلية التكنولوجيا
قسم الإلكترونيك

جامعة محمد بوضياف - المسيلة
Université Mohamed Boudiaf - M'sila

الرقم : ..../ق.إ/2025 المسيلة في : 2025/11/24

شهادة إدارية

بعد الإطلاع على التقارير الايجابية الواردة من السادة الخبراء أعضاء لجنة دراسة المطبوعة الجامعية والاتية أسماؤهم:

- بن ذيب سارة أستاذ محاضر "أ" جامعة محمد البشير الابراهيمي– برج بوعريريج
- ظريف محمود أستاذ محاضر "أ" جامعة محمد بوضياف – المسيلـــة
- بختي الهادي أستاذ محاضر "أ" جامعة محمد بوضياف – المسيلـــة

صادق أعضاء اللجنـة العلميـة على قبول المطبوعة البيداغوجية مع إمكانية إتخاذها سندا في تدريس طلبة السنة الاولى ماستر ميكروالكترونيك، في ميدان علوم و تكنولوجيا و أن تعتمد في أي تقييم المسار العلمي للأستاذ المعني حرحوز أحلام (أستاذ محاضر قسم "أ"– جامعة محمد بوضياف - المسيلة) تحت عنوان :

Simulation tools (TP)

رئيس القسم رئيس اللجنة العلمية

بوراس منير

طباخ مصطفى

PEOPLE'S DEMOCRATIC REPUBLIC OF ALGERIA
MINISTRY OF HIGHER EDUCATION
AND SCIENTIFIC RESEARCH
Mohamed Boudiaf University - M'sila

M1-Microelectronic
Department of electronics

Practical work

Simulation tools

Dr. HARHOUZ Ahlam

Structuring and Planning of Practical Work

Generalities

Practical work: Simulation Tools

This module focuses on the essential tools and techniques for simulating electronic circuits, specifically using SPICE (Simulation Program with Integrated Circuit Emphasis). It is designed to equip students and professionals with the knowledge needed to analyze and optimize circuit designs before implementation.

Module Information

Faculty: Technologies

Department: Electronics

Target audience: Master 1, specialty Micro-Electronics

Title: PW Simulation Tools

Schedule:

- **VHS (Course Time):** 22:30
- **PW (Practical Work Duration):** 1 hour 30 minutes

Credits: 2

Coefficient: 1

Evaluation Method: Continuous Assessment 100%

Teacher:

Dr. Ahlam HARHOUZ

Contact: by email at ahlam.harhouz@univ-msila.dz

Access link

https://moodle.univ-msila.dz/moodle/course/view.php?id=1726

Objectives:

- **Understand Simulation Concepts**: Learn the importance of circuit simulation in the design process.
- **Master SPICE Commands**: Familiarize yourself with the syntax and commands used in SPICE for various analyses.
- **Perform Different Analyses**: Conduct DC, AC, and transient analyses to evaluate circuit behavior under different conditions.
- **Interpret Simulation Results**: Analyze output data and visualize results using graphical representations.

Topics Covered:

1. **Introduction to SPICE**: Overview of the software and its capabilities.
2. **Circuit Design Basics**: How to create and edit circuit schematics.
3. **Types of Analyses**:
    - **DC Analysis (.DC)**
    - **AC Analysis (.AC)**
    - **Transient Analysis (.TRAN)**

4. **Component Modeling**: Understanding how to define and characterize both linear and nonlinear components.
5. **Simulation Workflow**: Steps from circuit creation to result analysis.
6. **Case Studies**: Practical examples of circuit simulations and real-world applications.

Prerequisites:

- Basic understanding of electrical engineering principles.
- Familiarity with circuit components and their functions.

Learning Outcomes:

By the end of this module, participants will be able to:

- Set up and simulate electronic circuits using SPICE.
- Interpret the results of different types of analyses.
- Utilize simulation tools to enhance circuit design efficiency.

This module is essential for anyone looking to deepen their understanding of electronic circuit design and simulation techniques.

Practical work Content

PW1: Introduction to the PSpice Simulator

- Overview of the PSpice interface and tools.
- Basic circuit setup and first simulations.
- Analysis of a voltage follower.
- Simulation of a Darlington pair.
- Study of a current source.
- Implementation of a current mirror.

PW2: Simulation of Fundamental Circuits with Bipolar Junction Transistors (BJTs)

PW3: Simulation of a Follower and Inverter Using Bipolar Technology

PW4: Simulation and Analysis of Class A Amplifier using SPICE

- Design and analysis of a Class A amplifier circuit.
- Evaluation of performance metrics.

PW4: Simulation of Amplifiers with Different Input Sources

PW5: Simulation of a NAND Gate in ECL Technology

- Understanding the implementation of digital logic in ECL.
- Analyzing the behavior of a NAND gate circuit.

PW n°.1 : Introduction to the SPICE Simulator

(The first SPICE commands / Study and simulation of passive circuits)

Conduct of the experiment.: ………. /……../………….. .

Hourly volume: 2^h.

Report made by:

Family name	First name	**Group**	**Final mark 20/20**
- - -	- - -	- - -	- - -

Instructions:

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   - **Names and surnames of the lab participants.**
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   - **Preparation and work should be handwritten.**

Goals:

- ✓ Introduction to the PSPICE simulator (OrCAD Capture + OrCAD PSpice A/D tools).
- ✓ Familiarization with three common analyses in electronics: OP, AC, TRAN.
- ✓ Theoretical study of the schematic, simulation, and quantitative interpretation of the results.

I. The PSPICE Environment:

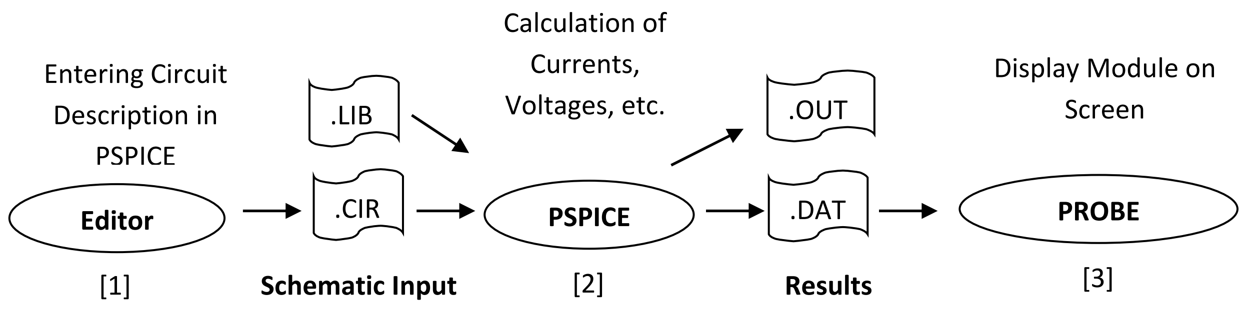


Figure.1: PSPICE Environment

[1] EDITOR: There are 2 ways to describe the circuit to be simulated:

Description by a schematic: In this case, the graphical editor CIS provided in the PSPICE installation package is used. To simulate the operation of a circuit, it must first be described. This can be done by drawing the schematic (CAPTURE). Once the drawing is complete, the software constructs a "netlist," which is a textual description of the circuit, along with a file with the .CIR extension.

Description by a text file: Either using PSPICE or a text editor like NOTEPAD on Windows. The file must have the .CIR extension.

[2] PSPICE: It reads the .CIR file: either one written by the user or one generated by the graphical editor. PSpice performs the requested calculations, provides important information in a .OUT file, and stores the results in a .DAT file, intended for curve plotting software.

[3] PROBE: The "PROBE" display module uses the .DAT file and presents the requested curves on the screen.

II. Electrical Schematic and Simulation Parameters (PSPICE A/D)

With PSPICE, the entry of electrical schematics is done through the PSPICE A/D tool, where the topology of the circuit is obtained from a circuit schematic editor.

You can create the circuit diagram using the graphical interface, placing components and connecting them as needed. Once the schematic is complete, you can set up the simulation parameters to analyze the circuit's behavior under different conditions.

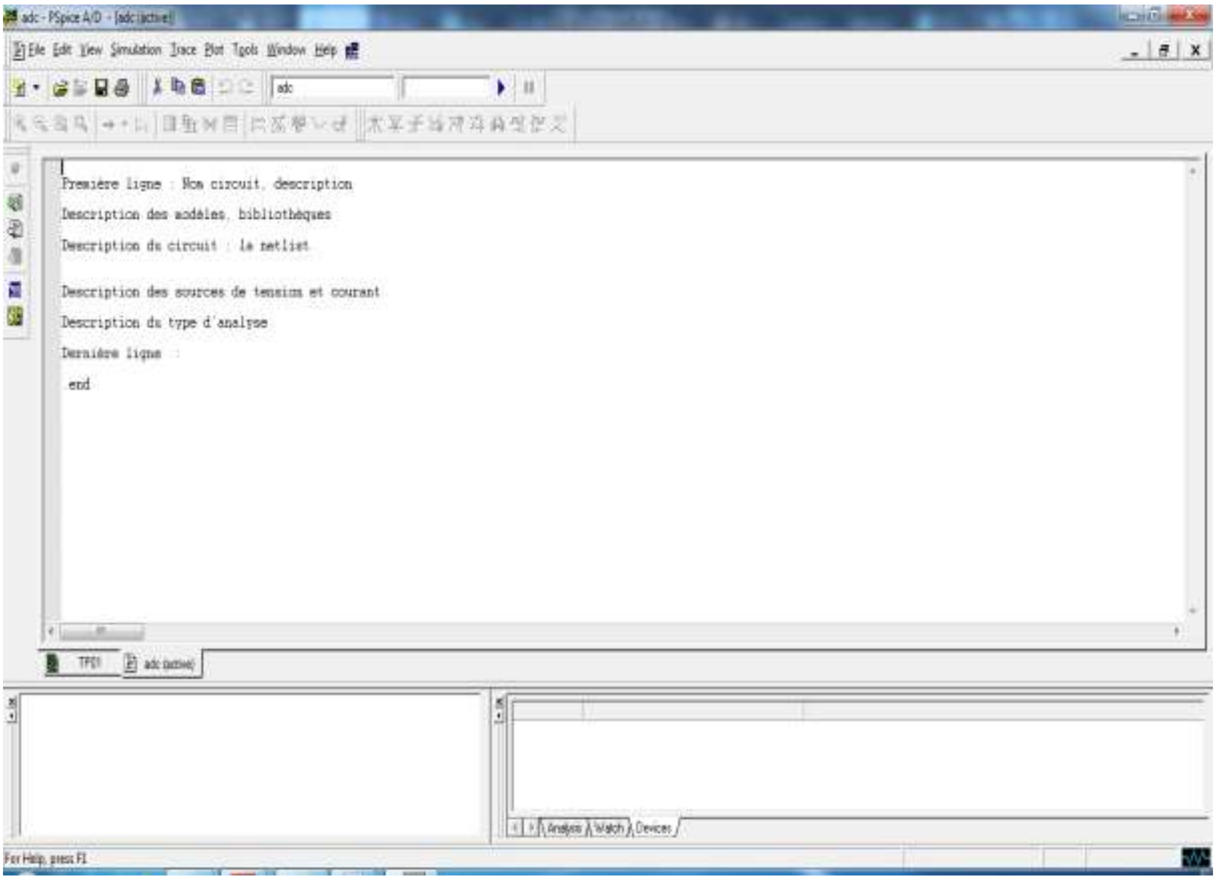


Figure.2 : PSPICE Editor

A text file (**.CIR**) is necessary to describe the circuit and specify the analyses to be performed for simulation in PSPICE. The section describing the components and their interconnections is included directly in the **.CIR** file.

To create or edit **.CIR** text files, you can use the editor in PSPICE via: File -> New -> Text File.

In a PSpice Netlist file (**.CIR**), you must describe the components and the interconnections between the elements of the circuit to be simulated. You can also indicate the libraries (for example: **.LIB** "**NAME.LIB**") to be read, which contain the circuit elements, along with directives for the simulation analyses. Finally, you conclude the program with **.END**.

II.1 Simulation Procedure

After describing the circuit schematic in the PSpice Netlist, it is necessary to define the simulation profile. This involves specifying the electrical quantities whose values you want to determine, the type of simulation desired (transient mode **.TRAN**, static mode **.DC**, frequency study **.AC**), and the duration of the simulation.

To initiate the simulation, simply click on: **Simulation -> Run**.

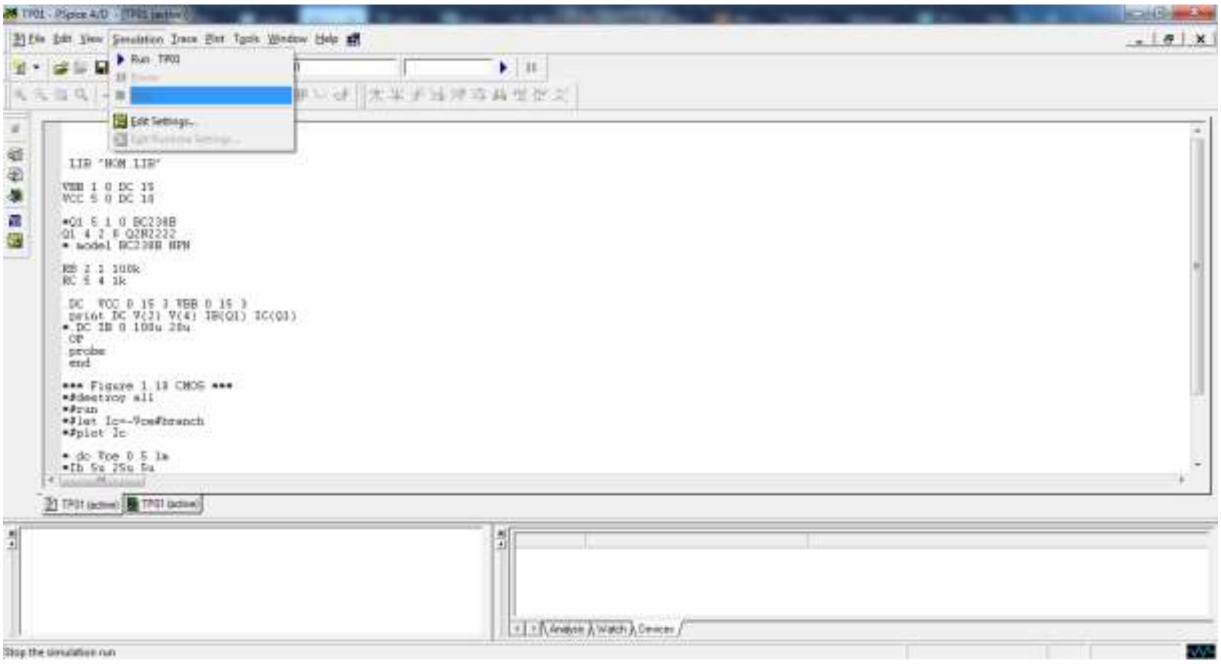


Figure.3 : Executing the Simulation

- **Prepare the Netlist**: Ensure that your PSpice Netlist file (.CIR) is complete, including all component descriptions, interconnections, and simulation directives.
- **Set Simulation Parameters**: Double-check the simulation profile, including the analysis type (e.g., .TRAN, .DC, .AC) and the simulation duration.
- **Run the Simulation**:

- Click on **Simulation** in the menu.
- Select **Run** to start the simulation process.

- **Monitor Progress**: During the execution, you can observe the progress in the simulation window. Any errors will be reported here, allowing you to troubleshoot if necessary.

II.3 Editing and Analyzing Results

- **View Results**: After the simulation completes, results can be accessed via the output files (e.g., .OUT, .DAT). You can use the PROBE tool to visualize waveforms and analyze the data.
- **Interpret Results**: Analyze the output to understand the circuit's behavior under the specified conditions. Look for key parameters such as voltage levels, current flows, and frequency response

After the simulation, PSPICE generates a .OUT file containing the simulation results (input and output states over time, or output states in relation to inputs) in the form of a table of values and curves. The PROBE display module is activated using the command **.PROBE**.

To choose the signal to visualize, follow these steps:

1. Go to the menu and select **Trace -> Add...**.
2. A window will appear displaying the available signal names.
3. Click on the signal(s) you wish to display.

When the simulation is launched, the PSPICE window displays the variable on the x-axis corresponding to the specified analysis (e.g., Time for transient analysis). The command **Trace/Add Trace** allows access to a menu presenting all viewable signals.

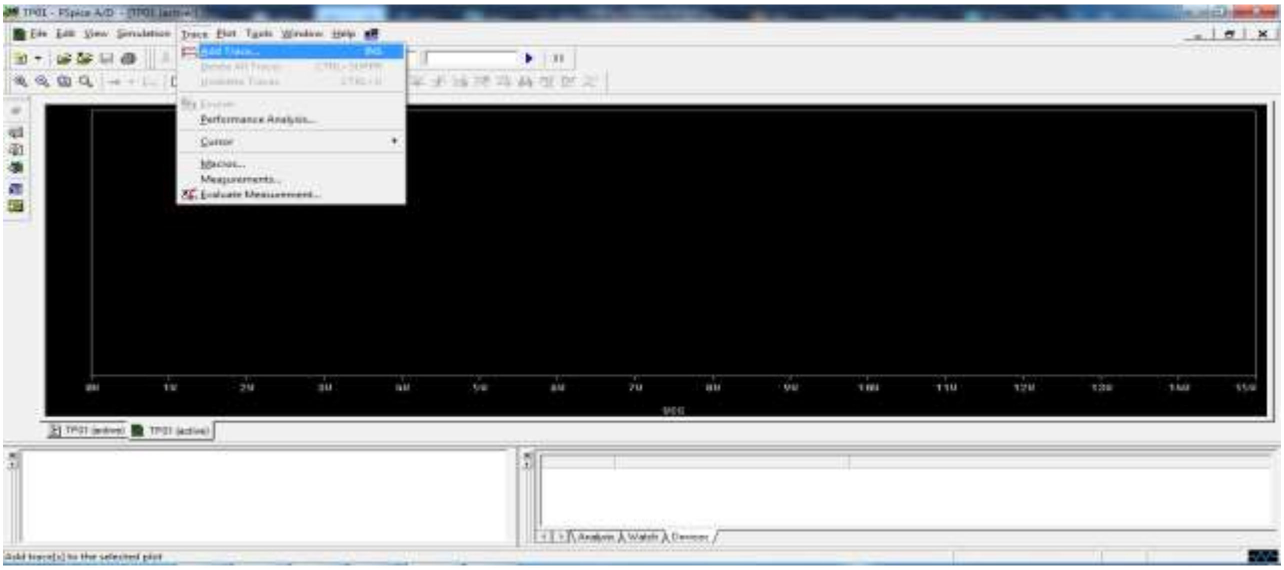
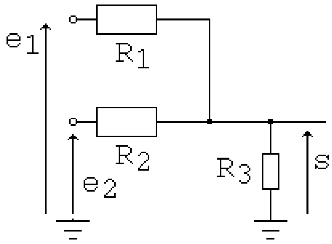


Figure.3 : Display Module on Screen

III. Simulation

III. 1. Example of Using .OP (Operating Point) in PSPICE

Consider the schematic below:



Given R1 = 3,3 kΩ ; R2 = 6,8 kΩ ; R3 = 4,7 kΩ.

1- **Apply** the superposition theorem to **determine** the DC potential at S when e1=1 V and e2=2V (theoretical)."

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1. **Write** the description

of this circuit in PSPICE language.

2. **Choose** the **.OP** directive for this analysis.

3. **Use** the output file (.**OUT**) to **determine** the DC potential at S and the **DC** currents supplied by each source."

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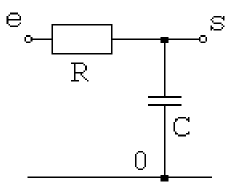
III. 2. An example of using .AC (small-signal dynamic analysis)

Consider the schematic below:



R = 3,3 kΩ ; C = 10 nf

We want to determine the harmonic response of H(j ω) = s(j ω) / e(jω, as well as the type and order of this filter.

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a) **Theoretical Study:**

1. **Establish** the transfer function of this filter.
2. What is the type and order of this filter?
3. **Express** the cutoff frequency fc in terms of R and C. **Calculate** this frequency.

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b) Simulation :

1. **Write** the description of this circuit in PSPICE language.
2. **Use** the **.AC** directive to perform a frequency analysis of 1000 points, starting from 100 Hz up to 100 kHz.
3. **Plot and comment** on the Bode diagram (gain curve in dB).
4. **Verify** the cutoff frequency fc.

Prog 2

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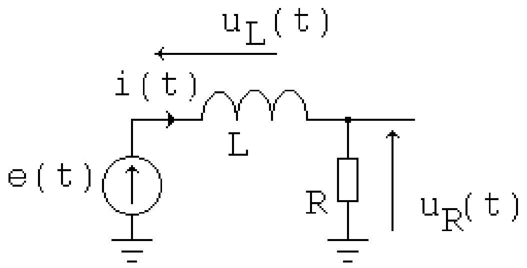
III. 3. An Example of Using .TRAN (Transient Analysis)



Consider the LR circuit shown here.
We want to determine the waveform $U_R(t)$ when e(t)is a step voltage with an amplitude of E0=3 V. Initial conditions are zero. R = 50 Ω, L = 1 mH.

a) Theoretical Study:

1. **Determine** the impulse response of this filter using the inverse Fourier transform of its transfer function (or the inverse Laplace transform).

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b) Simulation:

1. **Write** the description of this circuit in PSPICE language.
2. **Use** the **.TRAN** directive for this transient analysis.
3. **Plot and comment** on the impulse response of this circuit

Prog 3

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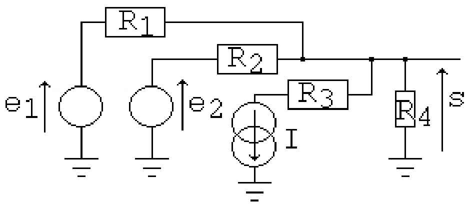
IV. Application to be done: Apply the same approach (theory, simulation, numerical interpretation) for the following setup:

Consider the schematic below :



We want to determine the DC potential at s when: e1 = 1 V, e2 = 2 V, I = 1 mA. Calculate, simulate, interpret.
Given : R1 = 3,3 kΩ ; R2 = 6,8 kΩ ; R3 = 4,7 kΩ ; R4 = 2,2 kΩ.

PW n°.2 : Simulation of Fundamental Circuits with Bipolar Junction Transistors (BJTs)

Conduct of the experiment.: ………. /……../…………. .

Hourly volume: 2^h.

Report made by:

Family name	First name	**Group**	**Final mark 20/20**
-	-	-	-
-	-	-	-
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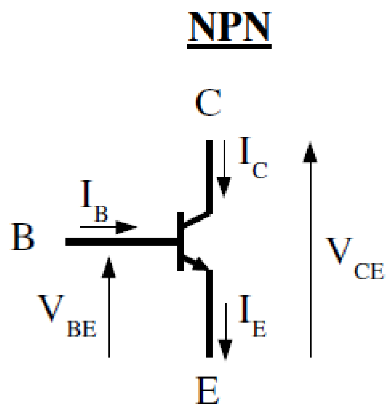
Goals:

- ✓ Study in Static Regime
- ✓ Plotting the characteristics of an NPN bipolar transistor and determining the operating point of a transistor circuit.
- ✓ Transient response of a follower circuit and an inverter circuit.

I. Theoretical Study:

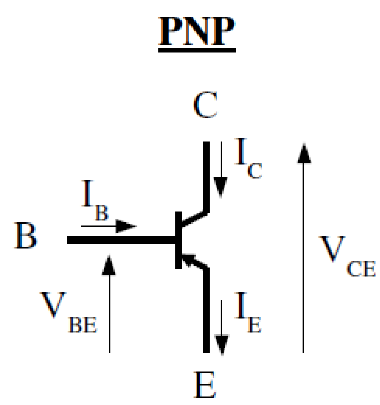
I.1. Bipolar Junction Transistor:

The bipolar transistor is a fundamental component of electronic systems. Its characteristics and various types of behavior make it suitable for many basic functions such as amplification and switching. A transistor consists of two back-to-back **PN** junctions: the base-emitter junction and the base-collector junction. There are two types of bipolar transistors: **NPN** and **PNP**. The typical transistors can be schematically represented as follows:



The emitter is indicated by the arrow, which symbolizes the actual direction of the current.

Positive values



Negative values

Figure.1 : Simple DC transistor converter

I.2. Modes of operation of the bipolar transistor:

a. Transistor in Switching Mode: The transistor can be in two different states		
Cut-off State	The transistor is considered as an **open switch.**	- *Ib= 0A => Ic = Ie = 0A* ; - *Vbe < Vbe0 = 0,6 V ou 0.7V* (threshold voltage).
Saturation State	The transistor is considered as a **closed switch** (if we consider... $Vce_{sat} = 0V$).	- $Ib > Ib_{sat} = Ic_{sat} / \beta$; - $Vce = Vce_{sat}$; - *β Ib>Ic> 0 et Ic* independent of *Ib*. - $Vbe_{sat} = Vbe0 = 0.6$ *à 0.7V* (Silicon) Vce_{sat} is on the order of *0.3 à 0.4V*. In practice, we take $Vce_{sat} = 0V$.
b. Transistor in Linear Mode:		
The transistor is considered as a current source Ic **controlled** by the base current Ib . - *Ib > 0A => Ic = β Ib* ; with $\beta = \frac{\alpha}{1-\alpha}$ et $\alpha = \frac{Ic}{Ie}$ - $Vce > Vce_{sat}$; - $Vbe_{sat} > Vbe >= Vbe0$; In practice, we take: *Vbe = Vbe0 = 0,6V à 0 .7V* (Silicon).		

I.3. Basic Configurations of Bipolar Transistors

With the transistor having three terminals, one of them will be common to both the input and the output. This results in three main configurations represented in the table below:

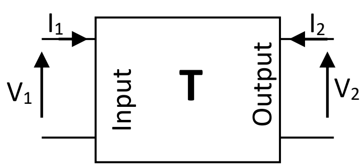
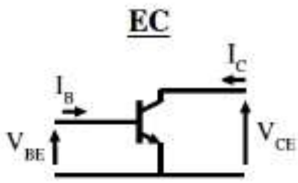
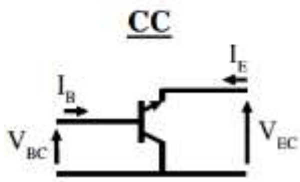
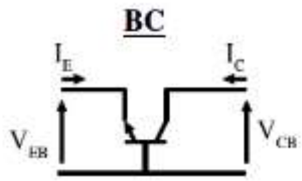


Figure. 2 : Quadripole Representation
of the Bipolar Transistor.

Configuration	Common Emitter 	Common Collector 	Common Base 
Input	Base	Base	Emitter
Output	Collector	Emitter	Collector

I.4. Electrical Characteristics of an NPN Transistor.

A transistor can be described by the quantities Ie, Ic, Ib, Vce, Vbe, and Vcb. . The operation of the transistor is summarized using its characteristic network: (for an NPN).

- The input characteristic.: Ib = f(Vbe)
- The transfer characteristic: Ic = f (Ib) with Vce constant.
- The output characteristic: *Vce = f (Ic)* with Ib constant.

The description of the transistor is made using these six quantities, whose dependence is graphically represented below.

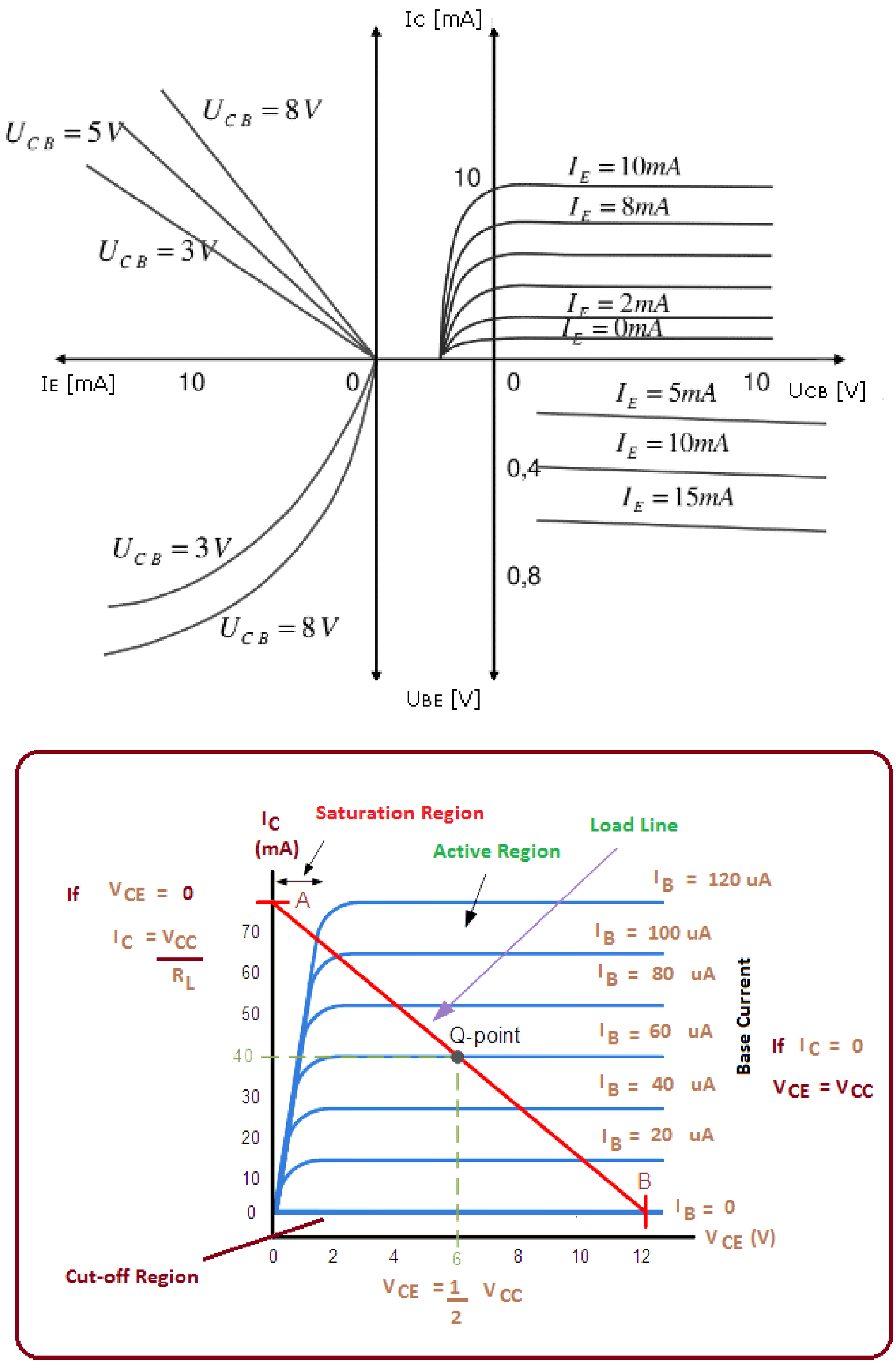


Figure. 3 : Characteristic Network of the NPN Bipolar Transistor.

I.5. Theoretical Preparation:

We take the biasing configuration from Figure 4 (common emitter configuration). We want to determine the quiescent point, for which we use a resistive divider bias and an emitter resistor. To do this, we need to know the four variables: specifically, the two currents *Ico* and *Ibo* and, on the other hand, the two voltages *Vceo* and *Vbeo*.

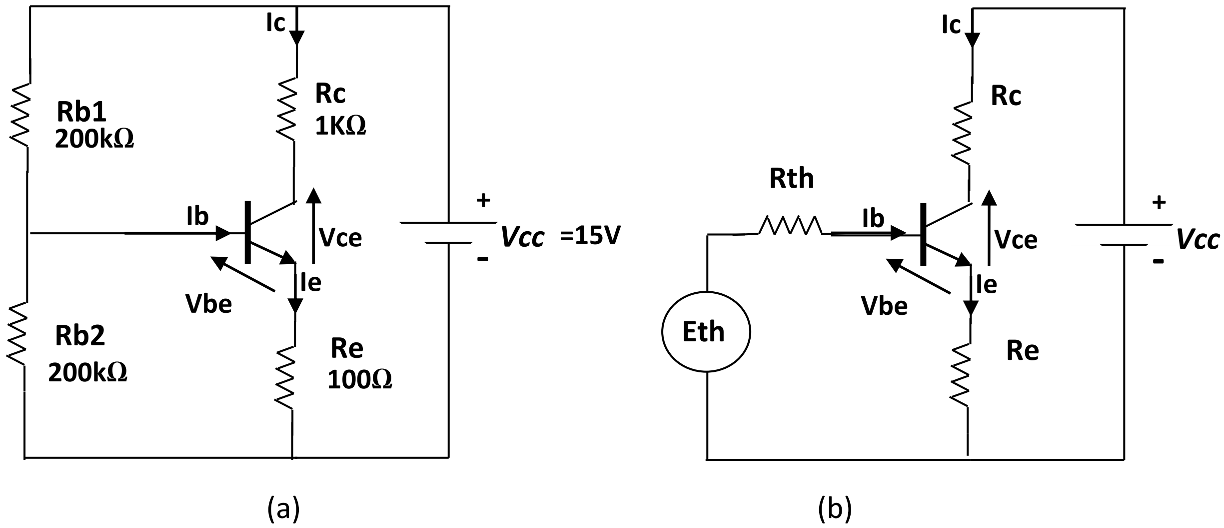


Figure.4 : Common Emitter Configuration (a) Biasing of an NPN transistor (Tr: 2N2222, β=100) using a resistive divider and emitter resistor.(b) Equivalent circuit diagram.

Using the Thévenin theorem applied to the voltage divider (consisting of Rb1, Rb2, and the DC supply voltage VCC

1- **Determine** the Thévenin resistance and the Thévenin equivalent voltage as seen by the base. (Rth and Eth)

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2- **Determine** the bias points *P(Ibo, Vbeo)* at the input (quiescent point) and *Q(Vceo, Ico)* at the output, respectively.

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3- **Plot** the static load line *Ic=f(Vce)* for the transistor circuit in Figure 4.

II. Simulation of the Bipolar Transistor with PSPICE

II. 1. Static Simulation

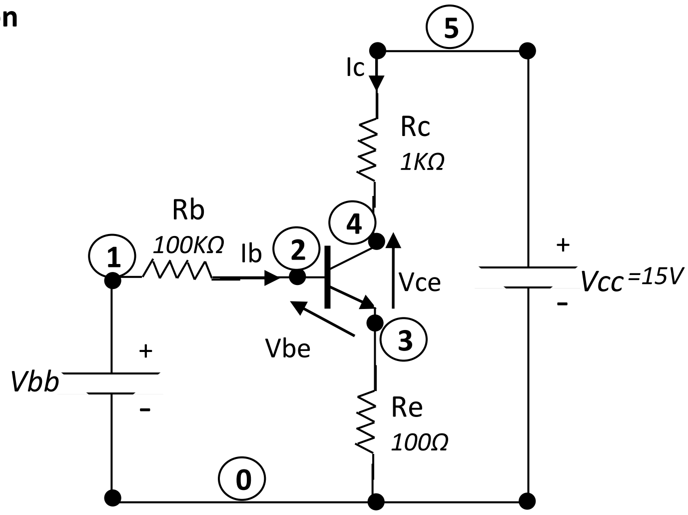

Figure.5 : Emitter Configuration.Biasing of an NPN Transistor (Tr: 2N2222, β=100) Using a Resistive Divider and Emitter Resistor

1- **Write** the circuit description for the Fig. 5 in the PSpice Netlist.

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a. **Plot** the characteristic Ic=f(Vce) for Vbb=1V by varying Vcc de 0 to 15V in increments of 0.1V using the DC analysis command **.DC**

Syntax :

.DC <nom de variable> <valeur de départ> <valeur de fin><incrément>

+ [spécification de balayage imbriqué]

b. On the same graph, **plot** the static load line Ic=f(Vce) with Rc=1kΩ and identify the operating point Q using the **.OP** command.

c. **Plot** the characteristic Ic=f(Vce) for Vbb=0 to 5Vin increments of 1V using the analysis command **.DC Vcc** ………. **Vbb**………….

d. **Plot** the characteristics Ic=f(Ib) and Vbe=f(Ib) for Ib=0 to 100µA in increments of 20µA ;

e. **Plot** Ic=f(Vce)) Ib=0 to 100µA in increments of 20µA; on the same graph, **plot** the static load line Ic=f(Vce. Then **complete** the following table:

Ib	0	20	40	60	80	100
Ic0						
Vce0						

PW n°.3 : Simulation of a Follower and Inverter Using Bipolar Technology

Conduct of the experiment.: ………. /……../…………. .

Hourly volume: 2^h.

Report made by:

Family name	First name	**Group**	**Final mark 20/20**
- - -	- - -	- - -	- - -

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Goal:

✓ Study the transient response of a follower circuit and an inverter circuit.

Overview

In this section, we will simulate a voltage follower (emitter follower) and an inverter (common emitter) using bipolar junction transistors (BJTs).

Application 1: Follower in Bipolar Technology

The circuit in Figure 1 corresponds to a follower in bipolar technology.

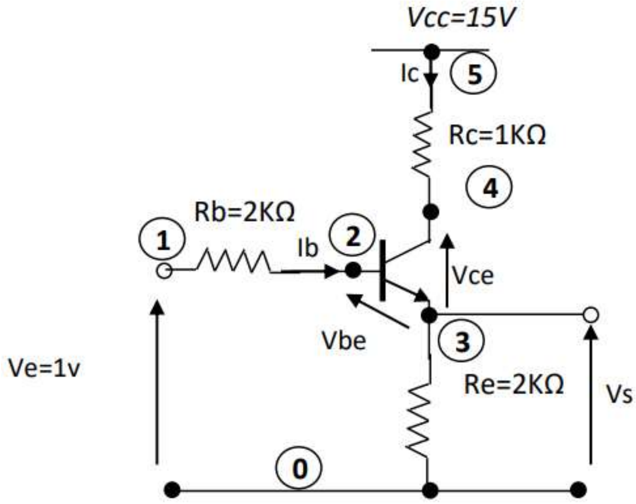

Figure.1 : follower in bipolar technology

1- **Plot** the transfer characteristic Vs=f(Ve) for RE=RB=2kΩR, varying Ve from -20 to 20V in increments of 0.1V using the **.DC Ve …….** command

2- **Comment** on the curve and highlight the sections corresponding to the cut-off, linear, and saturation regions by determining the input voltage ranges for these three different regions.

……

……

……

1- **Apply** a sinusoidal signal Ve with a peak-to-peak amplitude of 10V, a frequency of 1kHz, and a DC component of 5.5V (the Vbb generator will be removed from the circuit), then simulate the circuit in Figure 3 using the command **.tran 10u 5m 0 1u**.

Syntax :

.TRAN<intervalle d'édition> <temps final> [<délai avant édition>
+ [increment maximal]]

3- **Perform** a transient simulation to plot the input signal Ve and the output signal Vs as a function of time.

Application 2: Inverter in Bipolar Technology

The circuit in Figure 2 corresponds to an inverter in bipolar technology.

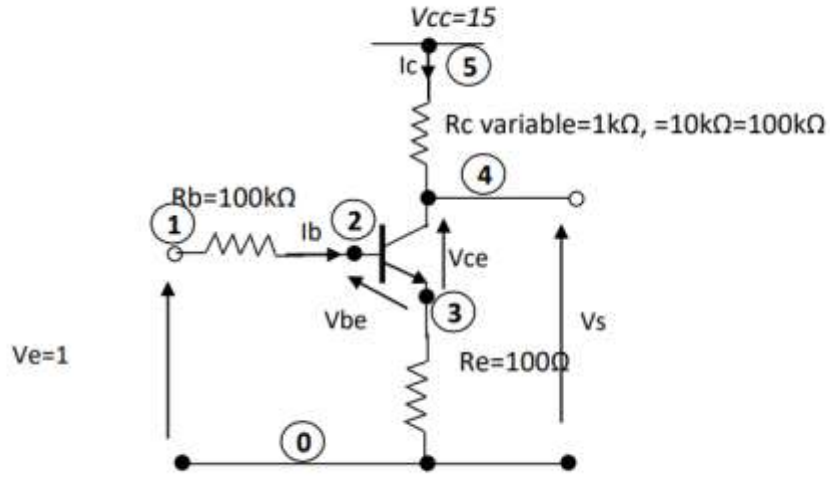

Figure.2 : Inverter in bipolar technology

1- **Plot** the transfer characteristic Vs=f(Ve) for Rc=1kΩ, 10kΩ et 100kΩ, varying Ve from 0 to 5V in increments of 0.1V using the **.DC Ve**...... command To change the value of Rc , use the **.param Rc=1k** .command.

2- **Comment** on the curve and highlight the sections corresponding to the cut-off, linear, and saturation regions.

……

……

……

3- **Apply** a square wave signal Ve with a peak-to-peak amplitude of 5V and a period of 200µs (the Vbb generator will be removed from the circuit), then simulate the circuit in Figure 3 using the **.tran 10u 5m 0 1u** command.

4- **Perform** a transient simulation to plot the input signal Ve and the output signal Vs as a function of time.

III. Application to be done: **Apply** the same approach (theory, simulation, graphical interpretation, and numerical analysis) for the following circuits: **Current mirror**, **Darlington pair**.

PW n°.4 : Simulation and Analysis of Class A Amplifier using SPICE

Conduct of the experiment.: ………. /……../………….. .
Hourly volume: 2^{h}.

Report made by:

Family name	First name	**Group**	**Final mark 20/20**
- - -	- - -	- - -	- - -

Instructions:

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   - **Names and surnames of the lab participants.**
   - **The report must include an introduction, specify the purpose of the simulations, present the results with interpretation, and conclude with a summary.**
   - **Preparation and work should be handwritten.**

Goal:

- ✓ Understand the operating principles of Class A amplifiers
- ✓ Master SPICE simulation techniques for analog circuits
- ✓ Analyze DC operating point and bias stability
- ✓ Characterize AC performance (gain, bandwidth, impedance)
- ✓ Evaluate power efficiency and distortion
- ✓ Study thermal effects on amplifier performance

I.Theoretical Background

I.1. Class A Amplifier Characteristics

Circuit 1: Basic Common-Emitter Class A Amplifier

- High linearity, low distortion
- Low efficiency (theoretical maximum: 25% for resistive load, 50% for inductive load)
- Simple implementation

I.2. Key Performance Parameters

- Voltage Gain: $Av = -g_m \times R_c$
- Input Impedance: $Zin = R_1 \parallel R_2 \parallel (\beta \times r_e)$
- Output Impedance: $Zout = R_c$
- Power Efficiency: $\eta = \frac{Pout}{PDC} \times 100\%$

II. Experimental Setup

II.2 Circuit 1: Basic Common-Emitter Class A Amplifier

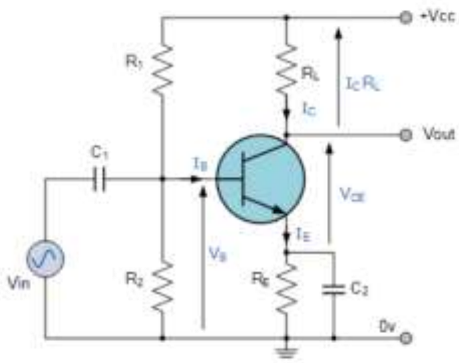

Figure.1 : Simple DC transistor converter

```
* Practical Work - Class A Amplifier
* Master Microelectronics - Circuit 1
* Basic Common-Emitter Configuration

* Power Supplies
VCC 10 0 DC 12V
* Bias Network
R1 10 2 82K
R2 2 0 12K
RE 3 0 1.2K
RL 10 4 3.9K

* Bipolar Junction Transistor
Q1 4 2 3 Q2N2222

* Coupling Capacitors
C1 1 2 10uF
C2 3 0 10uF

* Analysis Commands
.OP
.TRAN 0.01ms 5ms
.AC DEC 50 10Hz 1MegHz

* Transistor Model
.MODEL Q2N2222 NPN(
+ IS=3.295E-14 NF=1 BF=200 VAF=100
+ IKF=0.52 ISE=7.734E-15 NE=1.259
+ BR=4 NR=1 VAR=18 IKR=0.24
+ RB=5 IRB=5E-6 RBM=1
+ RC=0.56 CJC=1.12E-11 VJC=0.76
+ MJC=0.5385 FC=0.8 CJE=2.01E-11
+ VJE=1.1 MJE=0.5 TR=5E-7 TF=5E-10
+ ITF=1.5 VTF=2 XTF=1.5)

* Output Control
.PRINT DC V(2) V(3) V(4) I(Q1)
.PRINT AC VM(5) VP(5)
.PLOT TRAN V(1) V(5)
.END
```

II.3 Circuit 2: Improved Class A with Current Mirror Bias

```
* Circuit 2: Enhanced Class A with Active Load
* Improved linearity and thermal stability

VCC 10 0 DC 15V
VEE 20 0 DC -15V

* Input Signal
VIN 1 0 SIN(0 0.1V 1kHz)

* Differential Pair Input Stage
Q1 3 2 4 Q2N2222
Q2 5 6 4 Q2N2222
```

```
RE1 4 20 2.7K

* Current Mirror Bias
Q3 3 3 10 Q2N2222
Q4 5 3 10 Q2N2222

* Current Source
Q5 4 7 20 Q2N2222
RBIAS 7 20 8.2K

* Output Stage (Class A)
Q6 8 5 10 Q2N2222
RC 8 10 4.7K
RL 8 0 16Ω

* Coupling Capacitors
C1 1 2 22uF
C2 8 9 100uF

* Analysis
.OP
.TRAN 0.01ms 3ms UIC
.AC DEC 50 1Hz 2MegHz
.TEMP 27 50 75
.FOUR 1kHz V(8)

.MODEL Q2N2222 NPN(IS=14.34F XTI=3 EG=1.11 VAF=74.03
+ BF=255.9 NE=1.5 ISE=14.34F IKF=0.2847 XTB=1.5
+ BR=6.092 NC=2 ISC=0 IKR=0 RC=1 CJC=7.306P
+ MJC=0.3416 VJC=0.75 FC=0.5 CJE=22.01P
+ MJE=0.377 VJE=0.75 TR=46.91N TF=411.1P
+ ITF=0.6 VTF=1.7 XTF=3 RB=10)

.PRINT TRAN V(8) V(1)
.PRINT AC VM(8) VP(8)
.END
```

II.4 Experimental Procedure

II.4.1 Simulate Circuit 1 with ***.OP*** analysis

- Record all node voltages and branch currents
- Verify transistor operates in active region
- Calculate DC power consumption: $P_{PC} = V_{CC} \times I_{CQ}$

II.4.2 Measure and calculate:

- Quiescent current I_{CQ}
- Collector-Emitter voltage V_{CEQ}
- Base-Emitter voltage V_{BEQ}

Part A: DC Analysis

1 . Simulate Circuit 1 with .OP analysis

- Record all node voltages and branch currents
- Verify transistor operates in active region
- Calculate DC power consumption: $P_{PC} = V_{CC} \times I_{CQ}$

2. Measure and calculate:

- Quiescent current I_{CQ}
- Collector-Emitter voltage V_{CEQ}
- Base-Emitter voltage V_{BEQ}

Part B: AC Analysis

1 . Transient Analysis

- Apply 1kHz sine wave input (amplitude: 10mV)
- Measure output voltage swing

- Calculate voltage gain: $Av = \frac{Vout}{Vin}$

2. Frequency Response
   - Run AC analysis from 10Hz to 1MHz
   - Determine:
     - Low-frequency cutoff (f_L)
     - High-frequency cutoff (f_H)
     - Bandwidth: $BW = f_H - f_L$
     - Gain-bandwidth product (GBW)

Part C: Performance Characterization

1. Input/Output Impedance
   - Use "test voltage source" method
   - Calculate: $Zin = \frac{V_{test}}{I_{test}}$

2. Power Efficiency
   - Calculate output power: $Pout = \frac{Vout}{r_{ms2Rl}}$
   - Calculate efficiency: $\eta = \frac{Pout}{PDC} \times 100\%$

3. Distortion Analysis
   - Use Fourier analysis (***.FOUR***)
   - Measure Total Harmonic Distortion (***THD***)

Part D: Thermal Analysis

1. Temperature Sweep

- Simulate at 27°C, 50°C, 75°C
- Analyze bias point stability
- Calculate thermal drift coefficients

III. Results and Analysis

Table 1: DC Operating Point (Circuit 1)

Parameter	Simulated Value	Theoretical Value	Error %
V_B (V)			
V_E (V)			
VC (V)			
I_C (mA)			
V_{CE} (V)			

Table 2: AC Performance (Circuit 1)

Parameter	Value
Voltage Gain (dB)	
-3dB Bandwidth (Hz)	
Input Impedance (Ω)	
Output Impedance (Ω)	
Output Swing (Vpp)	

Table 3: Power Analysis

Parameter	Circuit 1	Circuit 2
PDC(mW)		
Pout,max (mW)		
Efficiency η (%)		
THD @ 1kHz (%)		

Table 4: Thermal Analysis

Temperature	ICIC (mA)	VCEVCE (V)	Gain (dB)
27°C			
50°C			
75°C			

1) Complete all measurement tables
2) Plot the curves:

   - Waveforms: Input/Output signals
   - Frequency response plots (Bode)
   - Power dissipation graphs

3) Explain the relationship between bias point and output swing
4) Compare measured efficiency with theoretical maximum
5) Analyze the effect of load resistance on performance
6) Discuss thermal stability and improvement methods
7) Compare simple and improved Class A configurations

PW n°.5 : Simulation of Amplifiers with Different Input Sources

Conduct of the experiment.: ………. /……../………….. .
Hourly volume: 2^h.

Report made by:

Family name	First name	**Group**	**Final mark 20/20**
- - -	- - -	- - -	- - -

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Goal:

This practical work investigates the critical interface between an amplifier and its input source. Students will learn that an amplifier's performance is not intrinsic but depends heavily on the characteristics of the source driving it.

Learning Outcomes:

- ✓ Simulate single-stage amplifiers (Common-Source, Common-Emitter) from a netlist perspective.
- ✓ Quantify the performance degradation caused by a high-impedance source.
- ✓ Differentiate between intrinsic voltage gain and overall system gain.
- ✓ Measure input/output impedance using SPICE techniques.
- ✓ Propose and verify a solution to the high-impedance source problem.

I.Theoretical Background

I.1 Amplifier Topologies under Test:

- **Circuit A: Common-Source (CS) Amplifier:** High input impedance (theoretically infinite), high output impedance, high voltage gain.
- **Circuit B: Common-Emitter (CE) Amplifier:** High input impedance (moderate), high output impedance, high voltage gain.

I.2. Input Source Models:

- **Ideal Voltage Source (V1):** RS = 0. Represents a perfect signal generator.
- **Non-Ideal Source (V2):** RS = 100k. Represents a real-world sensor (e.g., piezoelectric, microphone).

I.3. Key Concept: Input Impedance & Loading Effect :

The voltage at the amplifier's gate/base, Vin, is determined by the voltage divider between the source resistance R_{Sand} the amplifier's input impedance Z_{in}:

$$Vin = Vs \times \frac{Zin}{Rs + Zin}$$

If Z_{in} is not much greater than R_S, the signal is attenuated *before* being amplified. The **Overall Gain** (V_{out}/V_s) can be drastically lower than the amplifier's **Intrinsic Gain** (V_{out}/V_{in}).

II. SPICE Models and Setup

We will use generic but realistic models for the MOSFET and BJT.

```spice
* SPICE Model Definitions
.model NMOS_MOD nmos (level=1 VTO=0.7 KP=100e-6 LAMBDA=0.05)
.model PMOS_MOD pmos (level=1 VTO=-0.7 KP=50e-6 LAMBDA=0.05)
.model NPN_MOD npn (IS=1e-16 BF=100 VAF=50)
```

III. Practical Work Procedure

III.1. Common-Source Amplifier with Ideal Source

Schematic and Netlist:

```
spice

* Part 1: Common-Source Amplifier with Ideal Source (RS = 0)
VDD VDD 0 DC 2.5V
VSS VSS 0 DC -2.5V
Vbias Vbias 0 DC 0.8V     ; Bias for the current source
Vin Vin 0 DC 0 AC 1       ; Ideal AC source: RS = 0

* Current Mirror Bias
Mref Vbias Vbias VDD VDD PMOS_MOD W=20u L=1u
Mbias Vout_cs_bias Vbias VDD VDD PMOS_MOD W=20u L=1u
```

```
* Common-Source Stage
M1 Vout_cs Vin Vss Vss NMOS_MOD W=10u L=1u
M2 Vout_cs Vbias VDD VDD PMOS_MOD W=20u L=1u

* Analysis
.op
.ac dec 10 1 1G
.tran 0 2ms 0 1us

* Measure Intrinsic Gain (Vout/Vin) and BW
.measure ac gain_max max VDB(Vout_cs)
.measure ac bw when VDB(Vout_cs)=gain_max-3
.end
```

Tasks and Measurements:

1) Run an **.OP** analysis to verify M1 and M2 are in saturation (VDS > VGS - VTO).
2) Run an **.AC** analysis. Plot VDB(Vout_cs).
3) **Measure:**
   - **Low-Freq Intrinsic Gain (A_V_CS):** V_{out_cs}/V_{in} at 1kHz.
   - **-3dB Bandwidth (BW_CS):** Frequency where gain drops by 3dB.

III.2. CS Amplifier with Non-Ideal Source

Schematic and Netlist:

```spice
spice

* Part 2: Common-Source Amplifier with Non-Ideal Source (RS = 100k)
VDD VDD 0 DC 2.5V
VSS VSS 0 DC -2.5V
Vbias Vbias 0 DC 0.8V
Vs Sensor_In 0 DC 0 AC 1   ; Sensor voltage source
RS Sensor_In Vin 100k      ; High Source Impedance

* ... (Rest of the circuit from Part 1: M1, M2, etc.) ...

* Analysis
.op
.ac dec 10 1 1G
.tran 0 2ms 0 1us
```

```
* Measure Overall Gain (Vout/Vs) and Intrinsic Gain (Vout/Vin)
.measure ac overall_gain_max max VDB(Vout_cs)
.measure ac intrinsic_gain param='Vout_cs/Vin' at 1k
.measure ac bw_overall when VDB(Vout_cs)=overall_gain_max-3
.end
```

Tasks and Measurements:

1) Run **.AC** and **.TRAN** analyses.
2) In transient, apply a sine wave: **Vs Sensor_In 0 SIN(0 0.01 1k).**
3) **Measure:**

- **Overall Gain (G_V_CS):** V_{out_cs}/V_s at 1kHz. Compare it to A_V_CS from Part 1.
- **Bandwidth (BW_CS_NonIdeal).**
- In transient, observe the attenuation between $V_{(Sensor\_In)}$ and V(Vin).

III.3. Input Impedance Measurement

Netlist Addition:

```spice
* Part 3: Input Impedance Measurement for CS Stage
* Use the non-ideal source circuit from Part 2
I_test Vin 0 AC 1          ; Inject a 1A AC test current
*V_test Vin 0 AC 1         ; Alternatively, apply a 1V AC test voltage

.ac dec 10 1 100MEG
.plot ac Zin=V(Vin)/I(I_test)  ; Zin in ohms
*.plot ac Zin=1/I(V_test)   ; If using the voltage source method

.measure ac Zin_low param='V(Vin)/I(I_test)' at 1k
.end
```

Tasks:

1) Plot the input impedance Zin vs. frequency.
2) Measure the low-frequency input impedance. Is it very high as expected?
3) Explain how the Zin value interacts with RS=100k to cause the signal attenuation observed in Part 2 (III.2).

III.4. Common-Emitter Amplifier (Comparative Study)

Netlist:

```spice
* Part 4: Common-Emitter Amplifier
VCC VCC 0 DC 5V
Vs_Sig Sig_In 0 DC 0 AC 1
RS_Sig Sig_In Vbase 100k   ; Non-ideal source

Q1 Vce Vbase Vemitter NPN_MOD
Rc VCC Vce 5k              ; Collector Load
Re Vemitter 0 1k           ; Emitter Degeneration for stability

* DC Bias: Set collector current to ~1mA
Vbias_base Vbase 0 DC 0.78V ; Approx value to bias Q1

.op
.ac dec 10 1 100MEG
.tran 0 2ms 0 1us
```

```spice
.measure ac gain_ce max VDB(Vce)
.measure ac bw_ce when VDB(Vce)=gain_ce-3
.end
```

Tasks:

1) Run **.OP** to find the collector current Ic(Q1) and verify VCE > 0.2V.
2) Run **.AC** analysis for both RS=0 and RS=100k.
3) **Compare** the performance (Gain, Bandwidth, and impact of RS) of the CE stage with the CS stage.

III.5. Solution - The Source Follower (Buffer)

Netlist:

```
spice

* Part 5: Solution - Source Follower Buffer
VDD VDD 0 DC 2.5V
VSS VSS 0 DC -2.5V
Vs Sensor_In 0 DC 0 AC 1
RS Sensor_In Vin_old 100k  ; High impedance source

*--- NEW SOURCE FOLLOWER STAGE ---*
M_sf Vin_new Vin_old VSS VSS NMOS_MOD W=10u L=1u
I_bias Vin_new VSS 50u     ; Current source bias

*--- ORIGINAL CS STAGE ---*
M1 Vout_cs_buffered Vin_new VSS VSS NMOS_MOD W=10u L=1u
M2 Vout_cs_buffered Vbias VDD VDD PMOS_MOD W=20u L=1u
Vbias Vbias 0 DC 0.8V
```

```
.ac dec 10 1 1G
.tran 0 2ms 0 1us

.measure ac overall_gain_buffered max VDB(Vout_cs_buffered)
.end
```

Tasks:

1. Simulate the new circuit.
2. **Measure** the **Overall Gain** (Vout_cs_buffered/Vs). Compare it to the gain from Part 2.
3. Explain the role of the Source Follower: it provides a **high input impedance** (not loading the sensor) and a **low output impedance** (ideally driving the CS stage).

IV. Results and Analysis

1) Complete the following table

Table 1: Summarize all measured parameters (Gains, Bandwidth, Zin) for all circuits and conditions.

Circuit	Condition	Intrinsic Gain (dB)	Overall Gain (dB)	BW (MHz)	Zin (kΩ)
CS Amp	RS = 0 Ω				
CS Amp	RS = 100 kΩ				
CE Amp	RS = 0 Ω				
CE Amp	RS = 100 kΩ				
CS Amp + Buffer	RS = 100 kΩ				

2) Analyze the "loading effect" quantitatively. Does the measured overall gain match the calculation G_V = A_V * (Zin/(RS+Zin))?
3) Why did the bandwidth change in some cases? (Hint: think about the Miller effect and the new RC time constant formed by RS and the amplifier's input capacitance).
4) Compare CS and CE performance trade-offs.
5) Explain how the source follower solved the problem. What is the trade-off in using a buffer? (e.g., voltage headroom, noise).
6) To conclude, summarize the critical importance of impedance matching in analog design.

PW n°.6 : Design and Simulation of a NAND Gate in Emitter-Coupled Logic (ECL) Technology

Conduct of the experiment.: ………. /……../………….. .
Hourly volume: 2^h.

Report made by:

Family name	First name	**Group**	**Final mark 20/20**
- - -	- - -	- - -	- - -

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Goal:

This practical work introduces the student to the design and analysis of Emitter-Coupled Logic (ECL), a high-speed, current-steering logic family. Unlike CMOS, ECL operates transistors in the forward-active region to avoid slow saturation, enabling very high-speed operation.

- ✓ Understand the principle of operation of ECL gates.
- ✓ Design and simulate a basic 2-input ECL NAND gate.
- ✓ Perform DC, transient, and power analysis on the ECL gate.
- ✓ Characterize key performance metrics: propagation delay, noise margins, and power-delay product (PDP).
- ✓ Compare the performance trade-offs between ECL and CMOS technologies.

I.Theoretical Background

I.1. ECL Core Principles:

- **Differential Pair:** The heart of an ECL gate is a differential amplifier (emitter-coupled pair) that steers a constant current between two paths based on the input voltage.
- **Non-Saturating Operation:** Transistors are prevented from entering saturation, eliminating the storage delay time and enabling high-speed switching.
- **Voltage Referencing:** A precise reference voltage (V_{BB}) is used for decision making, typically set at the midpoint of the logic swing.
- **Emitter Followers:** Used at the outputs for low-output impedance, providing high fan-out capability and level shifting.

I.2. ECL NAND Gate Operation: For a 2-input OR/NOR gate, the inputs are applied to parallel transistors. A NAND function is achieved by applying the inputs to series transistors in the differential pair, or more commonly, by using the NOR output and applying De Morgan's theorem (NAND = NOT(OR)) by taking the inverting output.

This TP will simulate a true series-gated ECL NAND topology.

I.3. Logic Levels: A typical ECL logic swing is around 800mV (e.g., Logic '1' = -0.9V, Logic '0' = -1.7V), centered around a V_{BB} of -1.3V.

II. SPICE Models and Setup

We will use high-frequency NPN BJT models.

```spice
* ECL NAND GATE PRACTICAL WORK
* SPICE Model Definitions
.model NPN_HF npn (
+ IS=1.0E-16     BF=100    NF=1.0    VAF=50
+ IKF=0.01       ISE=1.0E-15  NE=1.5    BR=1
+ NR=1.0         VAR=10    IKR=0.01  ISC=1.0E-13
+ NC=2.0         RB=10      RBM=1     IRB=0.1
+ RC=5           RE=1       CJE=0.5P  VJE=0.7
+ MJE=0.33       CJC=0.3P  VJC=0.55  MJC=0.3
+ TF=10P         TR=30P     XTF=10    VTF=10
+ ITF=1)
```

```
* Power Supplies
VEE VEE 0 DC -5.2V
VCS VCS 0 DC -4V   ; Current Source Bias
VBB VBB 0 DC -1.3V ; Reference Voltage
.temp 27
.options TNOM=27
```

III. Practical Work Procedure

III.1. DC Analysis - Transfer Characteristic and Noise Margins

Netlist:

```spice
* Part 1: DC Analysis - ECL NAND Gate
VEE VEE 0 DC -5.2V
VCS VCS 0 DC -4V
VBB VBB 0 DC -1.3V

* Input A is swept, Input B is held at VHIGH (Logic 1)
VA A 0 DC -0.9V
VB B 0 DC -0.9V

* Current Source
Qcs Vtail VCS VEE NPN_HF  ; Diode-connected for bias
```

```
* Series-Gated Differential Pair for NAND
Q1 X1 A Vtail NPN_HF      ; Input A Transistor
Q2 Vnor B X1 NPN_HF       ; Input B Transistor (Series with Q1)
Q3 Vor VBB Vtail NPN_HF   ; Reference Transistor

* Load Resistors
Rc_nor VCC Vnor 220
Rc_or VCC Vor 220

* Emitter Followers for Output Buffering
Q4 NOR Vnor VCC NPN_HF    ; NOR Output Follower
```

```
Q5 OR Vor VCC NPN_HF      ; OR Output Follower

* Output Pull-Down Resistors
Re_nor NOR VEE 1.5k
Re_or OR VEE 1.5k

* Virtual VCC
VCC VCC 0 DC 0V

* Analysis: Sweep input A from HIGH to LOW
.dc VA -0.9 -1.7 0.01
*.dc VB -0.9 -1.7 0.01 ; Uncomment for second input
```

```
.plot dc V(NOR) V(OR)
.measure dc VOH_NOR FIND V(NOR) WHEN V(A)=-0.9
.measure dc VOL_NOR FIND V(NOR) WHEN V(A)=-1.7
.measure dc VIL_NOR WHEN deriv(V(NOR))=-1 cross=1
.measure dc VIH_NOR WHEN deriv(V(NOR))=-1 cross=2
.end
```

Tasks and Measurements:

1) Run the **.DC** analysis.
2) Plot the transfer characteristics V(NOR) vs. V(A) and V(OR) vs. V(A).
3) **Measure:**

- **Output High Level (V_{OH})** and **Output Low Level (V_{OL})** for the NOR output.
- **Input Low Voltage (V_{IL})** and **Input High Voltage (V_{IH})** from the points where the slope (derivative) equals -1.
- **Noise Margins:** NMH = V_{OH} - V_{IH} and NML = V_{IL} - V_{OL}.

III.2. Transient Analysis - Propagation Delay

Netlist:

```
spice

* Part 2: Transient Analysis - Propagation Delay
VEE VEE 0 DC -5.2V
VCS VCS 0 DC -4V
VBB VBB 0 DC -1.3V

* PULSE Syntax: PULSE(Vlow Vhigh Tdelay Trise Tfall Pulsewidth Period)
VA A 0 PULSE(-1.7 -0.9 1ns 20p 20p 10ns 20ns) ; Input A
VB B 0 DC -0.9V ; Input B held high

* ... (Insert the same transistor and resistor netlist from Part 1 here) ...
```

```
* Load Capacitance
Cload_nor NOR 0 50fF
Cload_or OR 0 50fF

.tran 0.1ns 40ns

* Measure Propagation Delays
.measure tplh_nor TRIG V(A) VAL='(VIH_NOR+VIL_NOR)/2' RISE=1
+                 TARG V(NOR) VAL='(VOH_NOR+VOL_NOR)/2' FALL=1
.measure tphl_nor TRIG V(A) VAL='(VIH_NOR+VIL_NOR)/2' FALL=1
+                 TARG V(NOR) VAL='(VOH_NOR+VOL_NOR)/2' RISE=1
.measure tpd_nor param='(tplh_nor+tphl_nor)/2'

.measure tplh_or TRIG V(A) VAL='(VIH_NOR+VIL_NOR)/2' RISE=1
```

```
+                 TARG V(OR) VAL='(VOH_OR+VOL_OR)/2' FALL=1
.measure tpd_or param='(tplh_or+tphl_or)/2'
.end
```

Tasks and Measurements:

1) Run the **.TRAN** analysis.
2) Plot the inputs V(A), V(B) and outputs V(NOR), V(OR).
3) Verify the logic function: The NOR output should be low only when both A AND B are high.
4) **Measure:**

   - **Propagation Delays (t_{PLH}, t_{PHL})** for both NOR and OR outputs.

- **Average Propagation Delay (t_{pd}).**

III.3. Power Consumption Analysis

Netlist:

```spice
* Part 3: Power Consumption Analysis
* Use the same netlist as Part 2 for transient analysis

* Measure average current from VEE supply
.measure pwr_avg AVG I(VEE) FROM 15ns TO 35ns
.measure pwr_dc param='-pwr_avg*5.2' ; P = V*I (I is negative from SPICE)

* Measure Power-Delay Product (PDP)
.measure PDP_nor param='pwr_dc*tpd_nor'
.end
```

Tasks and Measurements::

1) Run the **.TRAN** analysis from Part 2 with the added .measure statements.
2) **Measure:**

- **Average Power Consumption (P_{avg})** from the VEE supply.
- **Power-Delay Product (PDP)** for the NOR output.

III.4. Fan-out Study

Netlist:

```spice
* Add identical load gates
Xload1 NOR OR VCC VEE VBB VCS NAND_ECL
Xload2 NOR OR VCC VEE VBB VCS NAND_ECL
Xload3 NOR OR VCC VEE VBB VCS NAND_ECL

* Subcircuit Definition (enclose the main circuit here)
.subckt NAND_ECL NOR_OUT OR_OUT VCC VEE VBB VCS
* ... (Paste the entire transistor/resistor netlist from Part 1 here) ...
* Remember to change the top-level node names to the subcircuit pins
.ends NAND_ECL
```

```
.tran 0.1ns 40ns
* Re-measure tpd_nor with 3 fan-out gates
.measure tpd_nor_fanout param='(tplh_nor+tphl_nor)/2'
.end
```

Tasks:

1) Run the **.TRAN** analysis with 3 fan-out gates.
2) **Measure** the new **Average Propagation Delay (t_{pd_nor_fanout})**.
3) Compare it with the unloaded delay from Part 2 (III.2). Explain the change (due to the increased capacitive load on the emitter followers).

IV. Results and Analysis

1) Complete the following table
2) Plot the DC transfer characteristics for both NOR and OR outputs.
3) Plot the transient response showing the NAND/NOR operation and propagation delay.

Table 1

Parameter	Symbol	Simulated Value
Output High Voltage (NOR)	V_{OH}	
Output Low Voltage (NOR)	V_{OL}	
Noise Margin High	NM_H	
Noise Margin Low	NM_L	
Avg. Prop. Delay (NOR, no load)	t_{pd_nor}	
Avg. Prop. Delay (NOR, FO=3)	t_{pd_nor_fanout}	
Avg. Power Consumption	P_{avg}	
Power-Delay Product	PDP	

4) Analyze the shape of the transfer characteristic. Why is it not a perfect step function?
5) Comment on the measured noise margins. Are they sufficient for a robust logic family?
6) Discuss the speed-power trade-off. ECL is fast but power-hungry. Explain why the power consumption is relatively constant, unlike CMOS.
7) Explain the effect of fan-out on performance. Why does the delay increase?
8) Compare ECL with CMOS technology. List 3 advantages and 3 disadvantages of ECL.
9) To conclude, summarize the key characteristics of the simulated ECL NAND gate and the principles of ECL design you have learned.