University Mohamed Boudiaf of M'sila

FACULTY OF TECHNOLOGY

ELECTRICAL ENGINEERING DEPARTMENT

Serial number: ……...

Registration number: ……

Thesis

Presented for obtaining the diploma of:

MASTER

Specialty: Commande Electrique

THEME:

Control of parallel voltage source inverters, circulating current elimination and output power quality improvement

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June 2025

Acknowledgements

في البداية نشكر الله عز وجل الذي بفضله وتوفيقه تمكنا من انجاز هذه المذكرة.

We can only extend our thanks, gratitude and appreciation to our supervisor Professor CHBABAHI Ali, who helped us greatly through his invaluable support and guidance throughout this work, and by providing us with valuable comments and suggestions during the development of this work.

We extend our thanks to the members of the examination body for agreeing to read, evaluate, and comment on this thesis.

We would like to extend special thanks to our families as a whole for their continued support, assistance and understanding when conducting our research and writing our thesis.

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General Introduction

Three-phase three-leg pulse width modulation (PWM) converters have been widely used in many industrial energy applications, such as renewable power generation-based grid-connected energy distribution systems or stand-alone power-supply systems (SAPSSs) [1]. A high-efficiency device is also considered for such power systems due to its lower current THDs, superior current quality waveforms, and bidirectional power flow [2]. However, in high-energy applications, such as distributed energy generation systems and EV charging stations, single three phase PWM inverter cannot meet certain requirements, such as reliability, power capability, and modularity. To address these limitations, parallel PWM inverter configurations have become common in these types of applications due to their ability to increase system capacity, reduce the thermal stress and current rating limitations of power switches, and increase system stability and reliability [11, 12]. Unfortunately, a circulating current (CC) flow path can be formed in this configuration due to the difference between the zero-sequence voltages (ZSVs) of the parallel inverters, which is generally attributed to mismatches in the inverter filter inductances, unbalanced output current sharing, or unequal switching frequency [13, 14]. The CC is decomposed into high-frequency harmonic components (CC-HFHCs) and low-FHCs (CC LFHCs). CC-LFHCs increase inverter output current distortions due to the presence of LFHCs, especially the third harmonic and its multiples, causing the inverter filter inductances to exhibit abnormal noise and vibrations [15]. In addition, LFHCs increase the output voltage distortions and losses, decrease the system efficiency and reliability, increase electromagnetic interference (EMI), and increase the current stress of power switches [16]. To eliminate CC, several solutions have been proposed in the literature. An inter phase reactor-based varying impedance method was proposed in [17], which accurately reduced the CC-HFHCs in parallel converters to a suitable level; however, this method was unable to suppress the CC-LFHCs and required high cost and necessarily additional hardware circuits. Other efforts have proposed a series of special PWM techniques. In [18] and [19], a simple harmonic-elimination PWM (HEPWM) method was proposed for CC reduction in parallel PWM inverters by reducing the magnitude of the triple harmonic components. In [20] and [21], a carrier phase shift PWM strategy (CPSPWM) for suppressing the CC in modular interleaved converters was proposed. These methods effectively suppress all the harmonics of CC at a high modulation index, but they cannot successfully suppress the CC-LFHCs at a low modulation index, which degrades the quality of the output voltages and

causes extra switching and power losses in high-power applications, impacting the efficiency and reliability of the parallel system, as well as its operational lifespan. Therefore, a series of SVPWM techniques have been suggested for realizing parallel PWM converter-based grid connections with an active filter function and an SAPSS with a load voltage imbalance mitigation function. Some efforts include the use of 3-level SVPWM, while others use modified two-level SVPWM. For example, simple and discontinuous three-level SVPWM was suggested to minimize the CC and current ripple in [22, 23]. These strategies are used to control parallel PWM converters as if they were single 3-level PWM converters, which can minimize the CC while providing high efficiency and output voltage quality; however, these strategies increase the computational complexity and difficulty of implementation. Additionally, these strategies are becoming increasingly difficult to implement for multiple PWM converters connected in parallel. However, prior efforts [24-28] proposed an adjusted two-level SVPWM based on the CC-PI regulator to reduce the CC-LFHCs, especially the third harmonic and its multiples; this strategy consists of adjusting or parameterizing the zero vector duty ratios of the SVPWM using a command variable generated by the CC-PI technique. The notable advantages of this technique compared with the above-mentioned command strategies are as follows: (i) it provides a high impedance to the CC-LFHCs and is easy to realize; (ii) it is suitable for multi parallel PWM converters; (iii) it does not impact the control purposes or the output power quality of the parallel system; and it enhanced the efficiency and reliability of the parallel system, as well as its operational lifespan.

In this context, this study develops a simple and efficient CC suppression method based on a modified SPWM for a parallel connected PWM inverter system-based SAPSS. The fundamental concept of the proposed method is to eliminate the CC by eliminating the difference between ZSVs through the adjustment of inverter output voltage references using two control method. For this purpose, the inverter output voltage references are parameterized by an adjusting variable obtained from the regulation of CC or ZSC to zero using PI controller. The proposed modified inverter output voltage references method offers multiple advantages, including adjustable output voltage references for CC suppression, avoiding their effects on the output current quality under unbalanced current sharing or with discrepancies in the output-filter parameters, easy and direct control of the ZSVs, suppressing the difference between the ZSVs, providing high impedance to the CC-LFHCs, being easy to perform, being suitable for multi parallel PWM converters, and not impacting the control purposes and the output quality of the parallel system. Furthermore, the suggested approaches have the potential to enhance the efficiency, reliability, and operational lifespan of the parallel inverter-based SPSS system

by optimizing the utilization of power switching devices, minimizing unnecessary losses associated with CC and switching devices, and reducing stress on power switching devices. The remainder of this theses is organized as follows.

Chapters 1 and 2 describes the basic topology of three phase inverters-based SPSS and explains how they can be used for renewable energy generation as a SAPSS.

Chapter3, describes the mathematical model of the parallel three phase inverters system in with average equivalent circuits and the CC mechanisms and characteristics are analyzed and presented in this chapter. Then the CC suppression techniques based on PI controllers for the regulations of inverter's output currents and CC are described with simulation results using MATLAB under both cases, unbalanced output filter inductance values and unequal output current distribution.

Finally, in chapter 4, we use the super twisting control technique for regulating the inverter's output currents, aiming to improve its performance and quality, as well as CC elimination.

CHAPTER I

Three phase PWM inverters

I.1. Introduction:

The increasing demand for flexible, efficient, and reliable power systems has accelerated the adoption of power electronic converters across various applications. Among these, inverters play a critical role in converting DC power into AC form, enabling integration with the electrical grid and AC loads. When high power is required, operating multiple inverters in parallel becomes essential. However, this configuration introduces significant challenges, including power imbalance and circulating currents. These issues can degrade performance, reduce system efficiency, and cause thermal stress. Therefore, effective control strategies are necessary to ensure stable and balanced operation. This chapter provides an overview of inverter types, their modulation techniques, and the technical considerations involved in parallel operation. It also highlights the need for advanced control mechanisms to suppress circulating currents and maintain output power quality.

I.2. Energy conversion:

Historically, the shaping of electrical energy was carried out using complex assemblies based on rotating machines (dynamic converters). The rise of power semiconductors in the early 60s allowed a rapid development of static converters of electrical energy (as opposed to dynamic converters). Static converters are therefore now used to shape electrical energy and thus make it possible to adapt the different energy sources to the different loads. These static converters consist of electronic switches based on semiconductors and passive elements. They allow the transfer of energy while guaranteeing a correct efficiency. Indeed, the semiconductors are used

in switching mode so as to shape the electrical energy [4]. The different types of converters are illustrated

I.2.1. The DC/DC converter:

The function of the choppers is to supply a variable DC voltage from a fixed DC voltage. They can be isolated, and comprise a transformer ensuring galvanic isolation, or non-isolated [4]. Non-isolated converters can be divided into two types depending on their behavior and the direction of the energy they transfer, we distinguish as follows: non-reversible choppers which allow the transfer of energy from the source to the load only, Reversible choppers where the source can operate under load and vice versa, It is therefore possible to reverse the direction of travel of the energy. There are three types of reversible choppers depending on the type of conversion:

- The current reversible choppers
- The voltage reversible choppers
- The current and voltage reversible choppers.

I.2.2. The AC/AC converter

A dimmer is a power electronics device intended to modify an electrical signal in order to vary its voltage and its effective output current and thus modify the power in the load. This device is used on alternating voltages (often sinusoidal): it is a direct alternating-alternating converter [4].

The dimmer uses a triac varying the effective voltage at the output of the assembly. For high-power equipment, the dimmers can be made by groups of thyristors mounted in anti-parallel, or possibly by thyristor-diode association in the case of connection to polyphase networks.

Dimmers are used to make dimmers for certain appliances operating on the network, for the regulation of electric heating, as well as many industrial processes.

I.2.3. The DC/AC converter (Inverter)

An inverter is a power electronics device for supplying alternating voltages and currents from a continuous electrical energy source. This is the inverse function of a rectifier. The inverter is a static DC/AC converter [5] [6].

The inverter is one of the most widespread assemblies in power electronics, it has multiple applications:

- Uninterruptible power supplies.
- The connection of the solar panels to the electricity grid.
- Variable speed drives for reciprocating machines: the mains voltage is rectified and then an inverter transforms it to a voltage whose frequency and shape are adjustable.

I.2.4. The AC/DC converter (Rectifier)

A rectifier, also called AC/DC converter, is a converter intended to power a load that needs to be powered by a DC voltage or current from an AC source. The power supply is, most of the time, a voltage generator [4].

Uncontrolled rectifiers, essentially made from diodes, are used when the output voltage does not need to be adjusted.

The controlled rectifiers whose output voltage can be variable comprise thyristors or assemblies of diodes and thyristors. These rectifiers are always used at high power and when it is necessary to regulate or vary the quantities

electrical output. At low and medium power, controlled thyristor rectifiers are becoming obsolete and are advantageously replaced by the cascading of an uncontrolled rectifier and a DC/DC converter. In small powers, the control of an IGBT is simpler than that of a thyristor [4].

I.2.5. The power switches

The power converter is mainly made up of two types of components: passive components and active components. The elementary active component of power electronics is the power switch in the broad sense. This switch is made of a semiconductor material which allows it to be either on or blocked. Although this basic function is shared by all switches, there are no less a significant number of different components [7]. These switches can be differentiated according to many criteria, the main ones being:

• Their current conduction mode and their voltage resistance.

• Their type of priming: spontaneous opening and closing, controlled opening and closing or one controlled priming and the other spontaneous.

• Their type of control: current or voltage control, by continuous signals or by pulse.

Each component is then defined by a set of data and technical characteristics:

• Keeping them in tension.

• Kept them in the loop.

• Their maximum operating frequency

• Their static performance in the on state: resistance in the on state Ron and in the off state: leakage current If.

• The maximum power that the component can dissipate.

• Their price.

I.3. The inverters

I.3.1. Classification of inverters

A first classification can be made by distinguishing: non-autonomous inverters and autonomous inverter.

I.3.1.1.Non-autonomous inverter

An inverter is said to be non-autonomous if the energy necessary for switching the thyristors is supplied by the alternating network, which is therefore an active network. This is the case of inverter operation of rectifiers. The frequency and the waveform of the voltage are imposed by the alternating network [5].

I.3.1.2.Autonomous inverter

An autonomous inverter is a static converter providing DC-AC conversion. Continuously powered, it periodically modifies the connections between the input and the output and makes it possible to obtain alternating current at the output. An autonomous inverter depends essentially on the nature of the generator and the receiver between which it is mounted this leads to distinguish [5]:

- voltage inverters.
- Current inverters.

I.3.2.Types of autonomous voltage inverters:

I.3.2.1.Single-phase inverters:

To obtain an alternating voltage from a direct voltage using two switches, a midpoint is required, either on the side of the alternating output, or on the side of the direct input, this corresponds to :

- the single-phase inverter with a midpoint output transformer called the pushpull inverter (Figure I-1).
- the single-phase inverter with capacitive divider at the input called a half–bridge inverter. (Figure I-2).

• If we want to vary the relative width of the square waves forming the half-waves of the output voltage, we need four switches, that is: the single-phase bridge inverter (Figure I- 3). [8]

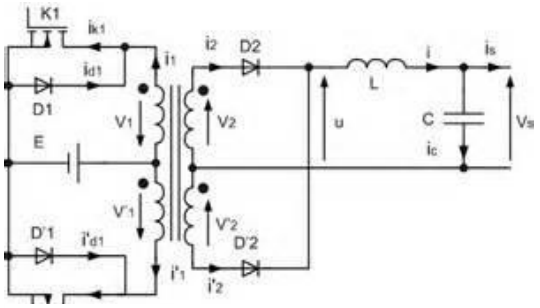


Figure I 1 Single-phase inverter with mid-bridge output transformer

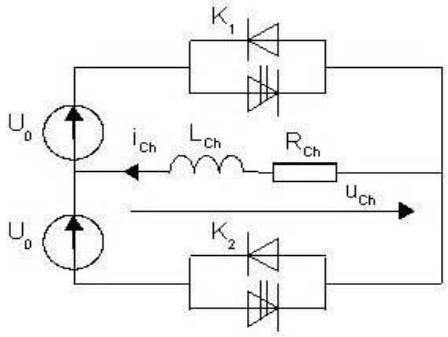


Figure I 2 Single-phase inverter with capacitive divider

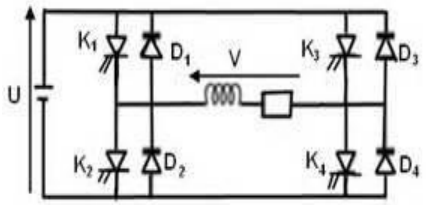


Figure I 3 Single-phase bridge inverter

I.3.2.2.Three-phase inverters

The three-phase voltage inverter follows immediately from three single-phase half-bridges, the three-phase inverter with six switches is obtained (Fig. I-4). Each half-bridge comprises a thyristor (or a transistor) and a diode.the DC voltage source is obtained from a rectifier bridge. To ensure the continuity of the alternating output currents ia, ib, ic, the switches S_{a1}, S_{a1}' and S_{a2}, S_{a2}', S_{a3} and S_{a3}' must be complementary two by two.

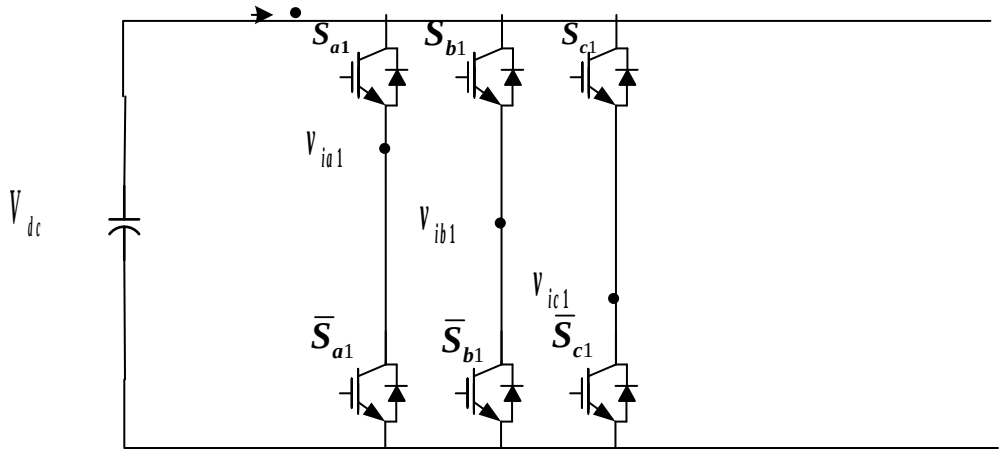


Figure I 4 Three-phase voltage inverter

I.3.2.3.The multi-level inverters

Multi-level inverters make it possible to increase the output voltage of static converters beyond the limits of semiconductors. To realize them or must have several DC voltage sources (obtained for example from a capacitive divider) [5]. It is possible to make as many elementary switching cells appear and associate them by superimposing them or by cascading them. This makes it possible to multiply the number of levels that can be given to the output voltage. The latter is often obtained by pulse width modulation (PWM). These inverters are used for driving high-power asynchronous motors, other applications are possible for motors that rotate at high speed (> 5000 rpm) [8].

I.3.3. Types of modulations

Several modulation techniques have been adopted in order to improve the quality of the voltage at the output of the inverter, among which we can mention:

I.3.3.1.Multiple linear modulation (UPWM)

In this technique, a triangular carrier is compared with a linear reference signal. The output wave is in the form of a pulse train in square waves of equal widths (Fig. I.4). If the modulation

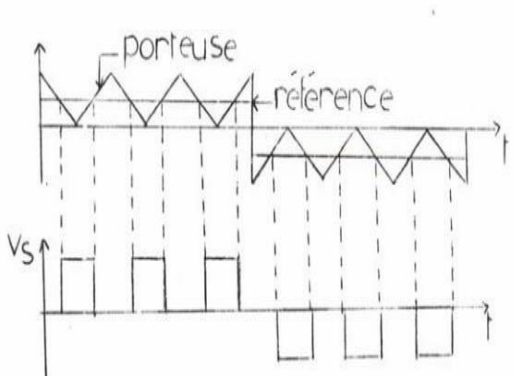


Figure I 5 Multiple pulse width modulation

index is equal to one, the singular modulation is obtained, in which the output signal is formed by a single pulse per half-period. [8].

I.3.3.2. The unipolar triangular sinusoidal modulation (SPWM):

In this case, the reference signal is sinusoidal, a wave formed by a pulse train of variable width is obtained at the output of the inverter (Fig. I.6). The switching instants are determined by points of intersection between the carrier and the modulator. The switching frequency of the switches is fixed by the carrier [8].

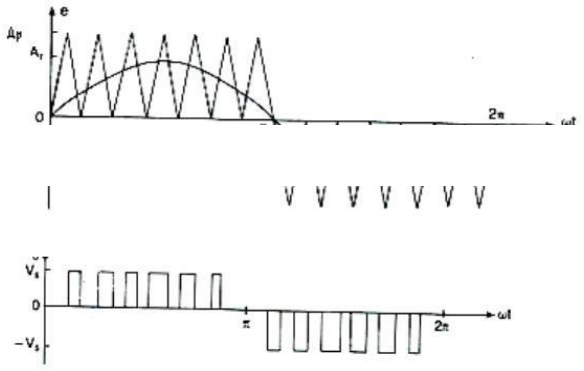


Figure I 6 Pulse width modulation,

I.3.3.3. Partial (or modified) sine wave modulation (MSPWM)

The reference signal is always sinusoidal, except that in this technique the carrier is not applied to the middle of the alternations of the sinusoid (Fig. I.7).

I.3.3.4. Vector Modulation (SVPWM)

Vector PWM is the recently best suited method for the control of asynchronous motors. Unlike other methods, the vector PWM does not rely on separate calculations of the modulations for each of the arms of the inverter. This PWM technique follows the following principles ([8], [9]):

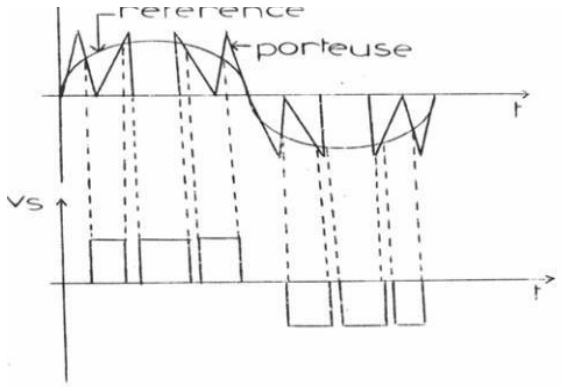


Figure I 7 modulation à largeur d'impulsion modifiée

• A reference voltage vector Vref is calculated globally and approximated over a modulation period "Tm" by an average voltage vector.

• For each phase, a pulse of width T centered on the period is produced, the average value of which is equal to the reference voltage at the sampling instant.

• All the switches of the same half-bridge have an identical state in the center and at both ends of the period.

The evolution of the power supplied by renewable energies requires new techniques for the transfer of energy from the DC bus to the electricity grid. Techniques have been developed. Among the latter, mention may be made of the paralleling of several switches in a switching cell, and the paralleling of the inverters.

I.4. The parallel association of semiconductors:

The paralleling of semiconductors has been used for many years in order to transfer the maximum power [10]. The main constraint during the parallel association of the components is to keep the semiconductors in their safety area and therefore not to exceed their maximum allowable current and voltage. Therefore, their study is very complex. Fig. I-8 illustrates a model of the parallel association of the components.

The realization of the auxiliary circuits helping the simultaneous opening and closing of the various switches placed in parallel is complex. Failure to comply with this instruction jeopardizes the entire conversion process.

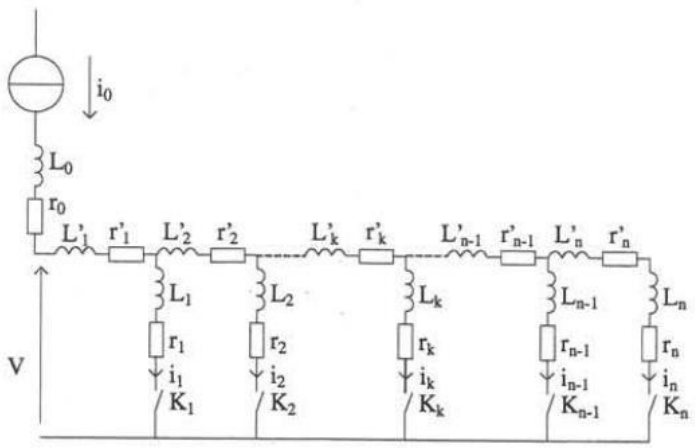


Figure I 8 Model used for the study of the association of n semiconductors in parallell

I.5.The paralleling of the inverters

The paralleling of inverters is often used to achieve levels of powers beyond the capacity of the greatest power that a structure can provide classic. In high power applications, we will have to use structures allowing on the one hand to obtain a strong output current, and on the other hand to be able to control according to the desired application [11] [12] [13] [14] [15].

The operation of the parallel inverters according to a modular configuration, gives a lot of advantages, and we can mention:

• High reliability.
• High power.
• High performance.
• Continuity of service in case of offloading of a module.
• The use of mature components.
• High flexibility and redundancy.
• The possibility of increasing the switching frequency.

The paralleling of three-phase inverters has interesting advantages such simplicity, ease of maintenance ..., but an imbalance of currents can cause a circulating current between modules which will greatly impair the sharing of power supplies to the load along the parallel-connected inverters [4].

I.6. Circulation Current

When we change the parameters of one of the two SPWMS while keeping the others fixed circuit parameters, a circulation current between the inverter modules takes birth. This is due to the fact that the switching intervals of the two inverters are different. This is due to the difference in the potential generated by the two inverters. This current causes an overload on one of the two inverters connected in parallel. This generates a decrease in the reliability of the system and can even cause the complete shutdown of the circuit. One circulating current can also be the cause of a difference between the impedances of a same inverter.

I.7. Conclusion:

In this chapter, we have introduced the parallel connection of the inverters used for the high power transfer. The latter generates a path of the circulation current which decreases the efficiency of the system thus the yield.

A study of this circulation current and a regulation will be detailed in the next chapter.

Chapter II
Modeling and control of Three-phase Voltage Source Inverter

II.1. Introduction

Standalone Power Supply System (SPSS) refers to a localized, self-sufficient electrical system typically designed to operate independently of a main utility grid. It is commonly implemented in remote or off-grid areas where grid connection is impractical or unavailable. A typical SPSS comprises distributed energy sources, such as photovoltaic (PV) panels, wind turbines, fuel cells, or diesel generators, interfaced through power electronic converters to supply local loads. These energy sources may be powered by renewable or non-renewable fuels, and in some cases, may incorporate combined heat and power (CHP) units to improve overall system efficiency through waste heat recovery.

In an AC SPSS, energy sources are commonly connected to the load through a three-phase voltage source inverter (VSI), which plays a crucial role in regulating the system's voltage and frequency. The VSI serves as the main control interface between the DC power sources and the AC load, ensuring stable operation and power quality under varying load and generation conditions. Control of the output voltage amplitude and frequency is achieved using only local measurements of the inverter’s output voltages and currents.

This chapter presents the fundamental circuit model of a three-phase VSI-based SPSS and details its voltage and frequency control strategies. As illustrated in Fig. II.9, the power circuit consists of a constant DC power source, a three-phase VSI connected to the load via an LC filter and coupling line impedance, and a voltage controller. The controller regulates the capacitor voltage both in amplitude and frequency: the frequency is maintained by controlling the phase angle of the output voltage (used in the transformation between the abc frame and the synchronous dq-frame), while the voltage amplitude is managed through a dual-loop control structure. This consists of an outer voltage loop and an inner current loop, typically implemented using proportional-integral (PI) controllers in the dq frame to ensure both voltage regulation and transient current suppression.

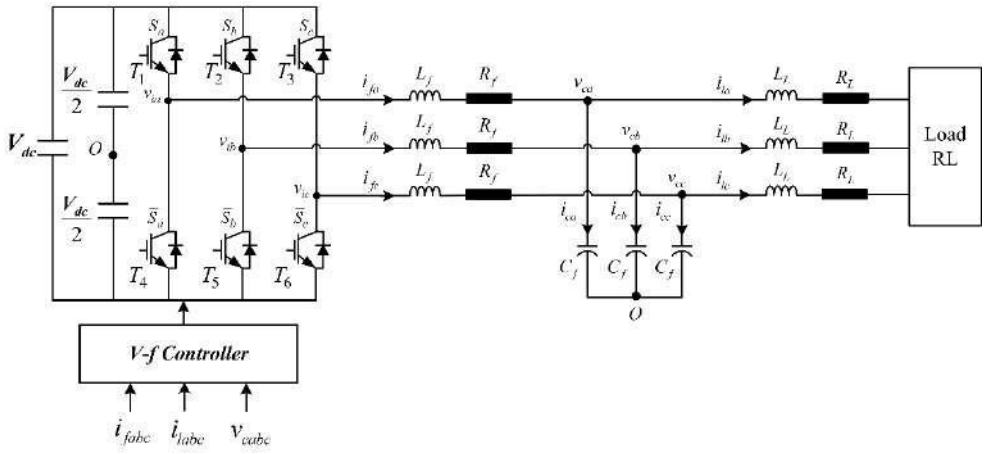


Figure II 1 The basic topology of three-phase VSI based DG an islanded MG

In this figure, V_{dc} is the DC input voltage, L_f is the filter inductor, R_f is the filter resistance and C_f is the filter capacitor. a, b, and c three-phase inverter arms from left to right. The three-phase output voltages of the inverter are v_{ia}, v_{ib}, v_{ic}. The three-phase filter capacitor at the output is star-connected and (*o)* is the midpoint of the filter capacitor. The output voltages of the inverter are the capacitor voltages v_{ao}, v_{bo}, v_{co}. The three phase inductor or VSI output currents are i_{fabc}. The three-phase output capacitor voltages are v_{cabc}.The three phase output currents of the load are i_{labc}. The establishment of a mathematical model of a three-phase VSI is the basis for its theoretical analysis and is a prerequisite for the design of reasonable control parameters.

II.2. Modeling of Three-phase Voltage Source Inverter (VSI)

The modeling and local control of the three-phase VSI unit are critical for the reliable and efficient operation of AC SPSSs. By developing accurate models and effective control strategies, we can enhance the performance, stability, and resilience of microgrids, paving the way for sustainable and autonomous energy systems.

II.2.1. Voltage Source Inverter (VSI)

VSI uses semiconducting switches to convert DC voltage to AC voltage. Because the inverter relies on DC sources, the VSIs are essential to the functioning of the SPSS that is being studied. Each VSI's control system is also used to manage the SPSS locally. Fig. II.2 shows a three-phase VSI with an output voltage vi and an input dc-voltage Vdc. Together with the input DC voltage at the inverter, the VSI's switching determines the output voltage vi. The next part will cover pulse-width modulation, which is a common method of controlling the semiconducting switches in the three phase VSI. This control circuit is independent from the rest of the system.

The subsequent section will discuss pulse-width modulation (PWM), a widely employed technique for controlling the semiconductor switches within a three-phase VSI. Notably, this control

circuit operates independently from the rest of the system.

II.2.2. Averaged VSI Model

The averaged circuit model of the three phase inverter is given as in Fig. II. 2.

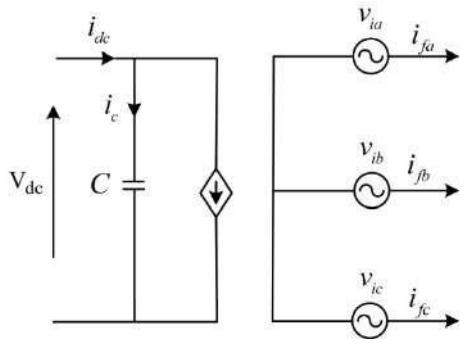


Figure II 2 Averaged VSI model circuit

Equation (II.1) represents the active power on the input of the VSI, while equation (II.2) represents the instantaneous active power on the output of the VSI.

$$P_{dc\,inv} = v_{dc}\, i_{dc} \quad \text{(II.1)}$$

$$P_{ac\,inv} = v_{ia}\, i_{fa} + v_{ib}\, i_{fb} + v_{ic}\, i_{fc} \quad \text{(II.2)}$$

The DC input power P_{dcinv} is equal to the AC output inverter power P_{acinv} if both the inverter power losses and commutation power losses are ignored.

II.2.3. Switched Model of the VSI-based DG

The VSI depicted in Fig. II.1 functions by turning the switching elements ON or OFF in response to the status of the control signals (Sa, Sb, and Sc) generated by the PWM approach. Regardless of i_{fx} polarity, the waveform of the VSI output voltage vix is exclusively governed by the switching functions given by:

$$S_x = \begin{cases} 1 \text{ if } T_x \text{ is close and } T_{x+3} \text{ is open} \\ 0 \text{ if } T_x \text{ is open and } T_{x+3} \text{ is close} \end{cases} \qquad x = a, b, c \quad \text{(II.3)}$$

As shown in Fig. II.2, the three input voltages of the VSI (vao, vbo, and vco) called also the potentials of the nodes a, b, and c of the VSI with respect to the imaginary midpoint (o) are expressed as a function of the switching states and DC voltage by:

$$S_x = \begin{cases} v_{ao} = \frac{V_{dc}}{2}(2s_a - 1) \\ v_{bo} = \frac{V_{dc}}{2}(2s_b - 1) \\ v_{co} = \frac{V_{dc}}{2}(2s_c - 1) \end{cases} \quad \text{(II.4)}$$

Using this equation, the VSI line-to-line output voltages are represented as follows:

$$\begin{cases} v_{ao} = v_{ao} - v_{bo} = v_{dc}(S_a - S_b) \\ v_{bc} = v_{bo} - v_{co} = v_{dc}(S_b - S_c) \\ v_{ca} = v_{co} - v_{oo} = v_{dc}(S_c - S_a) \end{cases} \quad \text{(II.5)}$$

These line-to-line output voltages are also expressed as a function of the line-to-neutral voltages by:

$$\begin{cases} v_{ab} = v_{an} - v_{bn} \\ v_{bc} = v_{bn} - v_{cn} \\ v_{ca} = v_{cn} - v_{an} \end{cases} \quad \text{(II.6)}$$

This gives:

$$\begin{cases} v_{ab} - v_{ca} = v_{an} - (v_{bn} + v_{cn}) + v_{an} \\ v_{bc} - v_{ab} = v_{bn} - (v_{cn} + v_{an}) + v_{bn} \\ v_{ca} - v_{bc} = v_{cn} - (v_{an} + v_{bn}) + v_{cn} \end{cases} \quad \text{(II.7)}$$

Since the sum of the voltages in a balanced three-phase system is:

$$v_{an} + v_{bn} + v_{cn} = 0 \quad \text{(II.8)}$$

From equations (II.7) and (II.8), we can write:

$$\begin{cases} v_{an} = -(v_{bn} + v_{cn}) \\ v_{bn} = -(v_{an} + v_{cn}) \\ v_{cn} = -(v_{an} + v_{bn}) \end{cases} \quad \text{(II.9)}$$

According to equations (II.7) and (II.9), the output line-to-neutral voltages of the VSI are expressed as follows:

$$\begin{cases} v_{an} = \frac{v_{ab} - v_{ca}}{3} \\ v_{bn} = \frac{v_{bc} - v_{ab}}{3} \\ v_{cn} == \frac{v_{ca} - v_{bc}}{3} \end{cases} \quad \text{(II.10)}$$

According to equations (II.5) and (II.10), the output line-to-neutral voltages of the VSI are expressed

as a function of the DC voltage and switching states (S_a, S_b, S_c) by the following equation:

$$\begin{Bmatrix} v_{ia} \\ v_{ib} \\ v_{ic} \end{Bmatrix} = \frac{V_{bc}}{3} \begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix} \begin{pmatrix} S_a \\ S_b \\ S_c \end{pmatrix} \tag{II.11}$$

From this equation, the output line-to-neutral voltages of the VSI within its eight different switching states are given in the abc and $\alpha\beta$ stationery reference frames as in the Tab. 2.1:

Table 1 Possible voltage vectors of the VSI in abc and αβ stationery reference frames

S_c	S_b	S_a	V_{ia}	V_{ib}	V_{ic}	V_α	v_β	$\vec{v}_i$
0	0	0	0	0	0	0	0	$\vec{v}_0$
0	0	1	$-\frac{V_{dc}}{3}$	$-\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$-\frac{V_{dc}}{\sqrt{6}}$	$-\frac{V_{dc}}{\sqrt{2}}$	$\vec{v}_1$
0	1	0	$-\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$-\frac{V_{dc}}{3}$	$-\frac{V_{dc}}{\sqrt{6}}$	$\frac{V_{dc}}{\sqrt{2}}$	$\vec{v}_2$
0	1	1	$-\frac{2V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$-\sqrt{\frac{2}{3}}V_{dc}$	0	$\vec{v}_3$
1	0	0	$\frac{2V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\sqrt{\frac{2}{3}}V_{dc}$	0	$\vec{v}_4$
1	0	1	$\frac{V_{dc}}{3}$	$-\frac{2V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{\sqrt{6}}$	$-\frac{V_{dc}}{\sqrt{2}}$	$\vec{v}_5$
1	1	0	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$-\frac{2V_{dc}}{3}$	$\frac{V_{dc}}{\sqrt{6}}$	$\frac{V_{dc}}{\sqrt{2}}$	$\vec{v}_6$
1	1	1	0	0	0	0	0	$\vec{v}_7$

Using the eight vector states and their correspondent output voltages in the Tab. II.1, we provide the switching polygon of the VSI as shown in Fig II.3.

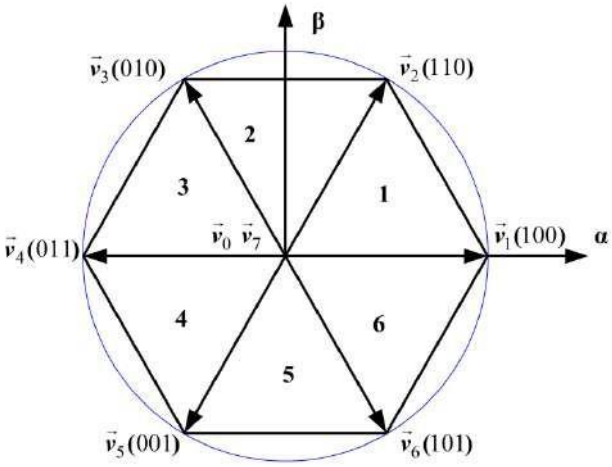


Figure II 3 Representation of the switching polygon of the VSI

The matrix form of (II.11) yields the following equation, which defines the VSI conversion matrix:

$$\begin{bmatrix} v_{ia} \\ v_{ib} \\ v_{ic} \end{bmatrix} = \frac{V_{bc}}{3} \begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix} \begin{pmatrix} S_a \\ S_b \\ S_c \end{pmatrix} \tag{II.12}$$

On the DC side, the output current is determined by:

$$Idc = \begin{bmatrix} S_a S_b S_c \end{bmatrix} \begin{bmatrix} i_{fa} \\ i_{fb} \\ i_{fc} \end{bmatrix} \tag{II.13}$$

II.3. Dynamic model of the three phase VSI

II.3.1. Model of the three phase VSI in the*abc* reference frame

Using Kirchhoff's theorem in the Fig. II.1, the VSI output current and capacitor voltages dynamics may be expressed as follows:

$$\begin{cases} C_f = \dfrac{dv_{ca}}{dt} = i_{ca} = i_{fa} - i_{La} \\ C_f = \dfrac{dv_{cb}}{dt} = i_{cb} = i_{fb} - i_{Lb} \\ C_f = \dfrac{dv_{cc}}{dt} = i_{cc} = i_{fc} - i_{Lc} \end{cases} \tag{II.15}$$

$$\begin{cases} L_f = \dfrac{dv_{fa}}{dt} = i_{ia} - R_f i_a - i_{ca} \\ L_f = \dfrac{dv_{fb}}{dt} = i_{ib} - R_f i_b - i_{cb} \\ L_f = \dfrac{dv_{fc}}{dt} = i_{ic} - R_f i_c - i_{cc} \end{cases} \quad \text{(II.16)}$$

II.3.2. Model of the three phase VSI in the *αβ* reference frame

By applying the Park transformation while preserving power invariance, known as the Concordia transformation, the VSI output voltages can be expressed in the αβ-reference frame as follows:

$$\begin{bmatrix} V_{i\alpha} \\ v_{i\beta} \end{bmatrix} = T_{3,2} \begin{bmatrix} v_{ia} \\ v_{ib} \\ v_{ic} \end{bmatrix} \quad \text{(II.17)}$$

where:

$$T_{3,2} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \quad \text{(II.18)}$$

Similarly, the capacitor voltages are expressed in the *αβ*-reference frame are given by:

$$\begin{bmatrix} V_{c\alpha} \\ v_{c\beta} \end{bmatrix} = T_{3,2} \begin{bmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \end{bmatrix} \quad \text{(II.19)}$$

Also, the output currents of the VSI in the *αβ*-reference frame are represented as follows:

$$\begin{bmatrix} i_{f\alpha} \\ i_{f\beta} \end{bmatrix} = T_{3,2} \begin{bmatrix} i_{fa} \\ i_{fb} \\ i_{fc} \end{bmatrix} \quad \text{(II.20)}$$

It is advised to convert the three-phase system into a virtual two-phase system in order to simplify the prior VSI model. This results in:

After converting the dynamics of the capacitor voltages and VSI output currents in equations (II.15) and (II.16) from the *abc*-reference frame into *αβ*-reference frame, we obtained:

$$\begin{cases} C_f = \dfrac{dv_{c\alpha}}{dt} = i_{c\alpha} = i_{f\alpha} - i_{L\alpha} \\ C_f = \dfrac{dv_{c\beta}}{dt} = i_{c\beta} = i_{f\beta} - i_{L\beta} \end{cases} \quad \text{(II.21)}$$

$$\begin{cases} L_f = \dfrac{dv_{f\alpha}}{dt} = i_{i\alpha} - R_f i_{f\beta} - i_{c\alpha} \\ L_f = \dfrac{dv_{f\beta}}{dt} = i_{i\beta} - R_f i_{\beta} - i_{c\beta} \end{cases} \quad \text{(II.22)}$$

The input DC current of the VSI in equation (II.13) is given as function of the switching states and output current in the *αβ*-reference frame as follows;

$$I_{dc} = S_a i_{fa} + S_\beta i_{f\beta} \quad \text{(II.23)}$$

where:

$$\left[S_\alpha S_\beta\right] = T_{3,2}\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \quad \text{(II.24)}$$

II.3.3. Model of the three phase VSI in the *dq* reference frame

By applying the direct Park transformation on the VSI output voltages in equation (II.17), we obtained these voltages in the dq reference frame as follows

$$\begin{bmatrix} v_{id} \\ v_{iq} \end{bmatrix} = T_{Park}\begin{bmatrix} v_{i\alpha} \\ v_{i\beta} \end{bmatrix} \quad \text{(II.25)}$$

where:

$$T_{Park} = \begin{bmatrix} \cos\omega t & \sin\omega t \\ -\sin\omega t & \cos\omega t \end{bmatrix} \quad \text{(II.26)}$$

Also, using this transformation, we convert the capacitor voltages from the *αβ*-reference frame into the dq reference frame as follows:

$$\begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix} = T_{Park}\begin{bmatrix} v_{c\alpha} \\ v_{c\beta} \end{bmatrix} \quad \text{(II.27)}$$

Similarly, we obtained the output currents of the VSI in the *dq*-reference frame as follows:

$$\begin{bmatrix} i_{fd} \\ i_{fq} \end{bmatrix} = T_{Park}\begin{bmatrix} i_{f\alpha} \\ i_{f\beta} \end{bmatrix} \quad \text{(II.28)}$$

After converting the dynamics of the capacitor voltages and VSI output currents in equations (II.21) and (II.22) from the *αβ*-reference frame into dq reference frame, we obtained:

$$\begin{cases} C_f \dfrac{dv_{cd}}{dt} = i_{cd} + \omega C_f v_{cq} \\ C_f \dfrac{dv_{cq}}{dt} = i_{cq} + \omega C_f v_{cd} \end{cases} \quad \text{(II.29)}$$

$$\begin{cases} L_f \dfrac{dv_{fd}}{dt} = v_{id} - R_f i_{fd} + \omega L_f i_{fq} - v_{cd} \\ L_f \dfrac{dv_{fq}}{dt} = v_{iq} - R_f iq - \omega L_f i_{fd} - v_{cq} \end{cases} \quad \text{(II.30)}$$

The input DC current of the VSI in equation (II.13) is given as function of the switching states and output current in the *dq*-reference frame as follows:

$$I_{dc} = S_d i_{fd} + S_q i_{fq} \quad \text{(II.31)}$$

II.4. Instantaneous active and rective powers in *abc* frame

II.4.1. Instantaneous active power (*P*)

In a three-phase VSI in Fig. II.1, the instantaneous active power is provided by:

$$P = v_{ca} i_{la} + v_{cd} i_{lb} + v_{cc} i_{lc} \quad \text{(II.32)}$$

II.4.2. Instantaneous rective power (*Q*)

The instantaneous reactive power in a three-phase system can be defined in terms of the cross-products of the capacitor voltages and VSI output currents. One common definition uses Clarke transformation to transform the abc-frame quantities to the $\alpha\beta$-frame and then compute the reactive power. However, in the abc-frame, an alternative approach involves defining a power that represents the energy exchanged between phases, which does not contribute to the net energy transfer to the load. This definition is less straightforward but can be understood as:

$$Q = \frac{1}{\sqrt{3}}\left[(v_{ca} - v_{cd}) i_{lc} + (v_{cb} - v_{cc}) i_{la} + (v_{ca} - v_{cc}) i_{lc}\right] \quad \text{(II.33)}$$

II.4.3. Instantaneous active and rective powers in $\alpha\beta$ -frame

By taking into account balanced three-phase systems and defining capacitor voltage and VSI output current phases as $\overline{V}_{c\alpha\beta} = V_{c\alpha} + jV_{c\beta}$ and $\boldsymbol{\overline{I}_{l\alpha\beta} = I_{l\alpha} - jI_{\beta}}$, respectively, the apparent complex power

in $\alpha\beta$-frame may be written as follows [ ]:

$$S = P + jQ = \bar{V}_{c\alpha\beta} I_{l\alpha\beta_{ref}} = \left(V_{c\alpha} + jV_{c\beta}\right)\left(I_{l\alpha} - jI_{l\beta}\right) \quad \text{(II.34)}$$

The active and reactive powers as functions of capacitor voltages and VSI output currents in the $\alpha\beta$-frame can be expressed by rearranging equation (II.34)) as follows:

$$\begin{cases} P = V_{cd} I_{ld} + V_{cq} I_{lq} \\ Q = V_{cd} I_{lq} - V_{cq} I_{ld} \end{cases} \quad \text{(II.35)}$$

II.4.4. Instantaneous active and rective powers in the *dq*-frame

Similar to this, the apparent complex power in the *dq*-frame may be found by using $\bar{V}_{cdq} = v_{cd} + jv_{cq}$ and $\bar{I}_{ldq} = i_{ld} - ji_{lq}$ as the capacitor voltage and VSI output current phases, respectively [ ]:

$$\bar{S} = P + jQ = V_{cdq} I_{ldq_{ref}} = \left(V_{cd} + jV_{cq}\right)\left(I_{ld} - jI_{lq}\right) \quad \text{(II.36)}$$

The active and reactive powers as functions of capacitor voltages and VSI output currents in the dq reference frame can be expressed by rearranging equation (II.36) as follows:

$$\begin{cases} P = V_{cd} I_{ld} + V_{cq} I_{lq} \\ Q = V_{cd} I_{lq} - V_{cq} I_{ld} \end{cases} \quad \text{(II.37)}$$

II.5. Low-Pass Filter (LPF)

The three phase VSI output filter circuits are essential components in power converter systems, particularly in applications where the quality of the output waveform is crucial, which has an important influence on the dynamic and static performance of the VSI output voltage and current control. These filters help to reduce harmonic distortion, mitigate high-frequency noise, and shape the output voltage waveform to meet specific requirements. There are three common types of output filter circuits: L, LC, and LCL filters.

II.5.1. Inductive Filter (L Filter)

A single inductor filter, also known as an L filter, is a basic type of output filter commonly used in power electronic systems, including VSIs. It consists of a single inductor L connected in series with the output load. This configuration forms a low-pass filter that attenuates high-frequency harmonics while allowing the fundamental frequency component (desired output frequency) to pass through with minimal attenuation.this filter is shown in Fig. II.12:

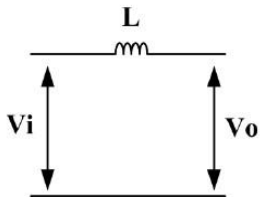


Figure II 4 L Filter

II.5.2. Inductive-capacitive Filter (LC Filter)

The LC filter is typically used to removing the higher-order harmonics from the outputs of the VSIs. The cut-off frequency (fc) of this filter is a trade-off between VSI control bandwidth and harmonic attenuation effect. Decreasing the cut-off frequency increases the harmonic attenuations; but can limits the VSI control bandwidth.

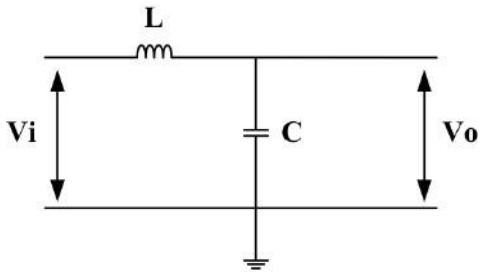


Figure II 5 LC Filter

Advantages:

- Simple and economical.
- Provides basic filtering for reducing harmonic distortion.

Disadvantages:

- Limited effectiveness in attenuating high-order harmonics.
- Can introduce resonances if not properly designed.

II.5.3. Inductive-capacitive-inductive Filter (LCL Filter)

The LCL filter is an advanced version of the LC filter, incorporating two inductors (Lf1 and Lf2) and a capacitor (Cf). It provides better harmonic attenuation and improved filtering performance compared to the LC filter. The additional inductor (Lf2) helps to mitigate resonances and provides additional filtering of higherorder harmonics. this filter is shown in Fig. II.13

Advantages:

- Better harmonic attenuation compared to LC filters.
- Helps to suppress resonances and improve stability.

Disadvantages:

- More complex and expensive compared to LC filters.

• Requires careful design to prevent resonance and ensure stability

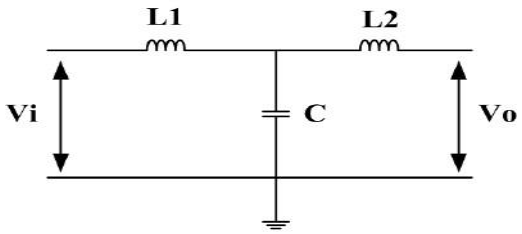


Figure II 6 LCL filter

In this theses we are speak to LC Low-Pass filter that show in Fig. II.5:

II.5.4. Parameters tuning of LC Filter

Usually, the cut-off frequency is maintained between and three times the fundamental frequency and onefive of the switching frequency as [7]:

$$3f_0 < f_c < (1/5) f_{sw} \quad \text{(II.38)}$$

The inductance of the LC filter (L_f) is chosen such that its voltage drop remains within 3% of the VSI output voltage as follows [7]:

$$I_{f\max} \times (2\pi f L_f) < 0.03 V_{inv} \quad \text{(II.39)}$$

where:

$I_{f\max}$ is the max of the inverter output current.

According to equation (II.39), the inductance of the filter is expressed by:

$$L_f < (0.03 V_{inv}) / (I_{f\max} \times (2\pi f) \quad \text{(II.40)}$$

The cut-off frequency of the LC filter is expressed as a function of the inductance and capacitor by:

$$fc = \frac{1}{2\pi\sqrt{L_f V_f}} \quad \text{(II.41)}$$

According to this equation, the filter capacitance can be calculated as follows:

$$C_f = \frac{1}{(2\pi f_c)^2 L_f} \quad \text{(II.42)}$$

According to the system parameters in Tables A.1 and A.2 for I_{fmax} = 15 A and f_c = 150 Hz, we obtained:

L_f = 2 mH and C_f = 150 uF.

II.7. Load

As shown in Fig. II.1, a resistive-inductive linear load was selected in our thesis to study the characteristic of the inverter outputs (active and reactive powers, inverter output currents and

voltages, and line currents) of the investigated microgrid system, which has chosen to model a residential load, as given in the benchmark microgrid [ ]. This load is modelled as a constant impedance ($Z_0=R_0+jX_0$) and it adjusted to provide the nominal active, reactive, and apparent powers at the nominal voltage of the SPSS as follows:

$$\begin{cases} S_0 = \dfrac{V_{PCC}^2}{Z_0} \\ P_0 = \dfrac{V_{PCC}^2}{R_0} \\ Q_0 = \dfrac{V_{PCC}^2}{X_0} \end{cases} \quad \text{(II.43)}$$

II.8. Design of inner voltage and current controllers in the *dq*-frame

As shown in the general control schema of the three phase VSI-based SPSS shown in Fig. II.7, both capacitor voltages and VSI output currents are controlled using the Vector Oriented Control (VOC) concept, which consists of two control loops: the outer capacitor voltage control loop and the inner output current control loop. The basic principle of this method is to convert the three-phase capacitor voltage and output current quantities from the abc reference frame to the dq-frame and control them as constant vectors in the steady state with the goal of eliminating the static errors of both vectors by using PI controllers. The transformation of the three-phase capacitor voltage and output current quantities into the dq-frame is achieved using the Park transformation with power conservation named the Concordia transformation, in which the phase angle is provided using the phase locked loop (PLL). The details of different parts of the general control schema are described in the next subsections.

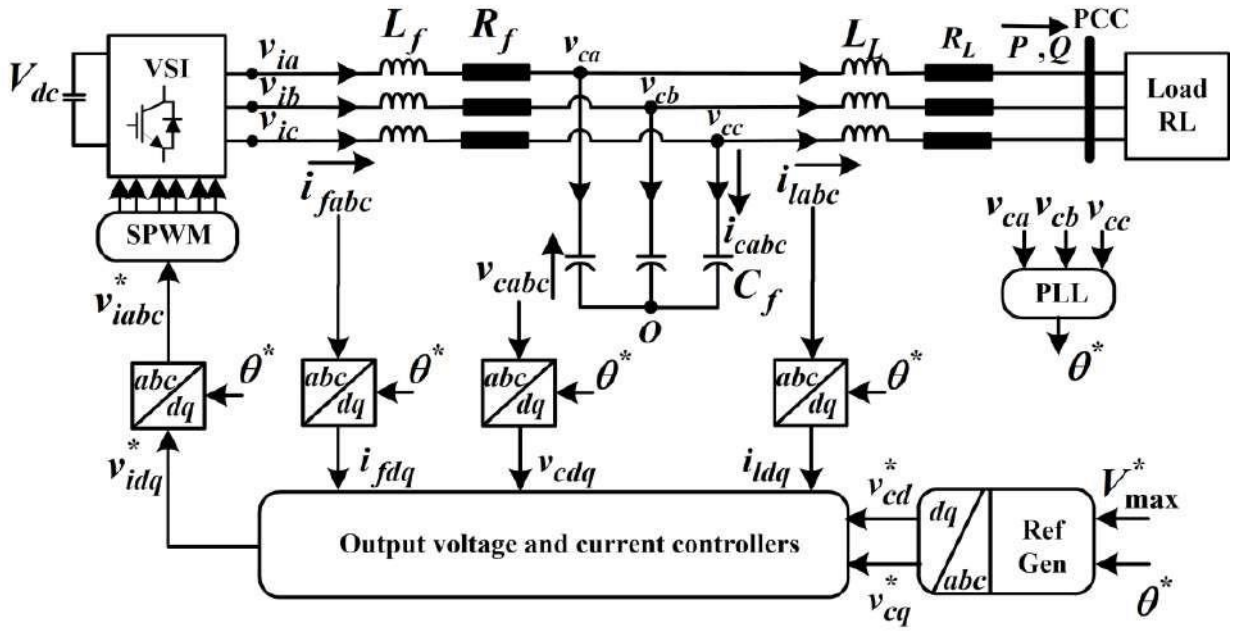


Figure II 7 Block diagram of single three-phase VSI based DG of an Islanded Microgrid with control.

II.8.1. Output currents and capacitor voltages dual classed loop controllers in the *dq* reference frame

The primary objectives of capacitor voltage control are to ensure that the voltages remain purely sinusoidal and balanced under various loading conditions, including linear and nonlinear, as well as balanced and unbalanced loads. Additionally, this control loop generates the appropriate reference signals for the inner output current control loop.

The inner output current control loop is responsible for regulating the output current to achieve multiple objectives, including controlling active and reactive power, decoupling the -axis and -axis components (thereby decoupling active and reactive power), protecting the VSI circuit from overcurrent conditions, and providing accurate VSI output voltage references. These references are subsequently used in the pulse-width modulation (PWM) stage to generate the appropriate switching states for the VSI, ensuring high-quality output voltages.

In this study, both the outer voltage control loop and the inner output current control loop are implemented using proportional-integral (PI) controllers, as illustrated in Fig. II.5.
According to the capacitor voltage dynamics in equation (II.27) we obtained the capacitor currents in the dq reference frame as follows:

$$\begin{cases} i_{cd} = \dfrac{dv_{cd}}{dt} - \omega C_f v_{cq} \\ i_{cq} = C_f \dfrac{dv_{cq}}{dt} - \omega C_f v_{cd} \end{cases} \quad \text{(II.44)}$$

The terms $C_f \dfrac{dv_{cd}}{dt}$ and $C_f \dfrac{dv_{cq}}{dt}$ are obtained with the opposite of coupling terms from the regulation of the capacitor voltages in the dq frame using *PI*-controllers as follows:

$$\begin{cases} C_f \dfrac{dv_{cd}}{dt} + \omega C_f v_{cq} = i_{cd} = (K_{pv} + \dfrac{K_{iv}}{S})(v^*_{cd} - v_{cd}) \\ C_f \dfrac{dv_{cq}}{dt} + \omega C_f v_{cd} = i_{cq} = (K_{pv} + \dfrac{K_{iv}}{S})(v^*_{cq} - v_{cq}) \end{cases} \quad \text{(II.45)}$$

The opposite of the coupling's terms is determined by the *PI*-regulators to compensate the coupling between *d-axis* and *q-axis* of the capacitor voltages.

$$\begin{cases} i^*_{fd} = i^*_{cd} + i^*_{Ld} = (K_{pv} + \dfrac{k_{iv}}{s})(i^*_{vd} - v_{cd}) - \omega C_f v_{cq} + i_{Ld} \\ i^*_{fq} = i^*_{cq} + i^*_{Lq} = (K_{pv} + \dfrac{k_{iv}}{s})(i^*_{cq} - v_{cq}) + \omega C_f v_{cd} + i_{Lq} \end{cases} \quad \text{(II.46)}$$

According to the VSI output current dynamics in equation (II.46), we obtained the VSI output voltages in the dq reference frame as follows:

$$\begin{cases} v_{id} = L_f \dfrac{di_{fd}}{dt} + R_f i_{fd} - \omega L_f i_{fq} + v_{cd} \\ v_{iq} = L_f \dfrac{di_{fq}}{dt} + R_f i_{fq} + \omega L_f i_{fd} + v_{cq} \end{cases} \quad \text{(II.47)}$$

The terms $L_f \dfrac{di_{fd}}{dt} + R_f i_{fd}$ and $L_f \dfrac{di_{fq}}{dt} + R_f i_{fq}$ represent the inductance drop voltages, which are obtained with the opposite of coupling terms from the regulation of the VSI output currents with their references obtained from the regulation of the capacitor voltages in equation (II.46)using PI controllers as follows:

$$\begin{cases} L_f \dfrac{di_{fd}}{dt} + R_f i_{fd} + \omega L_f i_{fq} = u^*_{ld} = (K_{pi} + \dfrac{k_{ii}}{s})(i^*_{fd} - i_{fd}) \\ L_f \dfrac{di_{fq}}{dt} + R_f i_{fq} + \omega L_f i_{fd} = u^*_{lq} = (K_{pi} + \dfrac{k_{ii}}{s})(i^*_{fq} - i_{fq}) \end{cases} \quad \text{(II.48)}$$

Subtracting equation (II.48) into equation (II.47), we obtain the VSI output voltage references as follows:

$$\begin{cases} v_{id}^{*} = u_{ld}^{*} + v_{cd} = (K_{pi} + \dfrac{k_{ii}}{s})(i_{fd}^{*} - i_{fd}) - \omega L_f i_{fq} + v_{cd} \\ v_{iq}^{*} = u_{lq}^{*} + v_{cq} = (K_{pi} + \dfrac{k_{ii}}{s})(i_{fq}^{*} - i_{fq}) - \omega L_f i_{fd} + v_{cq} \end{cases} \quad \text{(II.49)}$$

Furthermore, with in this control loop, the inverse of the coupling terms is computed by the PI controllers to compensate for the coupling effects between the -axis and -axis components of the VSI output currents.

Based on equations (II.46) and (II.49), the block diagram representing both control loops is given in the Fig. II.8:

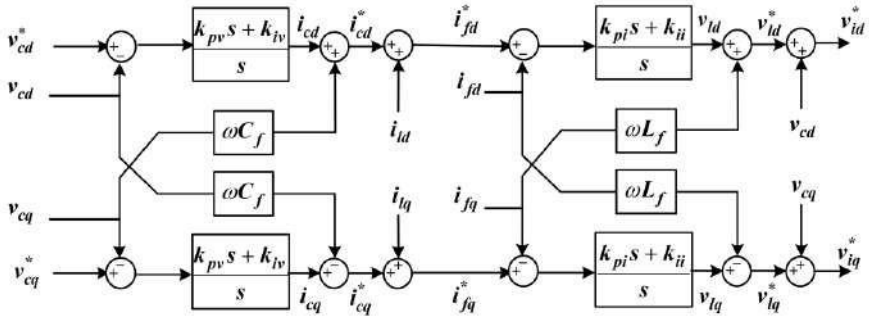
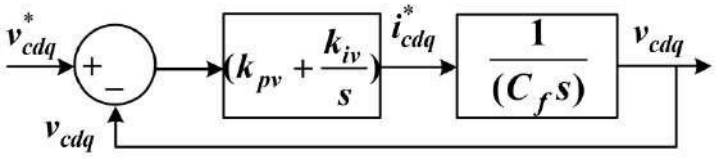


Figure II 8 Block diagram of dual loop voltage and current regulations in the dq reference frame

II.8.2. Parameter tuning of PI controllers

In steady state, when considering that the coupling terms of both control loops are compensated, the outer capacitor voltage close loop control and inner output current close loop control output current are given, respectively, in Figs. II.9 (a and b).



(a)

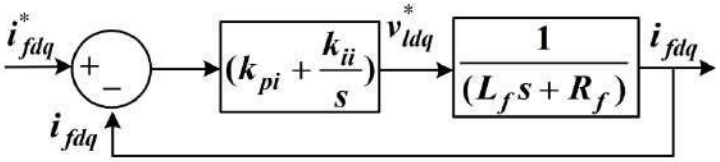


Figure II 9 Outer capacitor voltage and inner current close loop PI controllers. (a) Outer capacitor voltage close loop PIv control, (b) Inner output current close loop PIi control

(b)

According to Fig. II.10.a, the closed loop transfer function $F_v(s)$ of the capacitor voltage controller is given by:

$$F_v(s) = \frac{V_{cdq}}{V^*_{cdq}} = \frac{\frac{1}{C_f}(K_{pv}s + k_{iv})}{s^2 + \frac{k_{pv}}{C_f}s + \frac{k_{iv}}{C_f s}} \tag{II.50}$$

By identifying this transfer function with the closed loop transfer function of the second order system $F(x)$ given by equation (II.51),we obtain the gains of the PI_v as in equation (II.52):

$$F(s) = \frac{k\omega_c^2}{s^2 + 2\xi\omega_c s + \omega_c^2} \tag{II.51}$$

$$\begin{cases} \frac{k_{pv}}{C_f} = 2\xi\omega_{cv} \\ \frac{k_{iv}}{C_f} = \omega_{cv}^2 \end{cases} \Rightarrow \begin{cases} k_{pv} = 2\xi\omega_{cv}C_f \\ k_{iv} = \omega_{cv}^2 C_f \end{cases} \tag{II.52}$$

Similarly, we calculate the gains of the PI_i controller according to Fig. II.9.b as follows:

The closed loop transfer function $F_i(s)$ of the output current controller is given by:

$$F_i(s) = \frac{i_{fdq}}{i^*_{fdq}} = \frac{\frac{1}{L_f}(k_{pi}s + k_{ii})}{s^2 + \frac{(R_f + k_{pi})}{L_f}s + \frac{k_{ii}}{L_f}} \tag{II.53}$$

By identifying this transfer function with the closed loop transfer function of the second order system $F(x)$ given by equation (II.54),we obtain the gains of the PI_v as in equation (II.55):

$$F(s) = \frac{k\omega_{cv}^2}{s^2 + 2\xi\omega_c s + \omega_{cv}^2} \tag{II.54}$$

$$\begin{cases} \dfrac{R_f + k_{pi}}{L_f} = 2\xi\omega_{ci} \\ \dfrac{k_{ii}}{L_f} = \omega_{ci}^2 \end{cases} \Rightarrow \begin{cases} k_{pi} = 2\xi\omega_{ci}L_f - R_f \\ k_{ii} = \omega_{cv}^2 L_f \end{cases} \quad \text{(II.55)}$$

Where:

ξ and i ξ are respectively the damping factor of the PIv and PIi controllers. ωcv and ωci are respectively the cut-off frequency of the PIv and PIi controllers. To achieve well-damped oscillations and a slight overshoot, the voltage and current controllers have chosen a damping coefficient, ξv and ξi of 0.707. To obtain the correct response, it is therefore possible to determine the natural frequency, ωcv and ωci for each controller. The condition of choosing ωcv and ωci is knowing that the cut-off frequency of the voltage control loop is too low comparing to the cut-off frequency of the current control loop ω ω ≥10 ci cv [ ]. The outer voltage loop's lower cut-off frequency ensures stability and robustness by making the system less sensitive to high-frequency noise, disturbances, and unmolded dynamics, while the inner current loop's higher cut-off frequency provides fast response, better disturbance rejection, and decoupling. Both factors contribute to the system's robustness and stability.

II.9. Simulation results and discussions

To verify the characteristics of the three phase VSI-based SPSS, the system with its inner voltage and current in Fig. II.3 is simulated under the change of load in both cases balanced and unbalance load using MATLAB/Simulink. The parameters of system and simulation are given in the Appendix A. The results of both cases are presented in the Following subsections:

II.9.1. Characteristics of the VSI-based SPSS under balanced loads

The simulation results of this test when the inverter is feeding the three loads are shown in Figs. II.10 to II.16. Figs. II.10 to II.13 show the steady and transient waveforms of inverter output currents and voltages in the abc reference frame, as well as their dq components. These results demonstrate that the inverter with its inner voltage and current controller, can track the change in load and provide good output voltage and current waveforms, as well as can perfectly reject the disturbance of load. Both output voltages and currents are sinusoidal and can track their references with a steady state tracking error near zero and with very fast dynamic responses under the change of three phase load. Also, we can observe that the inverter can increase its output current to track the change in load and meet its active and reactive power requirements as shown in Figs. II.15 and II.16.

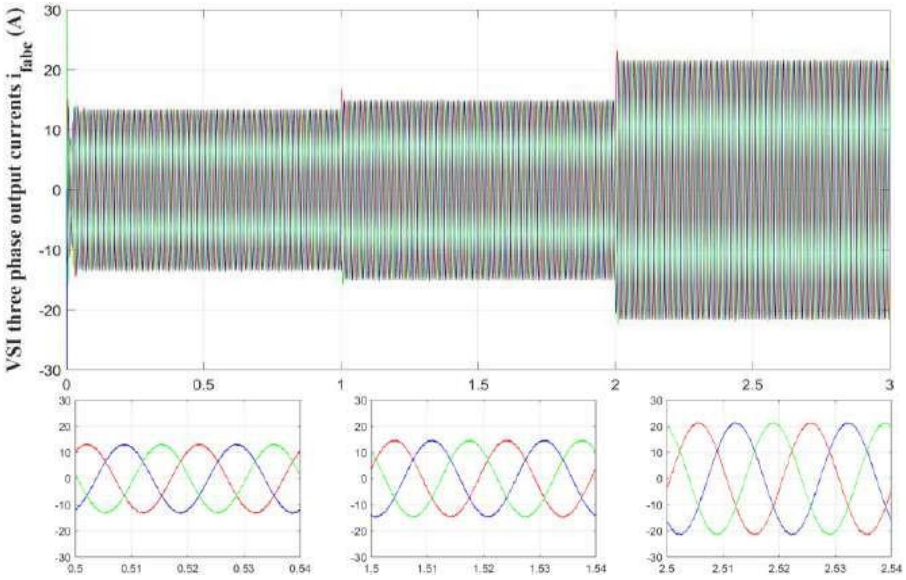


Figure II 11 Three phase VSI output currents

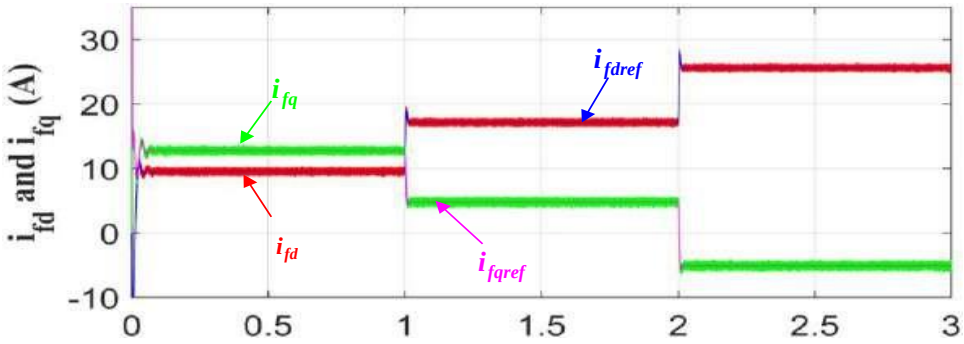


Figure II 12 VSI output currents in the dq reference frame.

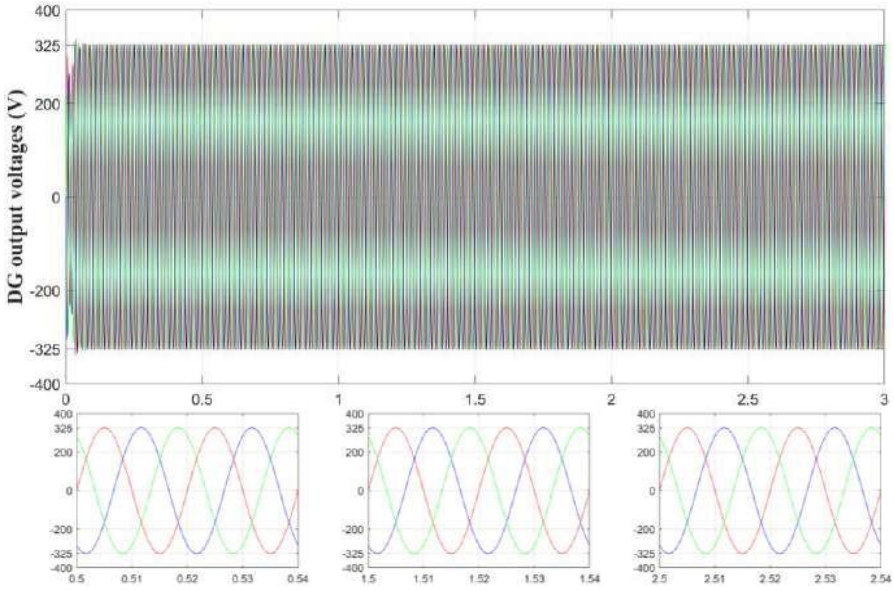


Figure II 13 Three phase VSI-based SPSS output voltages (capacitor voltages)

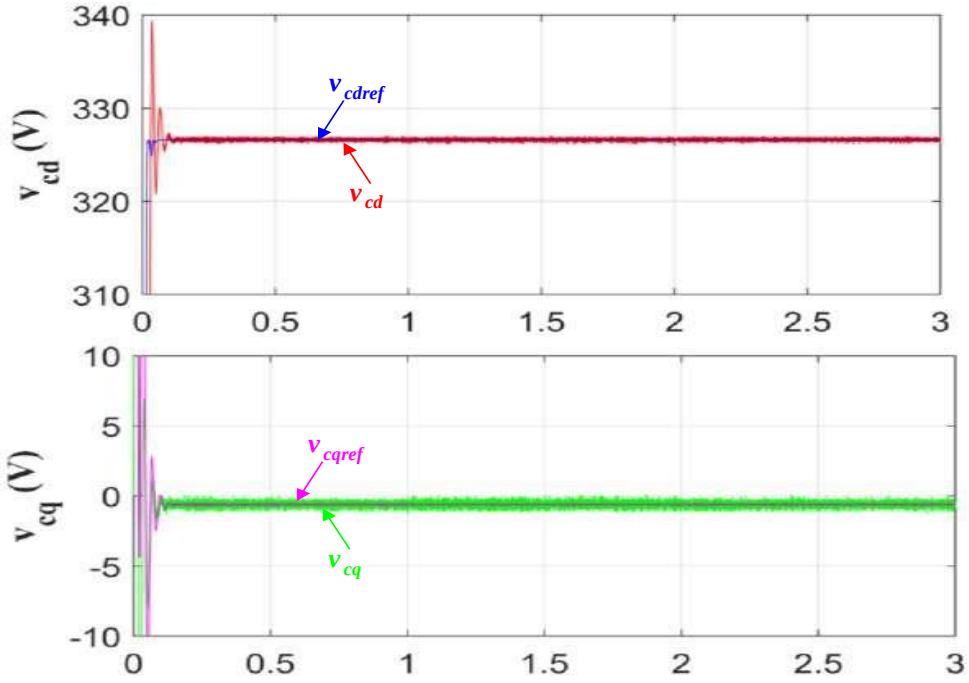


Figure II 14 Inverter output voltages in the dq reference frame

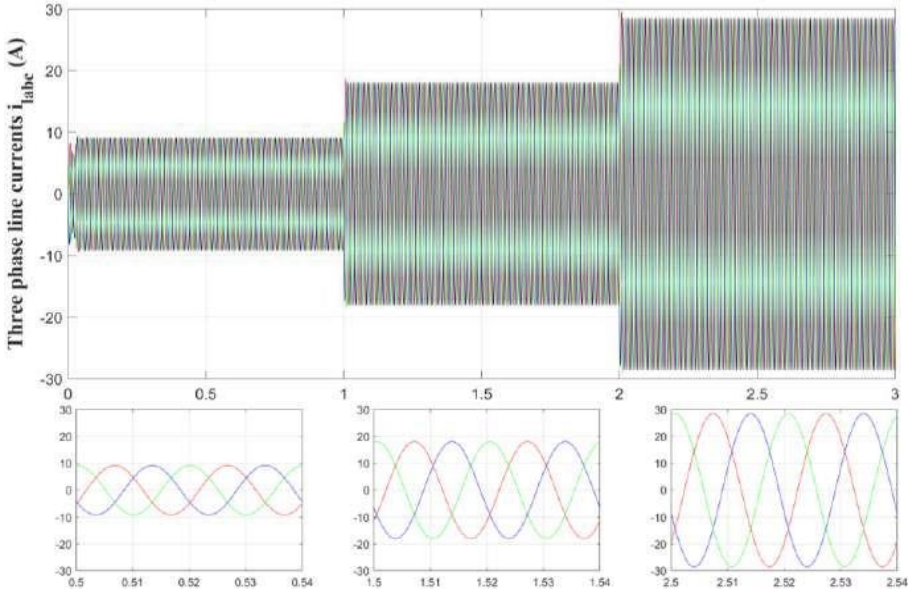


Figure II 15 Three phase load currents.

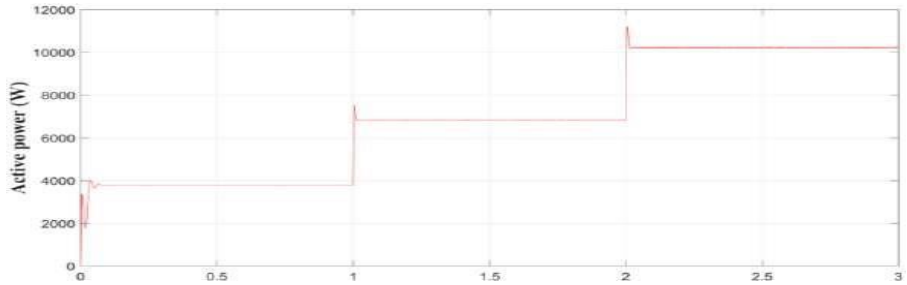


Figure II 16 Invaerter-based SPSS output active power

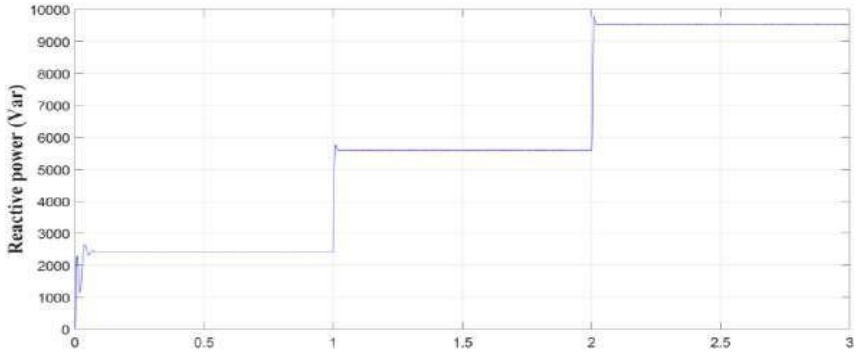


Figure II 17 Inverter-based SPSS output reactive power

Figure II.17 and Figure II.18 show the three phase SPSS voltages and its RMS value, respectively. Both figures demonstrated that the three phase SPSS voltages are sinusoidal under the three loads, with a decrease in its RMS voltage value under any change in load due to the increase in SPSS impedance drop voltage.

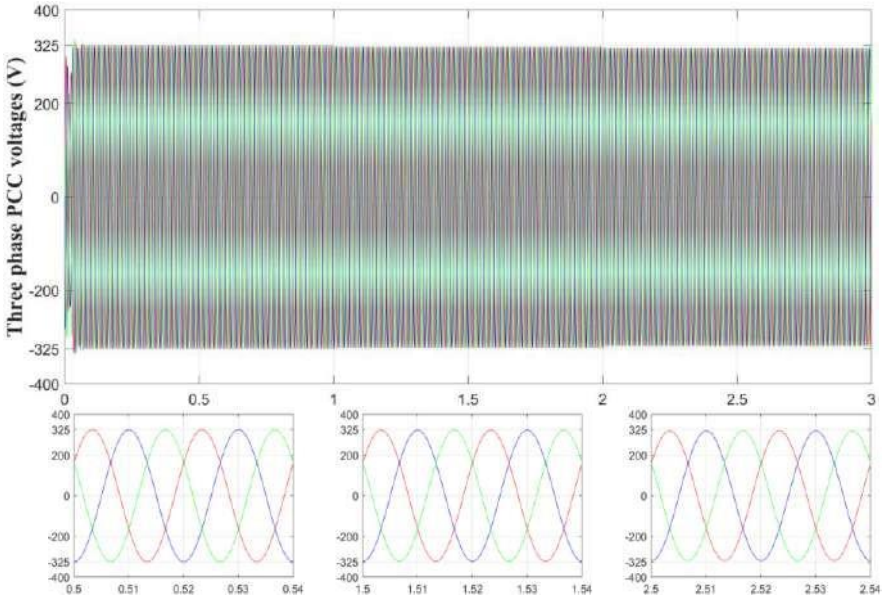


Figure II 18 Three phase SPSS voltages

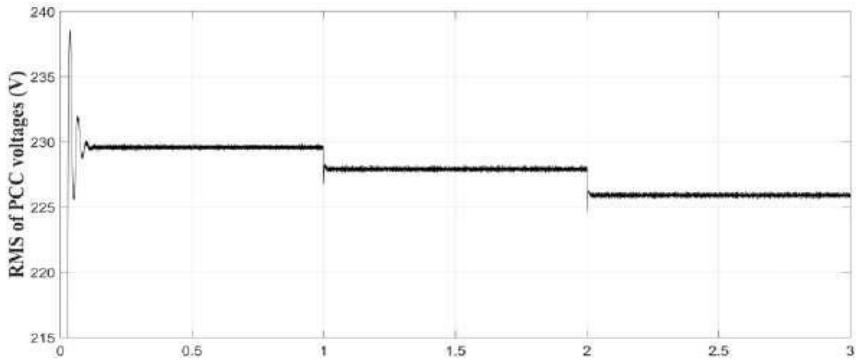


Figure II 19 RMS voltage of SPSS

II.10. Conclusions

In this chapter, a three-phase voltage source inverter with LC filter used as distributed generation unit in an SPSS is studied. In the first part of this chapter, the mathematical model of a VSI based SPSS including the dynamics of both VSI output current and capacitor voltages are presented in the three well knowing frames. The obtained dynamic models of the VSI output currents and capacitor voltages in the dq reference frame is used to develop the inner voltage and current controllers in the dq reference frame to control the output active and reactive powers and regulate the capacitor voltages of the VSI. For both the VSI output current control loop and the capacitor voltage control loop, PI controllers are used. In the second part of this chapter, the characteristics of the three phase VSI are tested and analyzed using the controllers that are designed before. The obtained simulation results show the good responses of the VSI in terms of output currents, capacitor voltages, line currents, active and reactive powers. Based on these, an SPSS with parallel VSIs is constructed in the next chapter, in which a circulating current elimination method combined with the inner voltage and current control loop is proposed in the control of the SPSS to improve the output current among the parallel VSIs.

Chapter III
Modeling and control of parallel VSI systems with elimination of the circulating current

III.1. Introduction:

In power applications requiring significant energy capacity, including distributed energy generation-based renewable energy sources, individual PWM inverters encounter restrictions related to power switch current limitations. These constraints impede the achievement of critical performance metrics including reliability, power capacity, and modular functionality. Parallel configuration of PWM inverters represents a viable solution that enables enhanced power capacity while addressing these inherent limitations. The implementation of parallel inverter topologies offers significant advantages over single inverter, including increased system capacity, reduced thermal stress on switching elements, mitigation of current rating constraints, and enhanced system stability, reliability, and modularity. However, major concerns associated with this topology include the presence of a circulating current (CC) that circulates between the phase legs of these inverters when the inverters operate under unbalanced current sharing or unbalanced output-filter parameters, which leads to multiple consequences, including output current distortion, power losses, and system stability degradation, as well as impacting the efficiency, reliability, and operational lifespan of the system. This work will focus on developing CC suppression method based on the adjustment of the voltage references of the PWM for parallel PWM inverters. The performance will be assessed through simulations.

III.3. Modeling of the paralleling of the two inverters

The schematic of the parallel connected three phase inverters is shown in Fig. III.1.

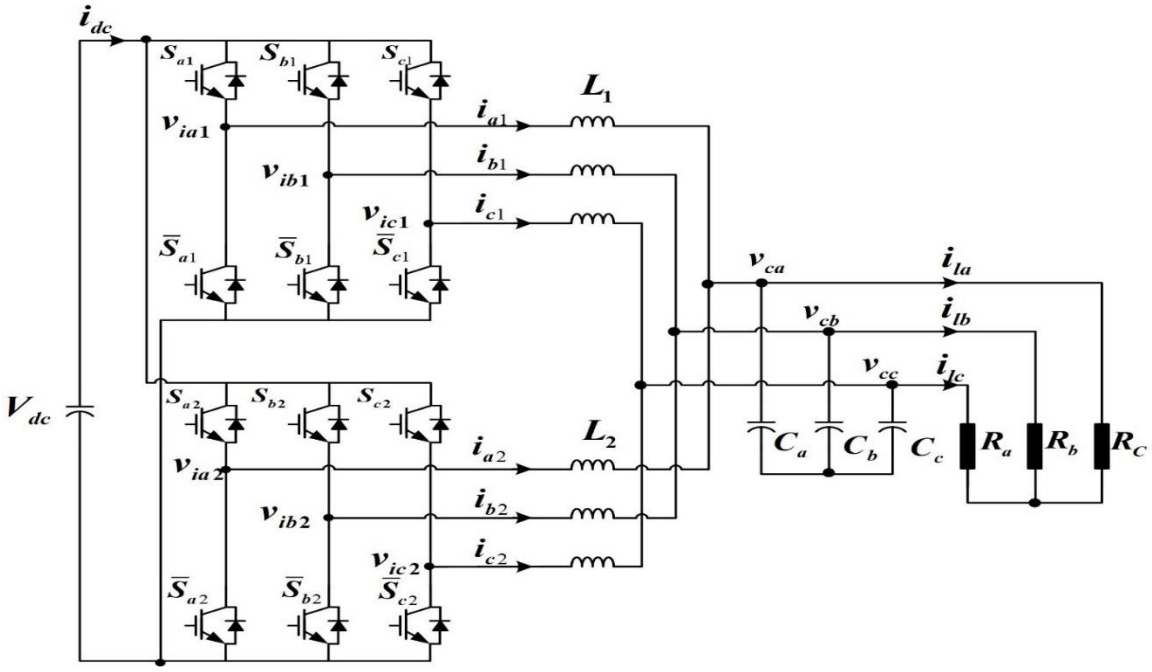


Figure III 1 Configuration of the parallel inverters in standalone mode

The diagram represents a parallel configuration of two three-phase Voltage Source Inverters (VSIs), in which both inverters are supplied by a common DC voltage source (V_{dc}). Each inverter consists of six IGBT switches arranged in a three-phase bridge, The output of each inverter is connected to the load through inductors L_{abc1} and L_{abc2}, which act as filters and limit circulating currents. The inverter outputs are combined at a common node before supplying the load. Capacitors (C_a, C_b, C_c) are placed at the output to smooth the voltage waveform and filter high-frequency harmonics The load is a balanced three-phase resistive load (R_a, R_b, R_c), Output voltages are labeled v_{ca}, v_{cb}, and v_{cc}, and load currents are i_{la}, i_{lb}, and i_{lc}. This system is suitable for grid-connected or standalone applications requiring high power and improved power qualiy.

III.8. Modeling of CC in paralleled three-phase two-PWM inverter

The parallel inverters topology in Fig. III.1 indicates that they have four circulating current (CC) tracks, which can be illustrated in Figs. III.2 (a), (b), (c), and (d).

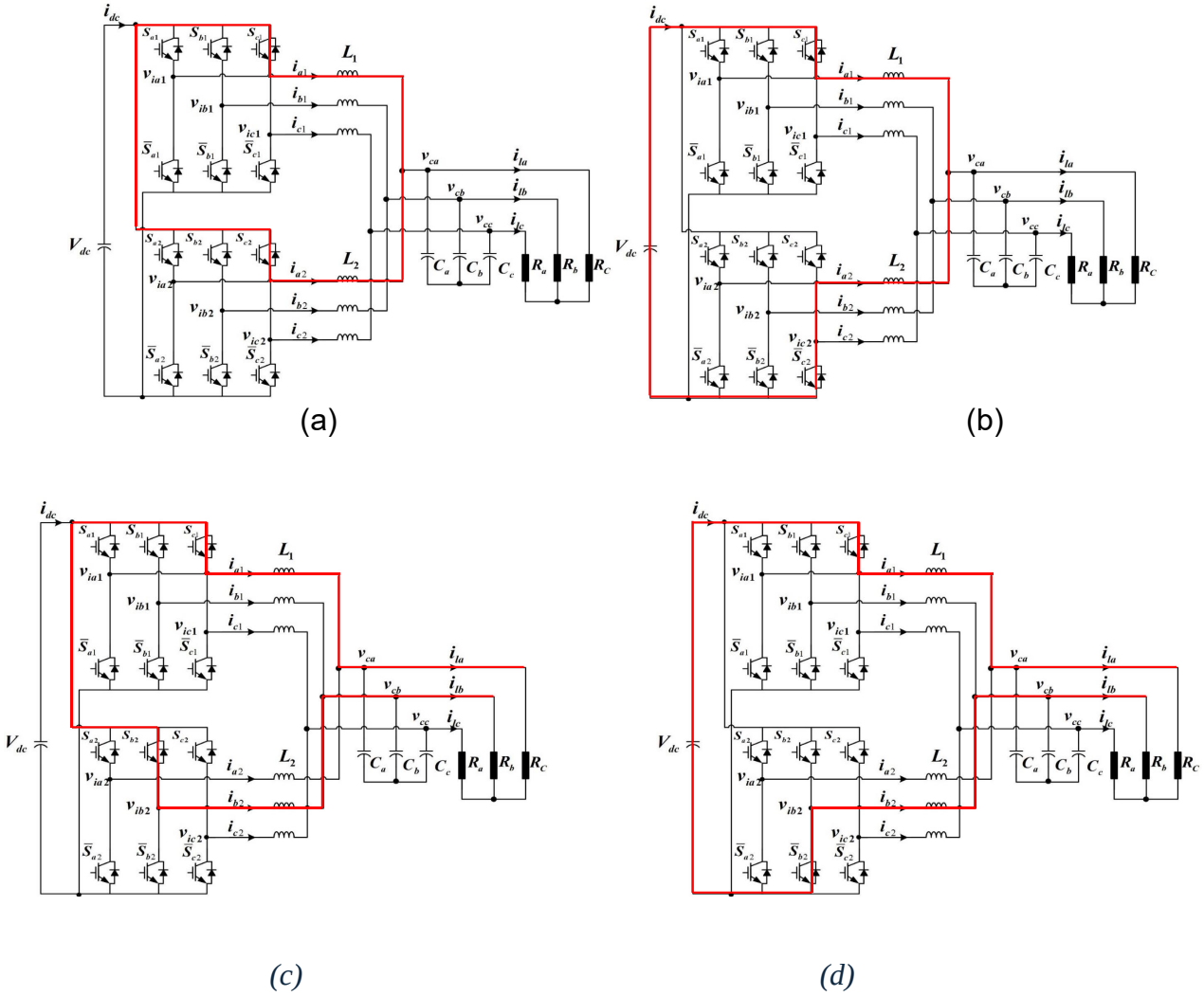


Figure III 2 Circulating current tracks parallel multi PWM rectifiers (a) do not pass by AC source, (b) pass only by DC-bus, (c) pass only by AC source, (d) pass both by AC source and DC-bus.

According to Figure III.2, the four CC tracks are divided into two CC types: the intra-phase CC type illustrated in Figure III.2 (a) and (b) and the inter-phase CC type illustrated in Figure III.2 (c) and (d). The intra-phase CC type (a and b) is CC and the tracks include the upper IGBTs of the same filter phase in different PWM rectifiers or lower IGBTs of the same filter phase in different PWM rectifiers, which is the focus of this work. The inter-phase CC is non CC, and the tracks include the two phase AC sources and the upper IGBTs of different phases in different PWM rectifiers or lower IGBTs of different phases in different PWM rectifiers.

III.4 Average equivalent circuit model of the two parallel in the 3-phase reference frame.

The average equivalent circuit model of the two parallel inverters in the 3-phase reference frame is shown in Fig. III.3.

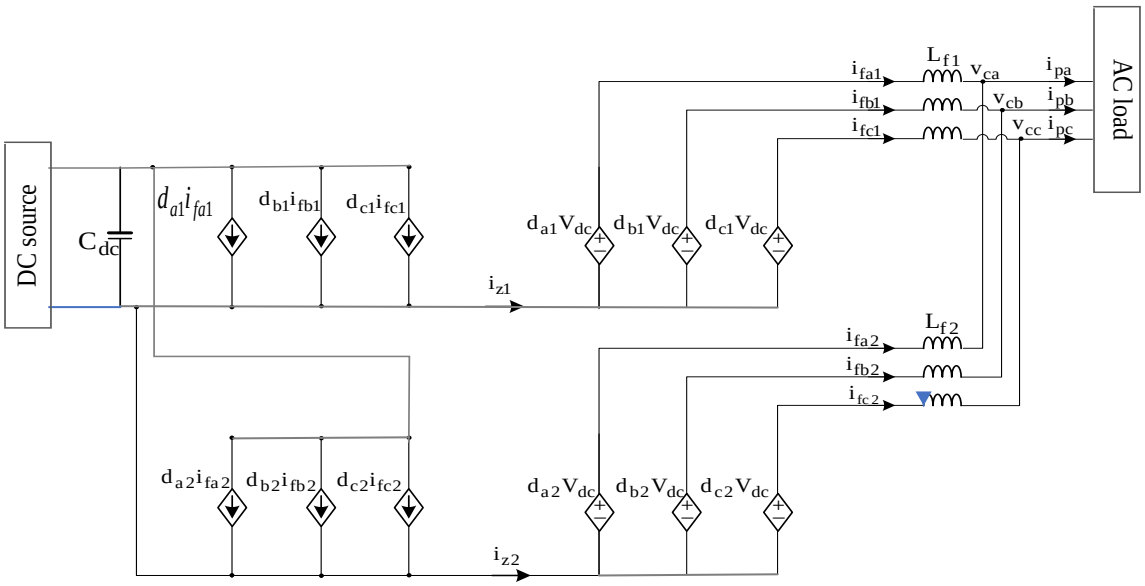


Figure III 3 Average equivalent circuit model of the two parallel inverters

By applying Kirchhoff's laws to the equivalent circuit model depicted in Figure **Error! No text of specified style in document.**-2, the mathematical model of the parallel system in the 3-phase reference frame can be obtained as follows:

$$\begin{cases} v_{ia1} = R_1 i_{a1} + L_1 \frac{di_{a1}}{dt} + v_{ca} \\ v_{ib1} = R_1 i_{b1} + L_1 \frac{di_{b1}}{dt} + v_{cb} \\ v_{ic1} = R_1 i_{c1} + L_1 \frac{di_{c1}}{dt} + v_{cc} \end{cases} \quad \text{(III.1)}$$

$$\begin{cases} v_{ia2} = R_2 i_{a2} + L_2 \frac{di_{a2}}{dt} + v_{ca} \\ v_{ib2} = R_2 i_{b2} + L_2 \frac{di_{b2}}{dt} + v_{cb} \\ v_{ic2} = R_2 i_{c2} + L_2 \frac{di_{c2}}{dt} + v_{cc} \end{cases} \quad \text{(III.2)}$$

From equation (III.1) and (III.2) we find the dynamics of both inverter's output currents as follows:

$$\begin{cases} L_1 \frac{di_{a1}}{dt} = v_{ia1} - R_1 i_{a1} - v_{ca} \\ L_1 \frac{di_{b1}}{dt} = v_{ib1} - R_1 i_{b1} - v_{cb} \\ L_1 \frac{di_{c1}}{dt} = v_{ic1} - R_1 i_{c1} - v_{cc} \end{cases} \quad \text{(III.3)}$$

$$\begin{cases} L_2 \frac{di_{a2}}{dt} = v_{ia2} - R_2 i_{a2} - v_{ca} \\ L_2 \frac{di_{b2}}{dt} = v_{ib2} - R_2 i_{b2} - v_{cb} \\ L_2 \frac{di_{c2}}{dt} = v_{ic2} - R_2 i_{c2} - v_{cc} \end{cases} \quad \text{(III.4)}$$

Additionally, the dynamics of the load or PCC voltages are given by:

$$\begin{cases} C \frac{dv_{ca}}{dt} = i_{ca} \\ C \frac{dv_{cb}}{dt} = i_{cb} \\ C \frac{dv_{cc}}{dt} = i_{cc} \end{cases} \quad \text{(III.5)}$$

Equations (III.3) - (III.4) - (III.5) demonstrate that the mathematical model of the two parallel connected inverter system in the 3phase reference frame is highly complex, which makes the analysis and control design highly complicated and difficult to implement. For simplicity, a low-complexity average model of this parallel system in the synchronous rotating reference frame (dq0 frame) is obtained as shown in Equations (III.6)-(III.7)- (III.8) based on Equations (III.3) - (III.4) - (III.5) using Park's transformation.

$$\begin{cases} L_1 \frac{di_{d1}}{dt} = v_{id1} - R_1 i_{d1} - v_{cd} + \omega L_1 \, i_{q1} \\ L_1 \frac{di_{q1}}{dt} = v_{iq1} - R_1 i_{q1} - v_{cq} - \omega L_1 \, i_{d1} \\ L_1 \frac{di_{01}}{dt} = v_{i01} - R_1 i_{01} - v_{c0} \end{cases} \quad \text{(III.6)}$$

$$\begin{cases} L_2 \dfrac{di_{d2}}{dt} = v_{id2} - R_2 i_{d2} - v_{cd} + \omega L_2 \, i_{q2} \\ L_2 \dfrac{di_{q2}}{dt} = v_{iq2} - R_2 i_{q2} - v_{cq} - \omega L_2 \, i_{d2} \\ L_2 \dfrac{di_{02}}{dt} = v_{i02} - R_2 i_{02} - v_{c0} \end{cases} \quad \text{(III. 7)}$$

$$\begin{cases} C \frac{dv_{cd}}{dt} = i_{cd} - \omega C \, v_{cq} \\ C \frac{dv_{cq}}{dt} = i_{cq} + \omega C \, v_{cd} \\ C \frac{dv_{c0}}{dt} = i_{c0} \end{cases} \quad \text{(III. 8)}$$

III.5. CC MECHANISMS AND CHARACTERISTICS

When inverters are connected in parallel through common AC and DC buses, a difference in the zero-sequence voltages between inverters is induced, which leads to the generation of CCs between these inverter phase legs. These CCs are complicated to model, analyze, and control. To facilitate the realization of these targets, the phase-leg average technique designed in [30] is adopted. The two parallel connected -leg inverter average phase-leg models obtained using this method are illustrated

in Fig III.2 Thus, the CCs of parallel modules could be derived. According to this figure, the CCs flowing between the two inverters have equal magnitudes and opposite phases, as shown in Equations (III.9) and (III.10):

$$\begin{cases} i_{z1} = i_{a1} + i_{b1} + i_{c1} \\ i_{z2} = i_{a2} + i_{b2} + i_{c2} \end{cases} \quad \text{(III. 9)}$$

$$i_z = i_{z1} = -i_{z2} \quad \text{(III. 10)}$$

Considering Fig III. 3, applying Kirchhoff's voltage laws results in:

$$\begin{cases} v_{z1} = \frac{v_{ia1}+v_{ib1}+v_{ic1}}{3} \\ v_{z2} = \frac{v_{ia2}+v_{ib2}+v_{ic2}}{3} \end{cases} \quad \text{(III.11)}$$

$$\begin{cases} v_{i1} = v_{l1} + v_{c1} \\ v_{i2} = v_{l2} + v_{c2} \end{cases} \quad \text{(III.12)}$$

$$\begin{cases} v_{l1} = L_1 \frac{di_1}{dt} \\ v_{l2} = L_1 \frac{di_1}{dt} \end{cases} \quad \text{(III.13)}$$

$$\Delta V = V_{l2} - V_{l1} = L_2 \frac{di_2}{dt} - L_1 \frac{di_1}{dt} \quad \text{(III.14)}$$

$$\begin{cases} v_{z1} = v_{la1} + v_{lb1} + v_{lc1} \\ v_{z2} = v_{la2} + v_{lb2} + v_{lc2} \end{cases} \quad \text{(III.15)}$$

$$\begin{cases} v_{z1} = L_{a1} \frac{di_{a1}}{dt} + L_{b1} \frac{di_{b1}}{dt} + L_{c1} \frac{di_{c1}}{dt} \\ v_{z2} = L_{a2} \frac{di_{a2}}{dt} + L_{b2} \frac{di_{b2}}{dt} + L_{c2} \frac{di_{c2}}{dt} \end{cases} \quad \text{(III.16)}$$

By summing the two equations of Equation (III.11), the following equation can be obtained:

$$\sum_{k=a,b,c} d_{k1}\, v_{dc} - L_1 \sum_{k=a,b,c} \frac{di_{k1}}{dt} = \sum_{k=a,b,c} d_{k2}\, v_{dc} - L_2 \sum_{k=a,b,c} \frac{di_{k2}}{dt} \quad \text{(III.17)}$$

The zero-sequence duty ratio of one PWM inverter can be defined as the total of the duty ratios of all phase legs of this inverter and can be expressed by Equation (III.18) in the two parallel inverters as follows:

$$\begin{aligned} d_{z1} &= \sum K = a,b,c\, d_{K1} = d_{a1} + d_{b1} + d_{c1} \\ d_{z2} &= \sum K = a,b,c\, d_{K2} = d_{a2} + d_{b2} + d_{c2} \end{aligned} \quad \text{(III.18)}$$

$$d_{z1} v_{dc} - L_1 \frac{di_{z1}}{dt} = d_{z2} v_{dc} - L_2 \frac{di_{z2}}{dt} \quad \text{(III.19)}$$

$$\begin{cases} v_{zsv1} = (d_{a1} + d_{b1} + d_{c1})\, v_{dc} \\ v_{zsv2} = (d_{a2} + d_{b2} + d_{c2})\, v_{dc} \end{cases} \quad \text{(III.20)}$$

$$(L_1 + L_2)\frac{di_z}{dt} = (d_{z2} - d_{z2})\ v_{dc} \quad \text{(III.21)}$$

$$(L_1 + L_2)\frac{di_z}{dt} = (v_{zsv2} - d_{zsv1}) \quad \text{(III.22)}$$

Usin Laplac, we have :

$$I_z = \frac{\Delta v_{zsv}}{(L_2+L_1)S+(R_2+R_1)} \quad \text{(III.23)}$$

III .6 CC Suppression

In this study, we use to methods for CC suppression, the first method is based on the modification of the inverters output voltage references to eliminate the difference between their zero sequence voltages. This is performed using the addition of voltage term that represent the difference between the zero sequence voltages to the output voltage references of only inverter, in which the add voltage term is generate from the regulation of the CC to zero using PI controller. While the second method is based on the regulation of the zero sequence current of each inverter to zero.

III .6.1. CC Suppression using the modified inverter output voltage references

According to the output current regulation of the single inverter in chapiter 2 (II.49), each inverter output voltage references are given by:

$$\begin{cases} v_{idx}^{*} = u_{ldx}^{*} + v_{cd} = (K_{pi} + \dfrac{k_{ii}}{s})(i_{dx}^{*} - i_{dx}) - \omega L_{1x} i_{qx} + v_{cd} \\ v_{iqx}^{*} = u_{lqx}^{*} + v_{cq} = (K_{pi} + \dfrac{k_{ii}}{s})(i_{qx}^{*} - i_{qx}) - \omega L_{x} i_{dx} + v_{cq} \end{cases} \quad \text{(III.24)}$$

In this method, the CC is eliminated using the modification of the output voltage references of only inverter. So, in this, we modified of the output voltage references of the second inverter and the new output voltage references that used in the PWM stage of the second inverter are given by:

$$\begin{cases} v_{ia2}^{*'} = v_{ia2}^{*} + v \\ v_{ib2}^{*'} = v_{ib2}^{*} + v \\ v_{ic2}^{*'} = v_{ic2}^{*} + v \end{cases}$$

where *v* is the add voltage term that obtianed from the regulation of the CC with zero using PI controller as follows:

$$v = (i_z^{*} - i_z)\left(k_{piz} + \frac{k_{iz}}{s}\right) \quad \text{(III.25)}$$

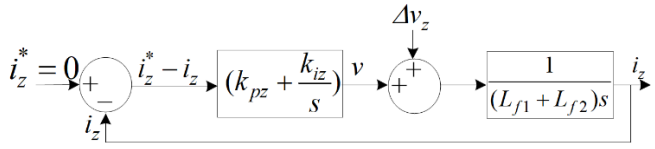


Figure III 4 Block diagram of the PI-based ZSCC regulation

where k_{pz} and k_{iz} are the proportional and integral the gains of the PI for the CC within the adjusted modulation voltages-based SPWM approach, which are expressed by:

$$\begin{cases} k_{pz} = (L_{f1} + L_{f2})\xi_z \omega_{cz} \\ k_{iz} = (L_{f1} + L_{f2})\omega_{cz}^2 \end{cases} \quad \text{(III.31)}$$

ω_{cz} and $\xi_z$are, respectively, the cut off frequency and the damping factor of the PI regulator for the ZSCC within the within the adjusted modulation voltages-based SPWM approach.

IV.6. Control of the parallel inverters using PI controllers based on the voltage reference modifications method for CC suppression

Figure III.5 illustrates a PI-based control architecture that achieves CC suppression by adjusting the voltage references of the parallel inverters. Each inverter is equipped with a current controller (typically in the ddd-qqq synchronous frame), and the voltage reference is updated based on the difference between measured and desired output currents.

This approach relies on direct CC mitigation, where improved current tracking indirectly reduces the generation of circulating currents. The scheme benefits from simplicity and ease of implementation, especially in systems already designed around PI control.

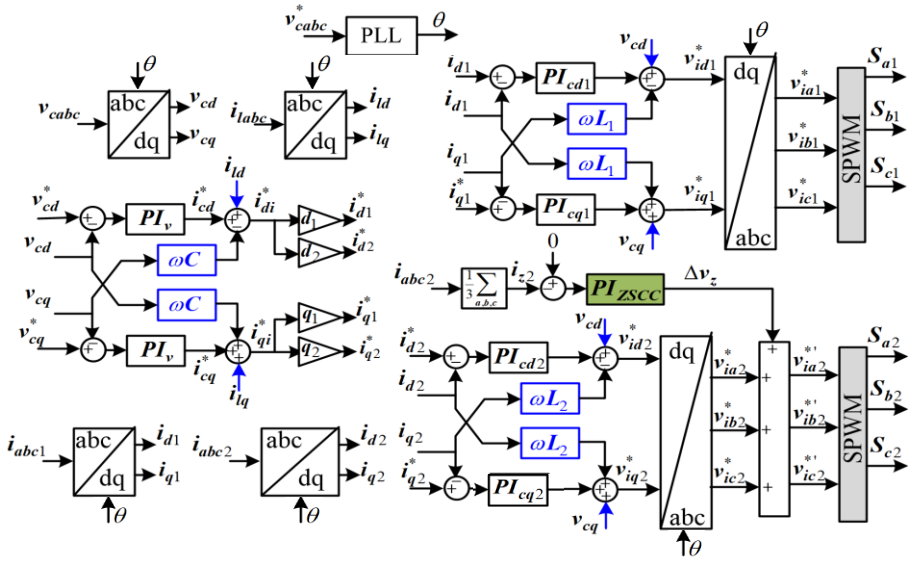


Figure III 5 Schematic diagram of the control of the parallel inverter adopting the CC suppression using the regulation of the CC

III.7. Simulation results of the parallel inverters

III.7.1. Under unbalanced output inverter's filter inductance values

Case 1: Simulation results of the parallel inverters without CC suppression

The simulation depicted in Figure 34 demonstrates a pronounced deterioration in current quality when no CC suppression is implemented. Significant circulating currents are observed, resulting from mismatched output filter inductances between the parallel inverters. This is evidenced by distorted current waveforms and elevated THD values (8.83% for Inverter 1 and 10.82% for Inverter 2). The harmonic spectrum reveals the dominance of low-order harmonics, severely degrading the system's power quality. These findings clearly demonstrate the sensitivity of parallel inverter systems to passive element asymmetry and underscore the necessity of incorporating explicit CC suppression mechanisms

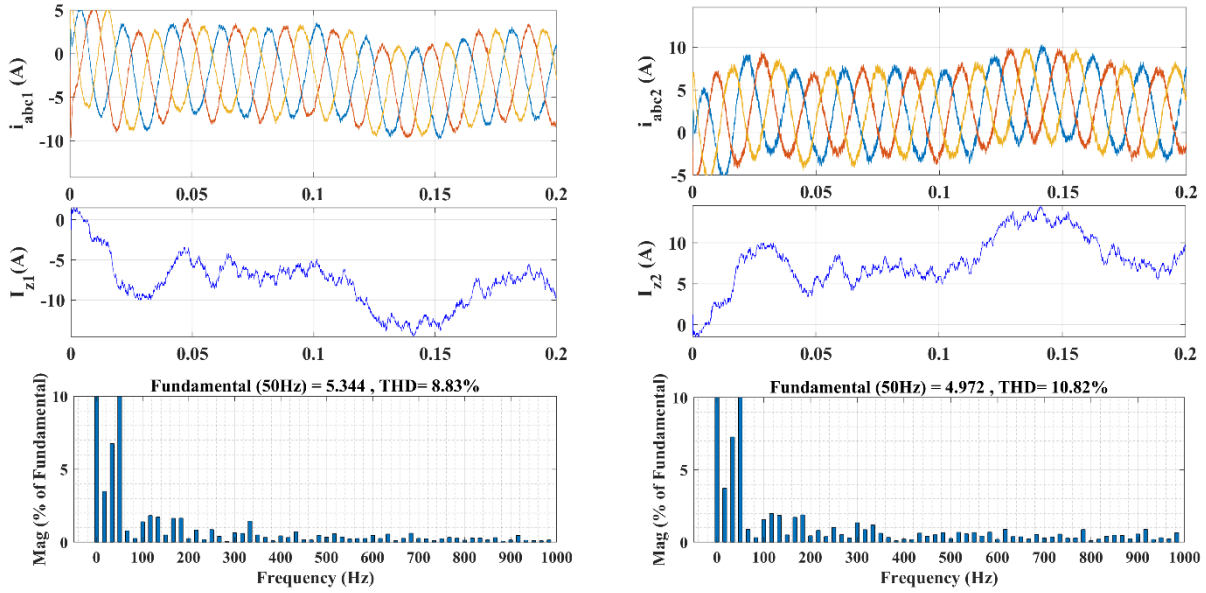


Figure III 6 Simulation results of the parallel inverters under mismatched output filter without CC control and suppression

Case 2: Simulation results of the parallel inverters with CC suppression using modification voltage references method

Figure III.6 shows the system response with PI-based CC suppression via voltage reference modification under the same unbalanced filter conditions. The control strategy significantly enhances current synchronization between the inverters. THD values drop to 4.12% and 4.43%, indicating effective harmonic reduction and improved waveform purity. Although the method does not explicitly regulate zero-sequence current, the indirect suppression achieved through coordinated voltage reference correction proves adequate under moderate mismatches, which reduce the CC to about 0.7 A. This validates the effectiveness of the proposed method in improving current sharing and maintaining power quality

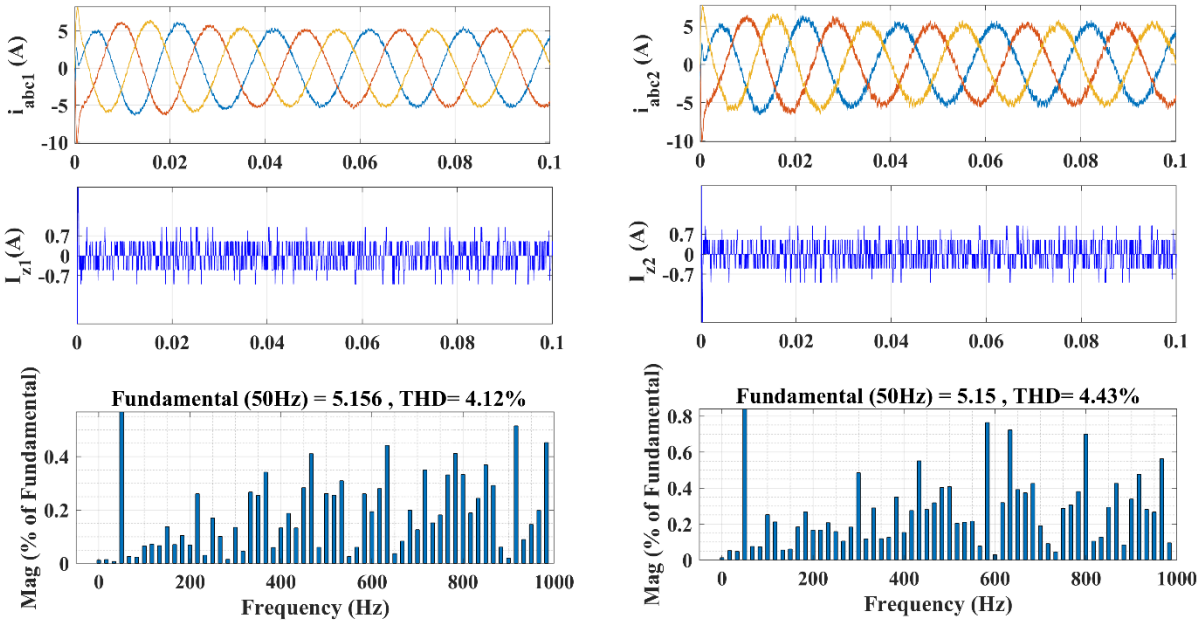


Figure III 7 Simulation results of the parallel inverters based on PI controllers under unbalanced output current with CC control and suppression

III.7.2. Under unbalanced parallel system output currents distributions

The simulation results of this case showing the output currents, CC, and THD of both parallel inverters are shown in Fig. III.7.

Case 1: Simulation results of the parallel inverters without CC suppression

In Figure 36, the inverters are subjected to unbalanced current demands without any form of CC suppression. The results exhibit substantial waveform distortion and uneven current distribution. Inverter 2 suffers a significantly higher THD (10.21%) compared to Inverter 1 (5.30%), indicating a clear imbalance. This condition can result in overheating, instability, and efficiency losses. The simulation highlights the system's vulnerability to dynamic mismatches and further justifies the necessity for a dedicated CC suppression mechanism, particularly under unbalanced parallel system output filter conditions.

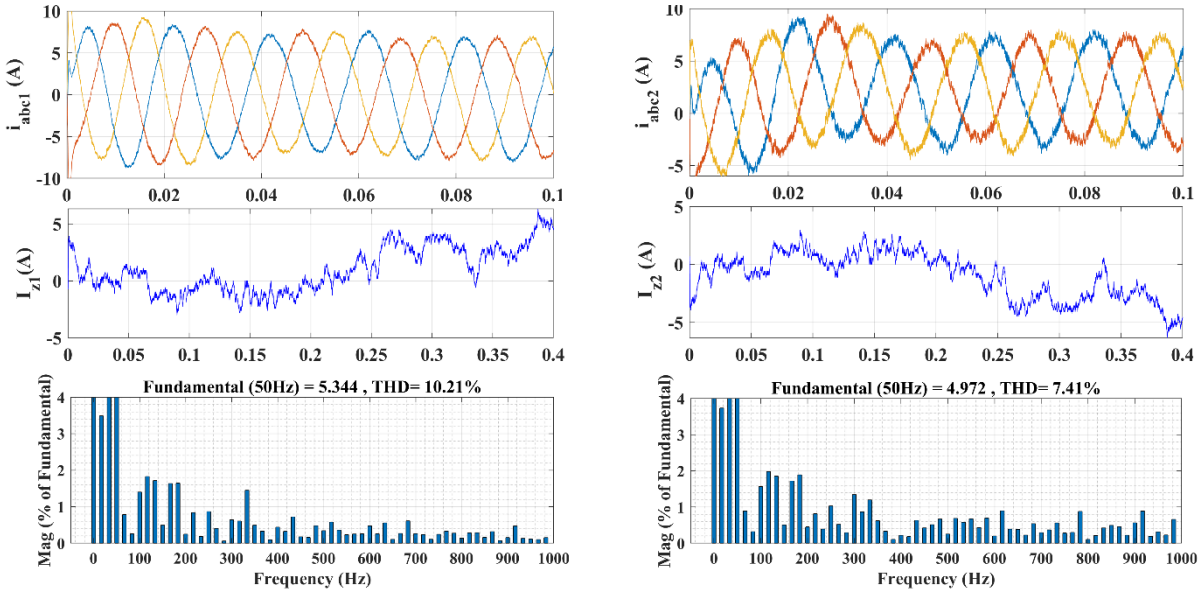


Figure III 8 Simulation results of the parallel inverters based on PI controllers under unbalanced output current without CC

control and suppression under unbalanced parallel system output currents distributions

Case 2: Simulation results of the parallel inverters with CC suppression using modification voltage references method

Figure III.8 illustrates the system behavior under unbalanced current sharing with the voltage reference modification method active. The control strategy leads to improved CC elimination and harmonic performance, reducing the CC to about 0.8A, and the THD values to 3.72% and 4.87%. The harmonic spectra show that higher-order harmonics are significantly suppressed, resulting in cleaner waveforms. Despite not fully eliminating performance asymmetry between the two inverters, the strategy demonstrates satisfactory disturbance rejection and robustness against current distribution mismatches.

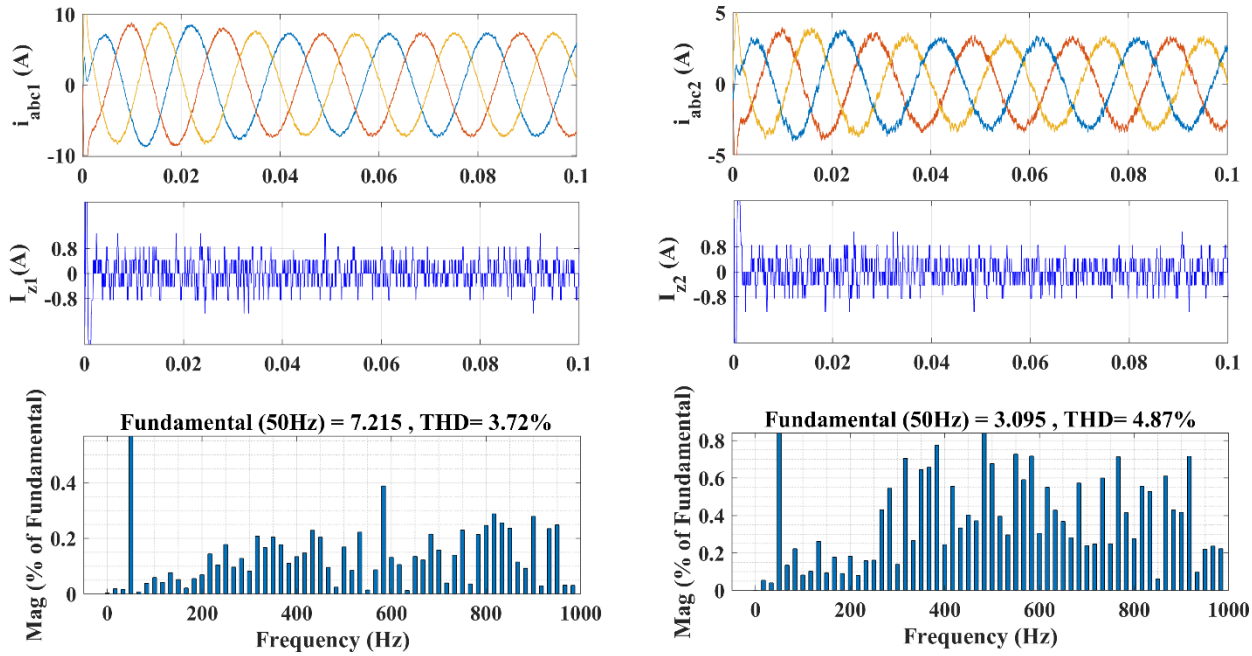


Figure III 9 Simulation results of the parallel inverters based on PI controllers under unbalanced output current with CC control and suppression using modification voltage references method under mismatched parallel inverter's output filter inductance values

IV.6. Control of the parallel inverters using PI controllers based on the ZSC regulation method for CC suppression

The control schematic shown in Figure III.9 integrates an explicit zero-sequence circulating current (ZSC) feedback loop within the PI control structure. This architecture directly targets CC suppression, making it more effective under severe mismatched conditions. The inclusion of ZSC sensing and regulation adds a robust layer of dynamic correction, ensuring both waveform symmetry and improved harmonic performance even under system disturbances

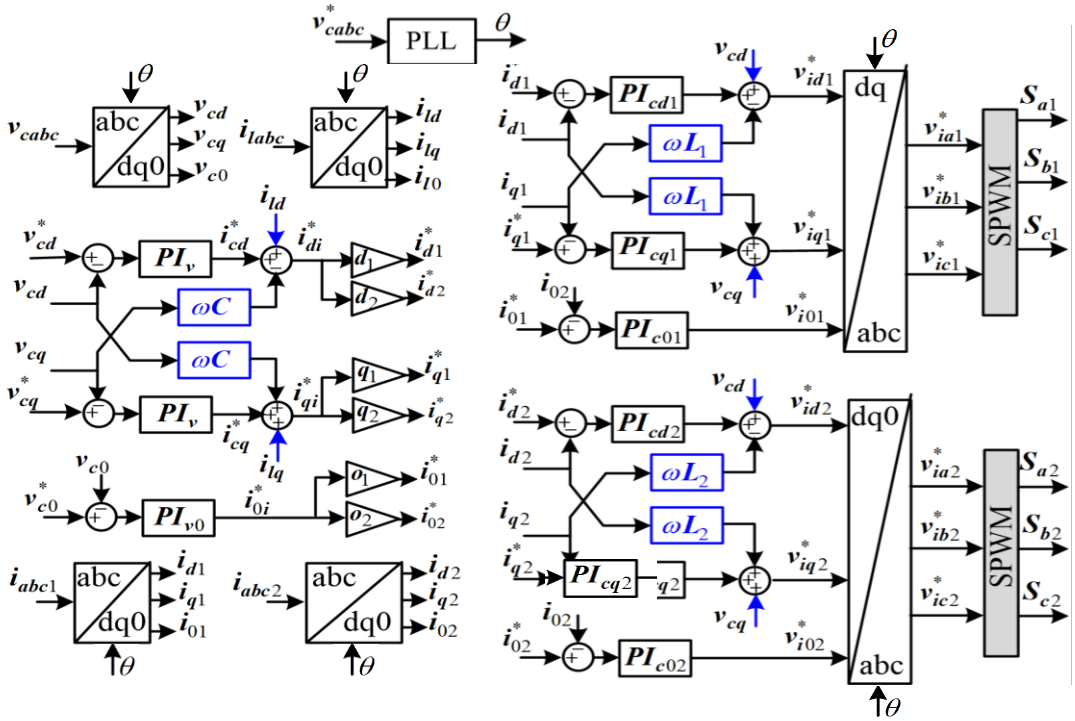


Figure III 10 Overall schematic diagram of the control of the parallel inverter using PI controllers adopting the on the ZSC regulation method for CC suppression

Simulation results

Case 1: Under unbalanced parallel system output filter inductance values

Simulation results in Figure III.11 illustrate the mixed performance of the ZSC regulation method under filter mismatch conditions. Inverter 1 maintains a low THD of 2.64% with a strong fundamental current (7.215 A), indicating excellent waveform fidelity. However, Inverter 2 experiences degradation, with higher THD (6.46%) and reduced fundamental amplitude (3.095 A). These findings suggest that while ZSC regulation improves CC suppression, the PI control structure may still lack the adaptability needed to fully equalize performance across both inverters when faced with significant passive mismatches.

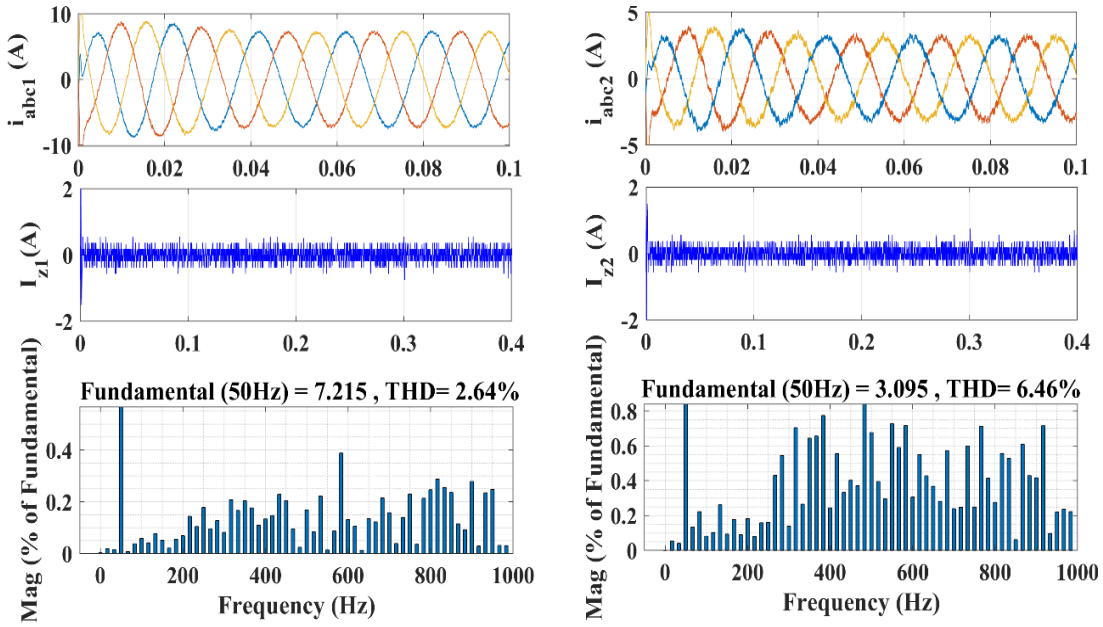


Figure III 11 Simulation results of the parallel inverters under unbalanced output current with CC control and suppression

Case. 2: Under unbalanced parallel system output currents distributions

The simulation results of this case showing the output currents, CC, and THD of both parallel inverters are shown in Fig. III.12.

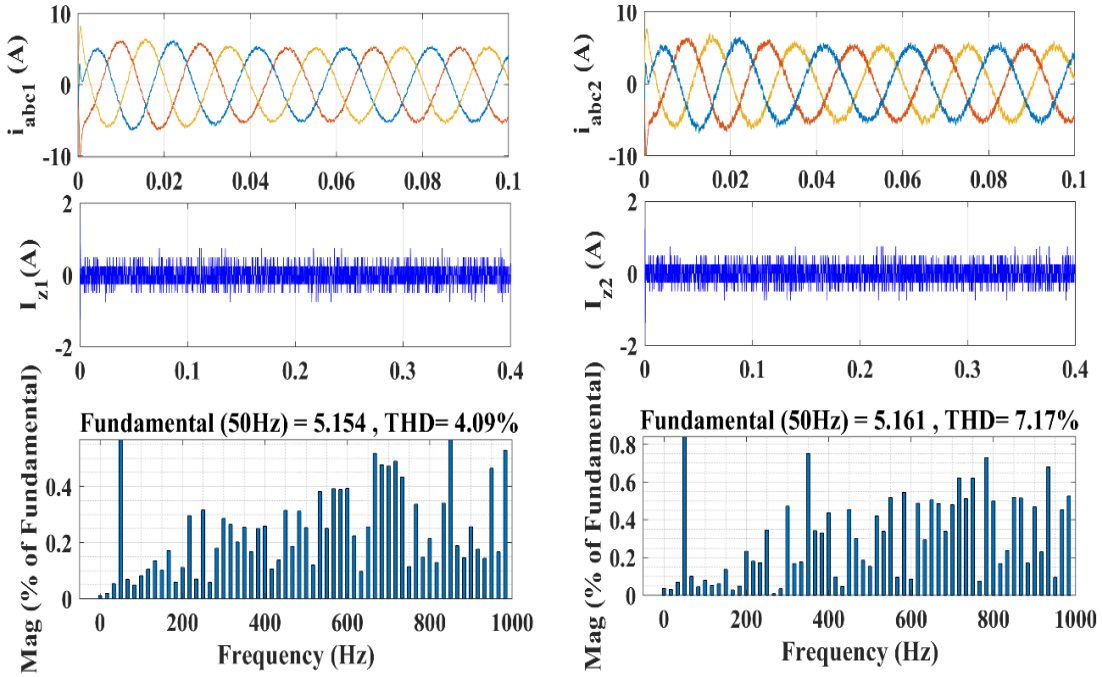


Figure III 12 Simulation results of the parallel inverters under mismatched output filter with CC control and suppression

Figure III.12 shows the system behavior under unbalanced current demands with active ZSC regulation. Both inverters produce nearly equal fundamental currents (~5.15 A), indicating good current sharing. However, THD remains unequal (4.09% for Inverter 1 vs. 7.17% for Inverter 2), with Inverter 2 exhibiting pronounced high-frequency harmonic content. This residual distortion highlights the limitations of PI controllers under dynamic conditions, suggesting the need for nonlinear or adaptive enhancement to fully exploit the benefits of ZSC regulation

III.9. Conclusion

This study presented a comprehensive investigation into the control and coordination of parallel inverter systems under unbalanced operating conditions, with a specific focus on mitigating circulating current (CC) and improving output power quality. Two main control strategies were explored and compared: voltage reference modification and zero-sequence current (ZSC) regulation.

Simulation results demonstrate that under unbalanced filter inductances and uneven load sharing, the lack of CC suppression leads to significant harmonic distortion, unbalanced current sharing, and degraded overall performance. The PI-based controllers, when combined with voltage reference modification, offer a degree of CC mitigation and THD reduction. However, their effectiveness remains limited in highly unbalanced scenarios due to their inherently linear nature and static gain design.

The incorporation of ZSC regulation into the PI framework improved current synchronization and harmonic performance by directly targeting the circulating current. Nevertheless, the results reveal residual asymmetry in inverter performance and limited dynamic adaptability, especially under high-frequency disturbances.

Chapter IV
Command by super twisting .

IV.1: Introduction:

Usually, nonlinear control techniques are applied in order to resolve some of conventional control problems such as parametric variations,and ensuring zero static error also guarantying a rapid response, therefore have a stable and robust control system. Among these nonlinear control techniques, sliding mode control (SMC) is known by its simplicity and robustness.

SMC, developed in the early 1950s by V. Utkin, has been recognized as an efficient tool for robust controllers design in complex high-order nonlinear dynamic plants operating under various uncertain conditions. SMC, based on the variable structure system control theory, provides means to overcome poor performance or instability problems and to guarantee robustness under parameter uncertainties resulted when PID controllers are used . SMC's major advantage is its low sensitivity to parameter variations and disturbances, which relaxes the necessity of the system's exact modeling [14].

In the first part of this chapter, the objective will not to deal in depth with sliding mode control technique, but rather to present a brief reminder on it then to apply it in the control of the parallel inverter system with both back-to-back and point-to-point structures. The point is to enhance the control of active and reactive powers as well as the DC voltage by using the merits of first order SMC approach. In the second part of this chapter, a special attention will be given to the control by super twisting algorithm. For this, a theoretical brief on the super twisting algorithm will be given, and eventually; this control will be applied to the aforementioned parallel inverter systems by replacing the classic SMC controllers by super twisting algorithm controllers.

IV.2.First Order Sliding Mode Control:

One specific method of working with systems that have changeable structures is the sliding mode control technique. According to a well-defined switching logic, a system with a changeable structure is one that can alter its structure by alternating between two states, as shown in figure IV.1.

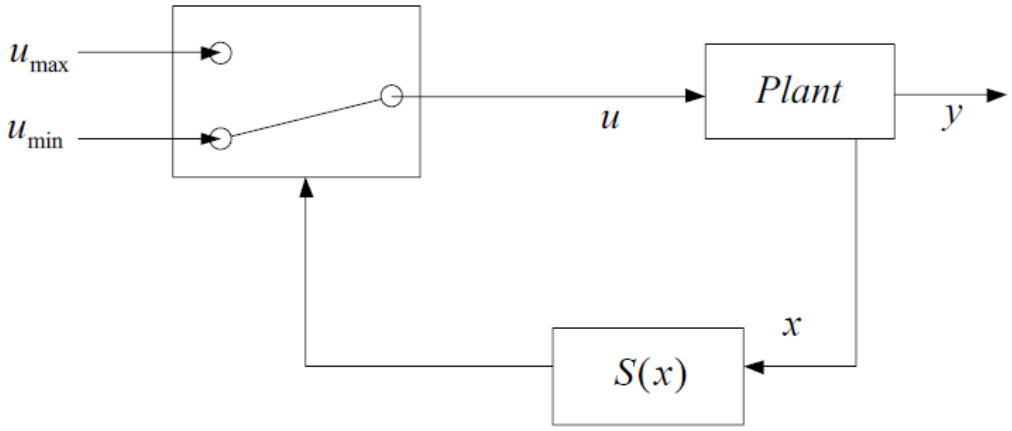


Figure IV 2 Variable structure regulation system with a change of structure by switching

The switching between two values is defined by the following law:

$$u = \begin{cases} u_{min} & for\ S(x) > 0 \\ u_{max} & for\ S(x) < 0 \end{cases} \qquad \text{(IV.1)}$$

A good characterization of the switching logic and a reasonable selection of each structure's characteristics are essential for systems with variable structures. The system is in sliding mode when switching occurs at a relatively high frequency under specific circumstances. S(x) = 0 defines the system's dynamic behavior; S(x) is the sliding surface. The goal is to move the system's state trajectory in the direction of this surface and keep the sliding regime going until the system reaches equilibrium [16].Robustness against parameter or disturbance changes is a major benefit of variable-structure control in sliding mode [16]. Other benefits of sliding mode control are its simplicity and ease of implementation. Because of these benefits, using this control is highly intriguing and ideal for grid-connected voltage source converters. Sliding mode control's "chattering" oscillation phenomenon, however, has a significant disadvantage in that it can excite high-frequency switching dynamics, which makes it undesirable as it frequently results in control inaccuracy and significant heat loss in electric circuitry [14].

Choosing the manifold in the state space that permits the trajectory of the system's state variables to converge towards the desired point of equilibrium is the first step in designing the control law in sliding mode. Next, the condition of the sliding mode's existence is established, which is connected to the convergence of the state trajectory, and the control laws that have the responsibility of preserving the sliding conditions (attractiveness) are determined. In other words, the process of conceptualizing the law of control by sliding mode is completed in three steps [16][14]:

Step 1: Choice of sliding surface.

Step 2: Development of the convergence condition.

Step 3: Determination of the control law.

IV.2.1 :Choice of Sliding Surface:

For a system defined by equation (IV.2), the vector of the surface *S*(*x*) has the same dimension as the command vector *u* .

$$\frac{dx}{dt} = f(x) + B(x)u \qquad \text{(IV.2)}$$

The sliding surface is a scalar function such that the variable to be adjusted slides on this surface and tends towards the origin of the phase plane [16]. A general form proposed by *J.J. Slotine* that ensure the convergence of the variable to settle towards its reference is given by :

$$S(x) = \left(\frac{d}{dt} + \lambda\right)^{r-1} e(x) \qquad \text{(IV.3)}$$

e(*x*) :Represents the difference between the variable to be regulated and its reference.

λ : is a positive constant.

r : is the relative degree of variable; it represents the number of times one takes to differentiate the output to bring up the control.

Maintaining the surface at zero is the control's goal. One way to think of the sliding surface is as a linear differential equation, with e(x) = 0. This comes down to a tracking the trajectory problem for an appropriate choice of controller gains, which is the same as an exact linearization of the difference while adhering to the convergence condition .

IV.2.2:Conditions of Existence and Convergence :

The system's dynamics can converge towards the sliding surface when the condition of convergence or attractiveness is met; this is accomplished by creating a scalar function of *Lyapunov* V (x) > 0 for the system's state variables. This function must be reduced by the control law. The answer is to create a command so that the square of the sliding surface corresponds to a *Lyapunov* function and to select a scalar function S(x) to ensure that the variable to be controlled is attracted to its reference value.

Lyapunov's function is defined as follows:

$$V(x) = \frac{1}{2}S^2(x) \qquad \text{(IV.4)}$$

The derivative of this function is:

$$\dot{V}(x) = S(x)\dot{S}(x) \qquad \text{(IV.5)}$$

The function V(x) can be forced by making sure that its derivative is negative. According to equation (IV.4), the square of the separation between a certain point on the phase plane and the sliding surface, represented by S 2 (x), continuously diminishes as long as The Lyapunov function's derivative is always negative, which forces the system's path to move from both sides in the direction of the surface. An ideal sliding regime with an infinite switching frequency is assumed by this condition .

IV.2.3:Determination of the Sliding Mode Control Law:

To achieve a sliding regime, a discontinuous control is necessary. A continuous component can be added to this discontinuous control if it is necessary [16]. The discontinuous control is used to confirm the attractiveness conditions when there is a disturbance. The sliding mode controller structure is composed of two sections: the stabilizing (u_{sw}) and the accurate linearization (u_{eq}) sections. It is determined by:

$$u = u_{eq} + u_{sw} \tag{IV.6}$$

The variable to be controlled on the sliding surface S(x) = 0 is maintained using the similar instruction put forward by Filipov and Utkin [16]. If this variable is not on the sliding surface, it is driven towards its reference using discontinuous control [53][12]. Verification of the convergence requirement is then established.

IV.2.3.1: Equivalent Control:

Consider the previous system (IV.2), an equivalent control vector can be developed by setting the derivative as a function of time of the switching function equal to zero:

$$S(x,t) = \left(\frac{\partial S}{\partial x}\right)(f(x,\dot{t}) + B(x,t) + \frac{\partial S}{\partial t} = 0 \tag{IV.7}$$

Hence, we can find the equivalent command defined by:

$$u_{eq} = -\left[\left(\frac{\partial S}{\partial x}\right)^t B(x,t)\right]^{-1}\left\{\left(\frac{\partial S}{\partial x}\right)^t f(x,t) + \frac{\partial S}{\partial t}\right\} \tag{IV.8}$$

With the condition of existence:

$$\left[\left(\frac{\partial S}{\partial x}\right)^t B(x,t)\right] \neq 0 \tag{IV.9}$$

IV.2.3.2: Discontinuous Control :

A control that can bring these trajectories closer to its references is required when the state trajectories are not on the sliding surface S(x) = 0 because of disruptions or modifications in the system parameters. This condition can be met by a discontinuous function (two-level switch), which is defined by:

$$u_{sw} = -k\,sgn(S(x)) \qquad with\ k > 0 \tag{IV.10}$$

With :

$$sgn(S(x)) = \begin{cases} 1 & S(x) > 0 \\ -1 & S(x) < 0 \\ 0 & S(x) = 0 \end{cases} \tag{IV.11}$$

IV.2.4:Integral Slide Mode Control :

In this approach, the sliding surface can be improved by inserting an integral action in its expression,

this surface is then defined by [16]:

$$S(t) = \left(\lambda + \frac{d}{dt}\right)^{r-1} e(x) + k_i \int e(t)dt \qquad \text{(IV.12)}$$

where k_i is a positive integral gain.

This method has the benefit of using a plane that passes through the origin as the sliding surface. When the system is second order, r = 2, the solution is found on a plane, however in the classic sliding mode, the solution is found on a line [16][12].

IV.3.2 Second-Order Sliding Mode Control:

A promising method for handling the chattering issue while retaining the primary benefits of the traditional SMC in terms of resilience, order reduction, simplicity, and ease of implementation is higher-order sliding modes (HOSM).. Furthermore, in the presence of switching delays and measurement noise, it is claimed that the practical application of HOSM yields a greater accuracy than the standard SMC . A continuation of the conventional sliding mode theory is HOSM. In this context, first-order sliding mode control (1-SMC) is typically used to refer to the classical SMC that was previously presented. The 1-SMC is restricted to situations where the sliding variable and the relative degree inside the system must be one, which may restrict the sliding variable's selection . This is another reason for the development of this approach. Prior to applying the actual control signal, integrators are added to the input channel with the primary goal of increasing the order of the controlled system. As a result, unlike in 1-SMC, the discontinuous control component affects the sliding variable's higher-order time derivative rather than its first-time derivative. To put it another way, this new approach can much lessen the chattering effect because the higher derivative of the sliding variable actually contains the discontinuous control action . HOSM can be achieved using a variety of algorithms. To zero the outputs with relative degree two or to prevent chattering when zeroing the outputs with relative degree one, the second order sliding mode controllers (2-SMC) are specifically used. The sub-optimal controller, terminal sliding mode controllers, twisting controllers, and super-twisting controllers are examples of second-order algorithms. Specifically, the method for twisting forces the S(x) knowledge is necessary to slide a variable of relative degree two into the 2-sliding set. Although the sliding variable has relative degree one, the super-twisting algorithm does not require that. Because it gets rid of chattering, the super-twisting algorithm is currently preferred over the traditional siding method. This section presents a brief review on the super-twisting algorithm, which has been successfully implemented to solve the chattering problems.

IV.4.Basic Concepts Second-Order Sliding Mode Control:

IV.4.1Super Twisting Algorithm:

Considering an uncertain nonlinear system whose dynamics is described by:

$$\begin{cases} x^n = f(x) + g(x)u \\ S = S(x) \end{cases} \quad \text{(IV.30)}$$

where S is the sliding variable, f (x) and g(x) are some smooth and uncertain vector functions, t is the time, $u \in R$ is the control input, and $x \in R^n$ is the state vector. In order to guarantee convergence in an unlimited amount of time, the sliding surface is built with a relative degree r with regard to the control variable u, and it is defined to satisfy the necessary control parameters. Driving the intended sliding variable S to zero in a finite amount of time is the control goal in 1-SMC. In contrast, 2-SMC requires that the sliding variable S and its derivative $\dot{S}$ be driven to zero in a finite amount of time. The second derivative of the sliding variable $\ddot{S}$ is subjected to a discontinuous control action in order to accomplish this . This technique, despite being a 2-SMC, was first created for systems with relative degree one in order to circumvent the chattering issue associated with the use of 1-SMC. That is, only when the system's relative degree is one can this technique drive the sliding variable and its derivative to zero in finite time. The sliding mode control's control signal is typically divided into two sections: one that relates to the equivalent control, which handles the system's and the sliding surface's dynamics, and another that relates to the switching control, which is in charge of preserving the system's dynamics on the sliding surface.

Defining the sliding surface as:

$$S(x) = e \quad \text{(IV.31)}$$

where *e* is the tracking error defined as follows:

$$e = x - x_{ref} \quad \text{(IV.32)}$$

where x_{ref} is the desired trajectory, and *x* is the actual trajectory.

The sliding mode control is given:

$$u = u_{eq} + u_{sw} \quad \text{(IV.33)}$$

where u_{eq} is the equivalent control proposed by *Filipov* without regarding the system uncertainty and external disturbance. It serves to keep the variable to control on the sliding surfaces. The equivalent control is derived by considering that the derivative of the surface is null $S(x) = 0$. u_{sw} is the discrete control, which ensures convergence such that $\dot{S}S > 0$.

In Super-Twisting sliding mode control, switching control is usually adopted as:

$$\begin{aligned} u_{sw} &= -\lambda |S|^{\frac{1}{2}} sign(S) + u_1 \\ \dot{u} &= -\alpha sign(S) \end{aligned} \quad \text{(IV.34)}$$

Therefore, the time derivative of the sliding surface *S(x)* is:

$$\dot{S}(x) = \dot{e} = \dot{x} - \dot{x}_{ref} \quad \text{(IV.35)}$$

Equation (IV.13) can be rewritten:

$$u_{eq} = \frac{-f(x)+\dot{x}_{ref}}{g(x)} \quad \text{(IV.36)}$$

The switching control law is designed based on the Super-Twisting algorithm, the algorithm is as follow:

$$u_{sw} = -\lambda|S|^{\frac{1}{2}}sign(S) - \int \alpha sign(S)\, dt \quad \text{(IV.37)}$$

where α and λ are positive constants.

The final control law can be obtained as follows:

$$u = \frac{-f(x)+\dot{x}_{ref}}{g(x)} - \lambda|S|^{\frac{1}{2}}sign(S) - \int \alpha sign(S)\, dt \quad \text{(IV.38)}$$

IV.4.2 Stability Analysis :

In order to achieve an explicit relation for the controller design parameters, the work published in proposes quadratic like Lyapunov functions for the super-twisting controller. We shall return this analysis in the lines that follow.

$$\dot{S} = \Psi(S) + u \quad \text{(IV.39)}$$

WhereΨ (S) is an unknown bounded perturbation term and globally bounded by:
$|\Psi(S)| \leq \delta|S|^{\frac{1}{2}}$ for some constant $\delta > 0$. The super-twisting sliding mode controller for perturbation and chattering elimination is given by:

$$\begin{aligned} u_{sw} &= -\lambda|S|^{\frac{1}{2}}sign(S) + u_1 \\ \dot{u}_1 &= -\alpha sign(S) \end{aligned} \quad \text{(IV.40)}$$

System (IV.22) closed by control (IV.23) results in:

$$\begin{aligned} \dot{S} &= -\lambda|S|^{\frac{1}{2}}sign(S) + u_1 + \Psi(S) \\ \dot{u}_1 &= -\alpha sign(S) \end{aligned} \quad \text{(IV.41)}$$

Proposing the following candidate *Lyapunov* function:

$$V = 2\alpha|S| + \frac{1}{2}u_1^2 + \frac{1}{2}\left(\lambda|S|^{\frac{1}{2}}sign(S) - u_1\right) = \xi^T P \xi \quad \text{(IV.42)}$$

Where

$$\xi^T = \left(|S|^{\frac{1}{2}}sign(S), u_1\right) \quad \text{(IV.43)}$$

$$P = \frac{1}{2}\begin{pmatrix} 4\alpha + \lambda^2 & -\lambda \\ -\lambda & 2 \end{pmatrix} \quad \text{(IV.44)}$$

The time derivative of (IV.25) is:

$$\frac{dV}{dt} = \frac{d}{dt}(\xi^T P \xi) = \dot{\xi}^T P \xi + \xi^T P \dot{\xi} \quad \text{(IV.45)}$$

Equation (IV.28) can be rewritten in the following form:

$$\dot{V} = -\frac{1}{\left|S^{1/2}\right|}\xi^T Q \xi + \frac{\Psi(S)}{\left|S^{1/2}\right|}q^T \xi \quad \text{(IV.46)}$$

Where:

$$Q = \frac{\lambda}{2}\begin{pmatrix} 2\alpha + \lambda^2 & -\lambda \\ -\lambda & 1 \end{pmatrix} \quad \text{(IV.47)}$$

$$q^T = \begin{pmatrix} 2\alpha + \frac{1}{2}\lambda^2 & -\frac{1}{2}\lambda \end{pmatrix} \quad \text{(IV.48)}$$

Applying the bounds for the perturbations as given in [31][32], the expression for the derivative of the Lyapunov function is reduced to

$$\dot{V} = -\frac{1}{2\left|s^{1/2}\right|}\xi^T \hat{Q}\xi \quad \text{(IV.49)}$$

Where:

$$\hat{Q} = \begin{pmatrix} 2\alpha + \lambda^2 - \left(\frac{4\alpha}{\lambda} + \lambda\right)\delta & -\lambda + 2\delta \\ -\lambda + 2\delta & 1 \end{pmatrix} \quad \text{(IV.50)}$$

$\dot{V}$ is negative if $\hat{Q} \geq 0$, which is valid if the controller gains α and λ satisfy the following conditions:

$$\lambda > 2\delta, \ and \ \alpha > \lambda\frac{5\lambda\delta + 4\delta^2}{2(\lambda - 2\delta)} \quad \text{(IV.51)}$$

IV.3. Super Twisting Control of a Parallel Inverter Systems

After having presented a brief introduction to the super twisting control, in the following sections, we will apply this technique to control the parallel inverter's output currents, aiming to improve their quality and CC elimination.

IV.3.1 Controllers Design

The overall model of the parallel inverter system in the synchronous reference frame (dq) is given by:

$$\begin{cases} \frac{di_{dx}}{dt} = \frac{-R_x}{L_x} i_{dx} + \omega \ \ i_{qx} - \frac{v_{idx}}{L_x} + \frac{v_{cd}}{L_x} \\ \frac{di_{qx}}{dt} = \frac{-R_x}{L_x} i_{qx} + \omega \ \ i_{dx} - \frac{v_{iqx}}{L_x} + \frac{v_{cqx}}{L_x} \\ \frac{di_{0x}}{dt} = \frac{-R_x}{L_x} i_{0x} - \frac{v_{i0x}}{L_x} + \frac{v_{c0x}}{L_x} \end{cases} \quad \text{(IV.13)}$$

To apply the super twisting control on the parallel inverter output currents, the system (III.12) should be subdivided into two subsystems as follows:

Subsystem 1

The first subsystem is characterized by the state vector $x = \begin{bmatrix} i_{dx} & i_{qx} \end{bmatrix}^T$, and the control vector $u = \begin{bmatrix} v_{idx}^* & v_{iqx}^* \end{bmatrix}^{\mathrm{T}}$, and it is defined by:

$$\begin{cases} \frac{di_{dx}}{dt} = \frac{-R_x}{L_x} i_{dx} + \omega \ \ i_{qx} - \frac{v_{idx}}{L_x} + \frac{v_{cd}}{L_x} \\ \frac{di_{qx}}{dt} = \frac{-R_x}{L_x} i_{qx} + \omega \ \ i_{dx} - \frac{v_{iqx}}{L_x} + \frac{v_{cqx}}{L_x} \end{cases} \quad \text{(IV.14)}$$

Subsystem 2: The second subsystem it is characterized by the state vector $x = i_{0x}$, and the control

vector $u = v_{i0x}^{*}$. It is governed by:

$$\frac{di_{0x}}{dt} = \frac{-R_x}{L_x} i_{0x} - \frac{v_{i0x}}{L_x} + \frac{v_{c0x}}{L_x} \quad \text{(IV.15)}$$

After dividing overall system in two subsystems, the design of inverter's output current's controllers requires to apply to each of these sub-models the super twisting control.

IV.3.1.1 Current Controller Design

From the model of the first subsystem, we define the following two surfaces: The first surface is that of the active component of the inverter's output current i_{dx} defined by:

$$S_{dx} = i_{dx} - i_{dx}^{*} \quad \text{(IV.16)}$$

The second surface is that of the reactive component of the alternating current i_{qx} defined by:

$$S_{qx} = i_{qx} - i_{qx}^{*} \quad \text{(IV.17)}$$

IV.3.1.2 Equivalent Control Design:

During the sliding mode, we have:

$$\begin{aligned} S_{dx} &= \dot{S}_{dx} = 0 \\ S_{qx} &= \dot{S}_{qx} = 0 \end{aligned} \quad \text{(IV.18)}$$

Using the two equations of the first subsystem, the two sliding surfaces derivatives take the following form:

$$\begin{aligned} \dot{S}_{dx} &= f_{dx}(x) + g_{dx} u_{eqdx} - \dot{i_{dx}^{*}} = 0 \\ \dot{S}_{qx} &= f_{dx}(x) + g_{qx} u_{eqqx} - \dot{i_{qx}^{*}} = 0 \end{aligned} \quad \text{(IV.19)}$$

with

$$f_x = \begin{bmatrix} f_{dx} \\ f_{qx} \end{bmatrix} = \begin{bmatrix} -\frac{R_x}{L_x} i_{dx} + \omega & i_{qx} & -\frac{v_{cd}}{L_x} \\ -\frac{R_x}{L_x} i_{qx} + \omega & i_{dx} & -\frac{v_{cq}}{L_x} \end{bmatrix}; \; g_x(x) = \begin{bmatrix} g_{dx} \\ g_{qx} \end{bmatrix} = \begin{bmatrix} -\frac{1}{L_x} & 0 \\ 0 & -\frac{1}{L_x} \end{bmatrix} \quad \text{(IV.20)}$$

From equation (III.18), the equivalent control law can be defined by:

$$u_{eqdx} = \frac{\dot{i_{dx}^{*}} - f_{dx}(x)}{g_{dx}} \quad \text{(IV.21)}$$

$$u_{eqqx} = \frac{\dot{i_{qx}^{*}} - f_{qx}(x)}{g_{qx}} \quad \text{(IV.21)}$$

IV.3.1.3 Discontinuous Control Design:

In the case where the state trajectory is different from the sliding surface, the discontinuous control ensures the reduction of the distance between the state trajectory and its sliding surface. The discontinuous control laws are defined as:

$$u_{swdx} = -\lambda |S_{dx}|^{\frac{1}{2}} sign(S_{dx}) - \alpha sign(S_{dx}) \quad \text{(IV.22)}$$

$$u_{swdx} = -\lambda |S_{dx}|^{\frac{1}{2}} sign(S_{dx}) - \alpha sign(S_{dx})$$

λ and α are positive constants.
The super twisting control laws of the inverter's output current's regulations is then given by:

$$v_{idx}^{*} = \frac{\dot{\iota}_{dx}^{*} - f_{dx}(x)}{g_{dx}} - \lambda |S_{dx}|^{\frac{1}{2}} sign(S_{dx}) - \alpha sign(S_{dx}) \quad \text{(IV.23)}$$

$$v_{iqx}^{*} = \frac{\dot{\iota}_{qx}^{*} - f_{qx}(x)}{g_{qx}} - \lambda |S_{dx}|^{\frac{1}{2}} sign(S_{dx}) - \alpha sign(S_{dx}) \quad \text{(IV.24)}$$

IV.5. Control of the parallel inverters using super twisting technique based on the modification of voltage references method for CC suppression

The schematic in Figure IV.2. outlines a control approach that modifies the voltage reference of each inverter based on its output current error, incorporating the Super Twisting Controller (STC) for robustness. The core idea is to indirectly suppress circulating currents by dynamically adjusting the reference voltages in response to real-time current imbalances.

However, while this strategy enhances the current regulation performance under balanced conditions, it lacks an explicit mechanism for detecting or regulating the zero-sequence circulating current. The absence of a dedicated CC feedback loop or ZSC measurement path limits its effectiveness under asymmetrical or mismatched conditions. This is particularly critical in parallel operation, where even slight mismatches in filter impedance or load sharing can give rise to significant CC. As a result, this schematic performs suboptimally when the system is exposed to parameter mismatches or load disturbances, as seen in the simulation results.

Furthermore, the design places a greater reliance on the STC to manage both current tracking and implicit CC suppression, which can saturate its capability and reduce robustness under harsh dynamic transients. Thus, while the schematic represents a step toward enhanced nonlinear control, its structural limitations restrict its full potential in complex, unbalanced operating scenarios.

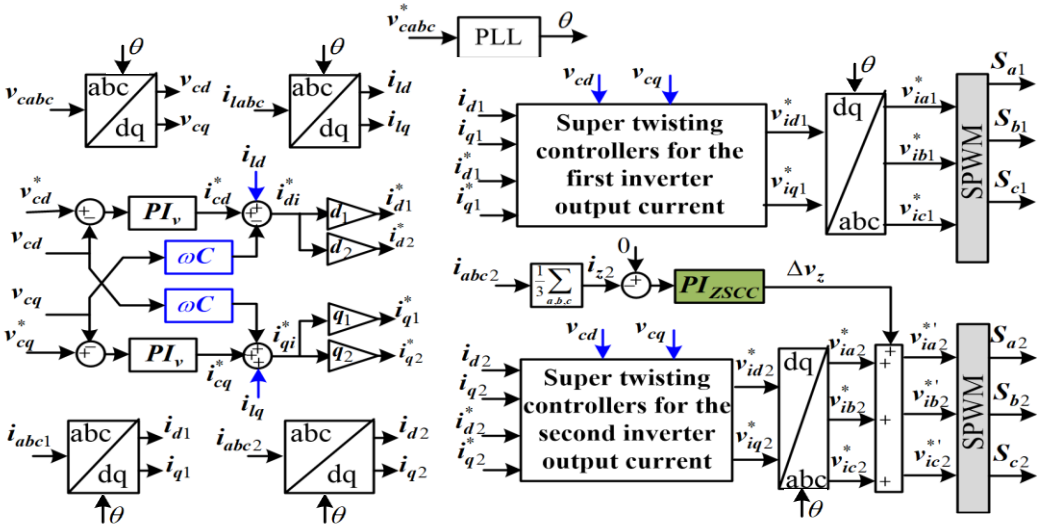


Figure IV 3 Control schematic of the of the parallel inverters using super twisting technique based on the modification of voltage references method for CC suppression

Simulation results

Case 1: Under unbalanced parallel system output filter inductance values

Figure IV.3presents the output currents, circulating current (CC), and total harmonic distortion (THD) for parallel inverters operating under mismatched output filter inductances without CC suppression. The results show significantly degraded current quality, with a CC of 0.4 A and a THD values of 2.31% and 2.57% for the two inverters. These elevated THD levels reflect the adverse impact of filter asymmetry on inverter performance. Furthermore, the lack of a dedicated CC mitigation strategy leads to pronounced zero-sequence circulating currents, which in turn amplify harmonic distortion and compromise current balancing. These findings highlight the necessity for a robust control approach that can suppress CC under component mismatches and maintain power quality.

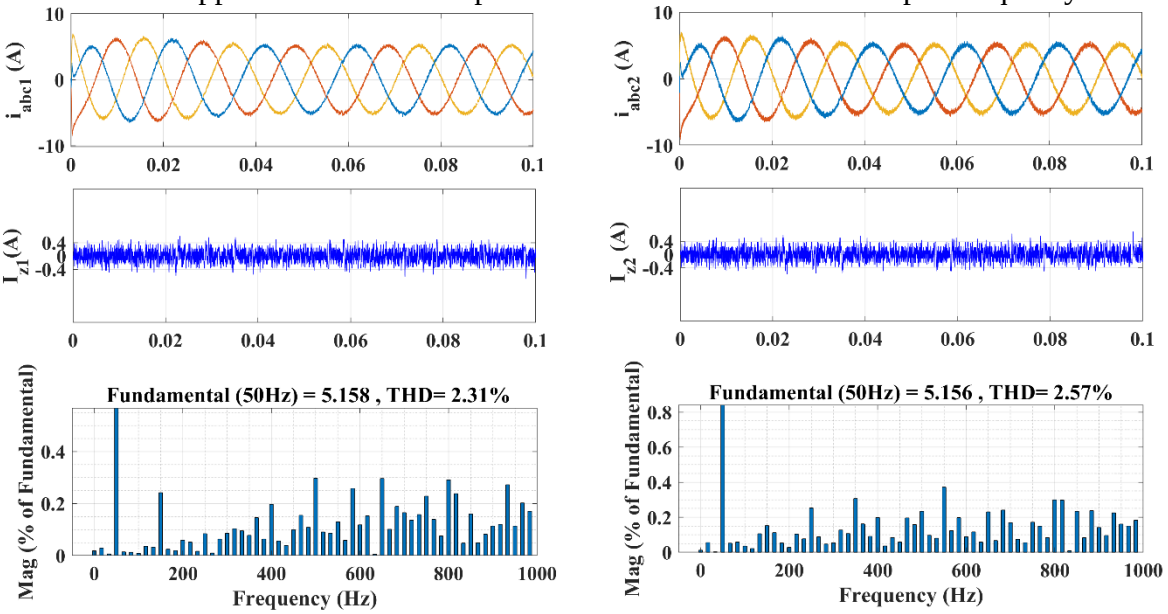


Figure IV 4 Simulation results parallel inverters using super twisting technique based on the modification of voltage references method for CC suppression under mismatched output filter

Case. 2: Under unbalanced parallel system output currents distributions

Figure IV.4 depicts the system response under conditions of unbalanced current distribution, again without CC control. The output currents exhibit poor sharing and uneven waveforms, with THD values ranging from 2.37% to 2.85%. This disparity in current levels between the inverters underscores their lack of coordination, further exacerbated by the presence of high-frequency harmonic components (notably in the 200–1000 Hz range). The results suggest that voltage reference modification alone, in the absence of a dedicated CC control mechanism, is insufficient to ensure current sharing or suppress high-frequency disturbances. An improved approach is thus needed to enhance the synchronization of inverter outputs and mitigate circulating currents effectively.

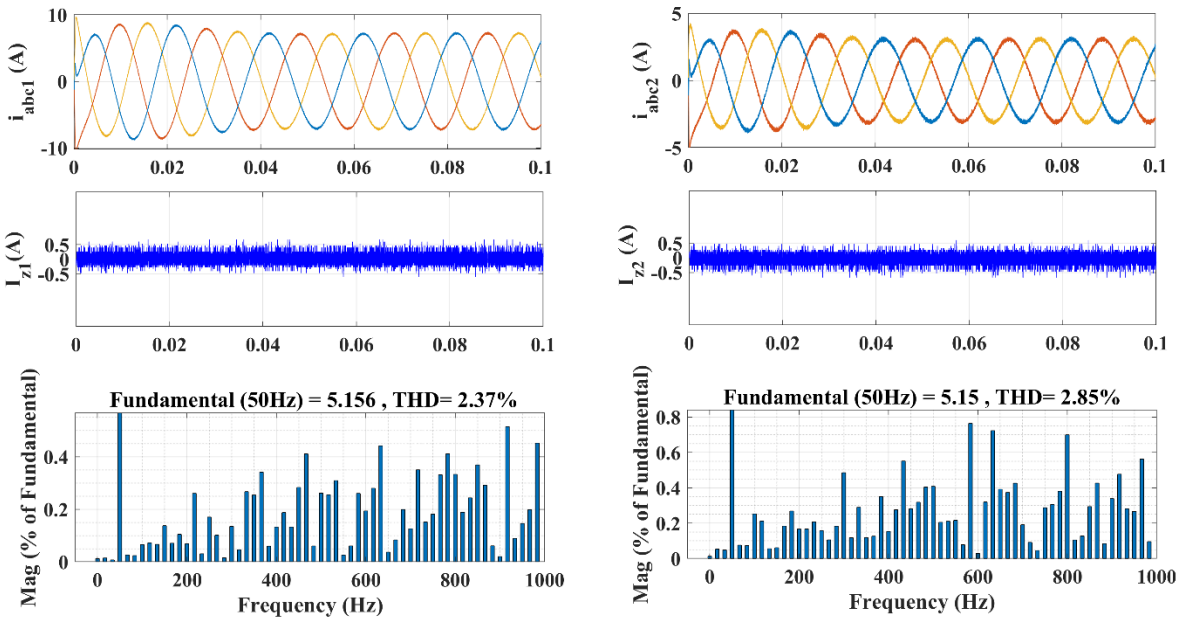


Figure IV 5 Simulation results parallel inverters using super twisting technique based on the modification of voltage references method for CC suppression under unbalanced parallel system output currents.

IV.6. Control of the parallel inverters using super twisting technique based on the ZSC regulation method for CC suppression

Figure IV.5 presents a more refined and comprehensive control architecture that explicitly integrates a zero-sequence current (ZSC) regulation loop into the super twisting control framework. This enhancement fundamentally changes the system's ability to manage circulating current.

The inclusion of ZSC measurement and feedback allows the controller to directly suppress the zero-sequence components in the inverter outputs. By feeding the measured ZSC into a dedicated STC structure, the control system acts to nullify CC in real time, improving the dynamic response and ensuring stable parallel operation, even under filter mismatches or uneven load distributions.

This schematic also promotes modularity and scalability, as the CC regulation layer is decoupled from the individual inverter voltage control loops. This decoupling not only simplifies controller tuning but also enhances the robustness of each inverter's current regulation process. As evidenced by the simulation results, the ZSC-based approach yields superior current symmetry, reduced THD, and almost complete elimination of circulating current, making it highly suitable for reliable parallel inverter operation in standalone.

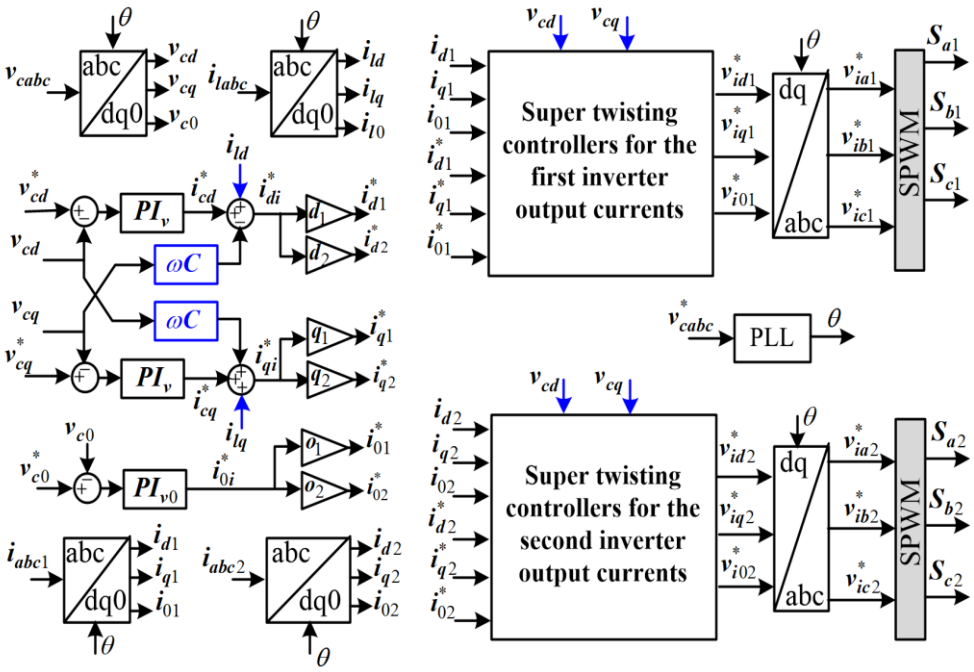


Figure IV 6 Control schematic of the of the parallel inverters using super twisting technique based on the ZSC regulation method for CC suppression

Simulation results

Case 1: Under unbalanced parallel system output filter inductance values

Figure IV.6 illustrates the performance of the super twisting control scheme incorporating ZSC regulation under mismatched output filter conditions. Unlike the previous method, the current waveforms remain well-balanced and sinusoidal, with both inverters operating at the nominal 50 Hz frequency. Crucially, the zero-sequence current components are effectively suppressed and remain close to zero, confirming the robustness of the ZSC-based strategy in eliminating CC, which provided a value of CC about 0.2 A. The THD values are significantly reduced to 2.06% and 2.24%, demonstrating enhanced harmonic mitigation. These results validate the effectiveness of the ZSC regulation method in maintaining stability and high-quality output, even

in the presence of physical mismatches in the output filter inductance values.

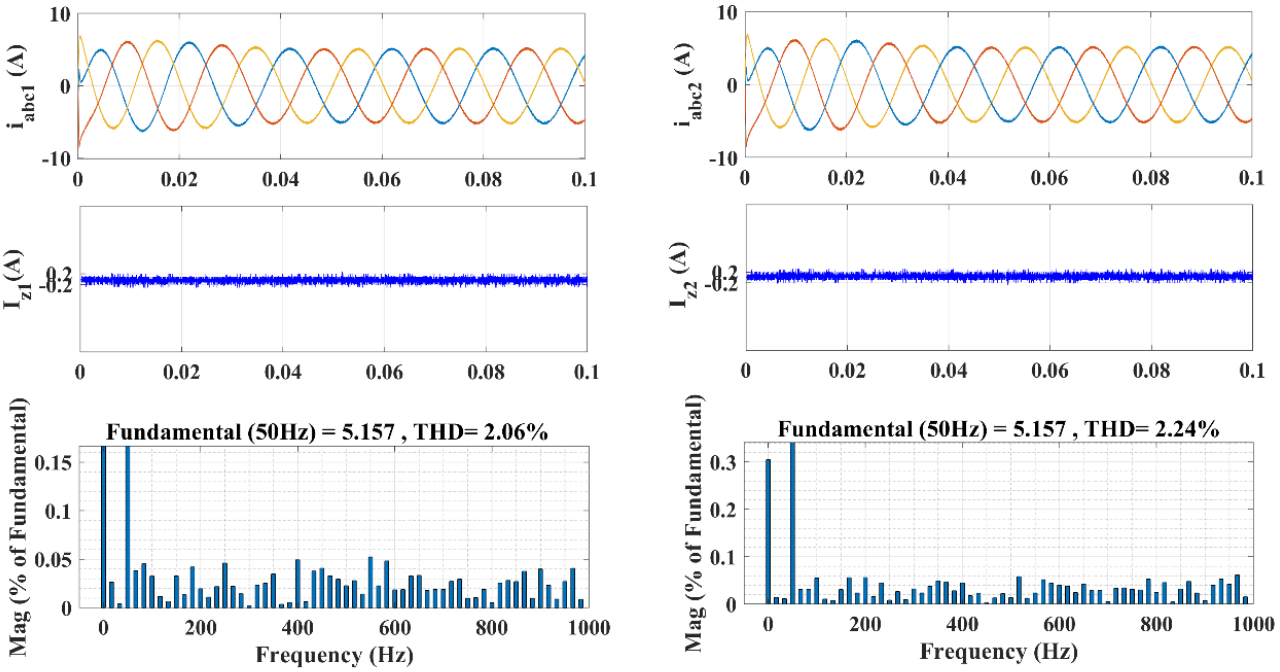


Figure IV 7 Simulation results of the parallel inverters under mismatched output filter using ZSC regulation

Case. 2: Under unbalanced parallel system output currents distributions

The simulation results of this case showing the output currents, CC, and THD of both parallel inverters are shown in Fig. IV.6.

Figure IV.7present parallel inverter's output current regulation performance under unbalanced current sharing when controlled via ZSC regulation. The output currents retain their sinusoidal shape, with THD levels of 2.88% and 3.85%, indicating a substantial improvement compared to the case without CC control. Despite the asymmetry in load sharing, the CC remains well-regulated, and the harmonic content, particularly at higher frequencies, is significantly attenuated. The left-hand case exhibits superior power quality, with a smoother waveform and reduced spectral energy beyond the fundamental frequency. Overall, these outcomes demonstrate that the integration of ZSC regulation within the super twisting control framework significantly enhances inverter synchronization and suppresses both low- and high-frequency harmonic disturbances, even under challenging operating conditions.

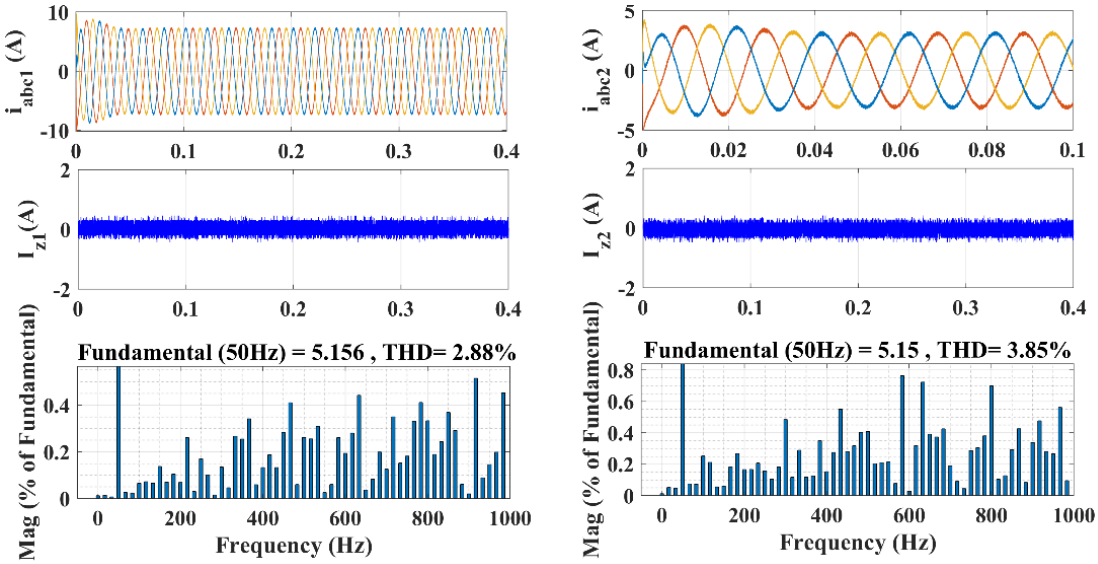


Figure IV 8 Simulation results of the parallel inverters under unbalanced output current using ZSC regulation

IV.7. Conclusion

This chapter has presented a detailed analysis and implementation of both linear and nonlinear control strategies for managing circulating currents and improving the performance of parallel inverter systems under unbalanced conditions. Initially, the chapter reviewed the fundamentals of first-order sliding mode control (SMC), highlighting its robustness to parameter variations and external disturbances. However, the well-known drawback of chattering, associated with SMC, necessitated the exploration of higher-order sliding modes, leading to the adoption of the Super Twisting Algorithm (STA).

The second part of the chapter focused on applying STA to parallel inverter systems, introducing two CC suppression approaches: voltage reference modification and zero-sequence current (ZSC) regulation. Both methods were evaluated under scenarios of unbalanced output filter inductance and unbalanced current distribution. Simulation results showed that while voltage reference modification using STA offered some degree of CC suppression and improved current quality, the integration of a ZSC feedback loop within the STA framework provided significantly better performance. The latter method yielded well-balanced current waveforms, consistently low total harmonic distortion (THD), and almost complete elimination of circulating currents.

A comparative analysis between the PI controller-based methods and the STA-based control strategies revealed the following key insights:

- Dynamic Performance: PI controllers offer acceptable performance in balanced scenarios but fail to adapt under disturbances or parameter mismatches. In contrast, STC demonstrates strong robustness and fast transient response due to its nonlinear nature and finite-time convergence properties.
- Circulating Current Suppression: While PI-based methods indirectly suppress CC through voltage adjustment, their performance deteriorates under unbalanced conditions. STA, particularly when combined with ZSC regulation, explicitly targets CC and maintains near-zero ZSC levels, regardless of system asymmetry.
- Harmonic Mitigation: STA consistently achieves lower THD values in all scenarios compared to PI-based methods, resulting in cleaner, more sinusoidal current outputs.
- Robustness and Scalability: The STC framework proves to be more resilient to filter mismatches and load imbalances, offering scalable performance for future inverter deployments in standalone or weak-grid systems.

In conclusion, while PI controllers remain simple and easy to implement, their limitations under non-ideal conditions restrict their suitability for advanced inverter coordination. The Super Twisting Control approach, especially when integrated with ZSC regulation, emerges as a superior solution for high-performance and disturbance-resilient parallel inverter systems. Future research may extend this work by incorporating adaptive gain tuning and observer-based disturbance estimation to further enhance system robustness and energy efficiency.

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Abstract

This thesis presents a comprehensive control strategy for parallel three-phase inverters operating in standalone mode, specifically addressing the critical issue of circulating current elimination under challenging operating conditions. The research focuses on developing robust control methods to manage circulating currents that arise between parallel inverters when subjected to unbalanced output inductive filters and unequal output current demands. The primary challenge addressed in this work stems from the inherent mismatch in output inductances and unequal output current demands, which create differential voltage drops across parallel inverter branches. These mismatches lead to unwanted circulating currents that reduce system efficiency, increase component stress, and compromise the overall reliability of the parallel inverter configuration.

A novel control method was developed and implemented to actively suppress circulating currents while maintaining balanced three-phase output voltages and currents. The proposed control scheme incorporates advanced super twisting output current regulations and modified pulse-width modulation (PWM) patterns based on inverter output voltage reference adjustments using the regulation of the circulating current with zero via PI controller that account for filter imbalances and unequal output current demands. Extensive simulation studies were conducted to evaluate the effectiveness of the proposed control method. The results demonstrate significant reduction in circulating currents and improvement in parallel inverter's output current quality under various operating scenarios, including unbalanced output inductive filters and unequal output current demands. The control system successfully maintains proper output currents among parallel inverters while ensuring stable operation and improved power quality.

This work provides valuable insights for the design and control of parallel inverter systems in standalone applications, particularly in renewable energy systems, uninterruptible power supplies, and distributed generation systems where reliable operation under varying conditions is essential.

Keywords

Parallel three phase inverters, circulating current suppression, standalone operation, unbalanced inductive filters, output current sharing, output voltage reference adjustments method.

الملخص

تقدم هذه المذكرة إستراتيجية تحكم شاملة للمحولات الثلاثية الطور المتصلة على التوازي والتي تعمل في الوضع المستقل، مع التركيز بشكل خاص على معالجة مشكلة التيارات الدورانية بين المحولات تحت ظروف التشغيل الصعبة. يركز البحث على تطوير طرق تحكم قوية للتحكم في التيارات الدورانية التي تظهر بين المحولات المتوازية نتيجة لاختلال توازن مرشحات الخرج الحثية واختلاف متطلبات تيار الخرج. تتمثل التحديات الرئيسية التي تم معالجتها في هذا العمل في عدم تطابق الحثيات عند الخرج واختلاف تيارات الخرج المطلوبة، مما يؤدي إلى فروقات في الجهد بين فروع المحولات المتوازية، ومن ثم إلى توليد تيارات دورانية غير مرغوبة تقلل من كفاءة النظام وتزيد من الضغط على المكونات وتؤثر سلبًا على موثوقية النظام.

تم تطوير وتنفيذ طريقة تحكم جديدة لكبح التيارات الدورانية بشكل فعال مع الحفاظ على توازن جهود وتيارات الخرج الثلاثية الطور. تتضمن الخطة المقترحة تقنيات متقدمة لتنظيم تيار الخرج باستخدام خوارزمية"Super-Twisting" ، بالإضافة إلى تعديل أنماط التضمين بعرض النبضة (PWM) بناءً على ضبط مرجع جهد الخرج من خلال تنظيم التيار الدوراني ليكون صفريًا باستخدام متحكمPI ، مع الأخذ بعين الاعتبار اختلالات المرشح واختلاف متطلبات تيارات الخرج. تم إجراء دراسات محاكاة موسعة لتقييم

فعالية الطريقة المقترحة، وأظهرت النتائج انخفاضًا ملحوظًا في التيارات الدورانية وتحسنًا في جودة تيار الخرج للمحولات المتوازية تحت مختلف سيناريوهات التشغيل، بما في ذلك وجود مرشحات حثية غير متوازنة واختلافات في متطلبات تيار الخرج.

يوفر هذا العمل رؤى مهمة لتصميم أنظمة المحولات المتوازية وتحكمها في التطبيقات المستقلة، وخصوصًا في أنظمة الطاقة المتجددة، ومزودات الطاقة غير المنقطعة، وأنظمة التوليد الموزعة، حيث تعتبر الموثوقية التشغيلية تحت ظروف متغيرة أمرًا بالغ الأهمية.

الكلمات المفتاحية:

محولات ثلاثية الطور متوازية، كبح التيار الدوراني، التشغيل المستقل، مرشحات حثية غير متوازنة، تقاسم تيار الخرج، طريقة ضبط مرجع جهد الخرج.